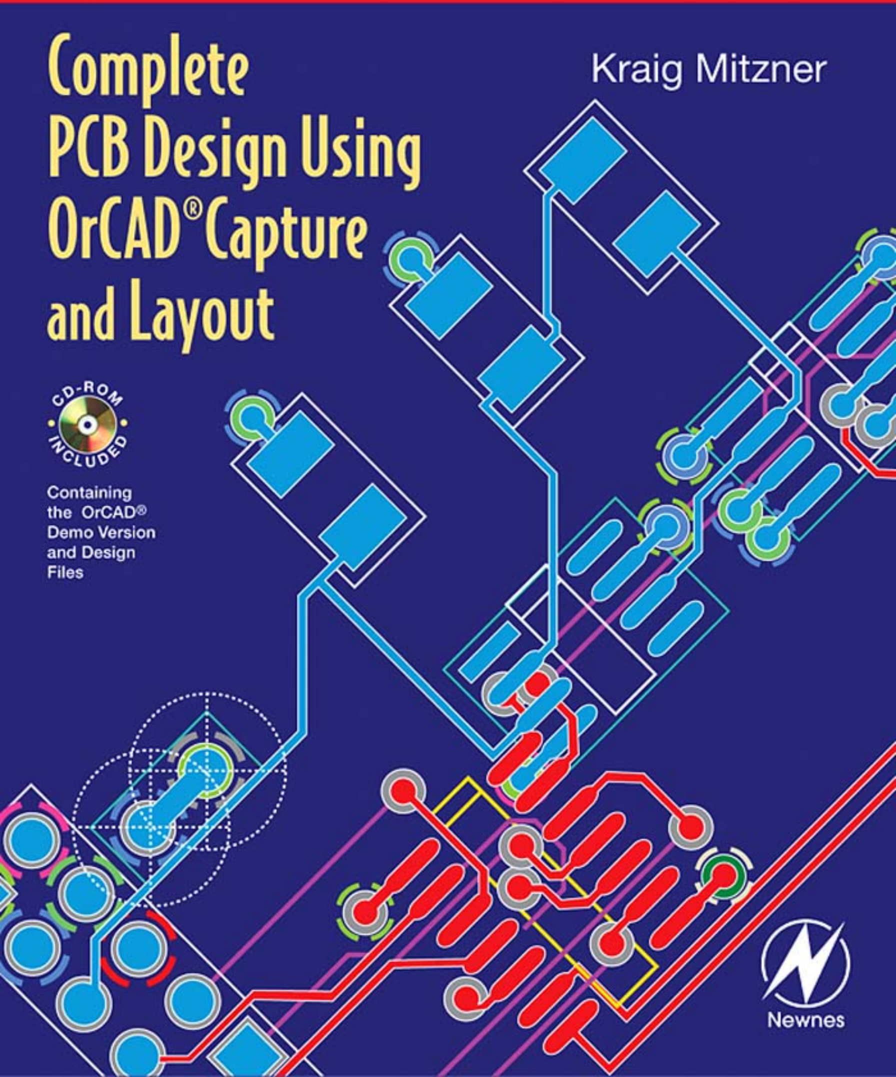
Complete PCB Design Using OrCAD® Capture and Layout

Kraig Mitzner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Complete PCB Design Using OrCad Capture and Layout

By

Kraig Mitzner

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Linacre House, Jordan Hill, Oxford OX2 8DP, UK

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Library of Congress Cataloging-in-Publication Data
Mitzner, Kraig.
Complete PCB design using OrCad capture and layout / Kraig Mitzner.
p. cm.
Includes bibliographical references and index.
ISBN-13: 978-0-7506-8214-5 (pbk. : alk. paper)
ISBN-10: 0-7506-8214-0 (pbk. : alk. paper) 1. Printed circuits—Design and construction.
2. OrCAD SDT. I. Title.
TK7868.P7.M56 2007
621.3815'31—dc22
2006034059

British Library Cataloguing-in-Publication Data
A catalogue record for this book is available from the British Library.

ISBN-13: 978-0-7506-8214-5
ISBN-10: 0-7506-8214-0

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Typeset by Charon Tec Ltd (A Macmillan Company), Chennai, India
www.charontec.com
Printed in China.

07 08 09 10 10 9 8 7 6 5 4 3 2 1

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Table of Contents

INTRODUCTION xv

ACKNOWLEDGMENTS xix

CHAPTER 1

INTRODUCTION TO PCB DESIGN AND CAD 1

Computer-Aided Design and the OrCAD Design Suite 1

Printed Circuit Board Fabrication 2

  PCB cores and layer stack-up 2

  PCB fabrication process 4

  Photolithography and chemical etching 5

  Mechanical milling 8

  Layer registration 9

Function of OrCAD Layout in the PCB Design Process 11

Design Files Created by Layout 14

  Layout format files (.MAX) 14

  Postprocess (Gerber) files 14

  PCB assembly layers and files 14

CHAPTER 2

INTRODUCTION TO THE PCB DESIGN FLOW BY EXAMPLE 17

Overview of the Design Flow 17

Creating a Circuit Design with Capture.....17
Starting a new project.....17
Placing parts.....20
Wiring (connecting) the parts.....23
Creating the Layout netlist in Capture.....23
Designing the PCB with Layout.....25
Starting Layout and importing the netlist.....25
Making a board outline.....29
Placing the parts.....31
Autorouting the board.....32
Manual routing.....32
Cleanup.....34
Locking traces.....34
Performing a design rule check.....35
Postprocessing the board design for manufacturing.....35

CHAPTER 3

PROJECT STRUCTURES AND THE LAYOUT TOOL SET.....39
Project Setup and Schematic Entry Details.....39
Capture projects explained.....39
Capture part libraries explained.....42
Understanding the Layout Environment and Tool Set.....43
Board technology files.....43
The AutoECO utility.....44
The session frame and Design window.....46
The toolbar.....47
Controlling the autorouter.....57
Postprocessing and layer details.....60

CHAPTER 4

INTRODUCTION TO INDUSTRY STANDARDS.....65
Introduction to the Standards Organizations.....66

Institute for Printed Circuits (IPC-Association Connecting Electronics Industries) 66
Electronic Industries Alliance (EIA) 66
Joint Electron Device Engineering Council (JEDEC) 66
International Engineering Consortium (IEC) 67
Military Standards 67
American National Standards Institute (ANSI) 67
Institute of Electrical and Electronics Engineers (IEEE) 67
Classes and Types of PCBs 68
Performance classes 68
Producibility levels 68
Fabrication types and assembly subclasses 69
OrCAD Layout design complexity levels—IPC performance classes 69
IPC land pattern density levels 70
Introduction to Standard Fabrication Allowances 70
Registration tolerances 70
Breakout and annular ring control 70
PCB Dimensions and Tolerances 71
Standard panel sizes 71
Tooling area allowances and effective panel usage 72
Standard finished PCB thickness 72
Core thickness 73
Prepreg thickness 73
Copper thickness for PTHs and vias 73
Copper cladding/foil thickness 74
Copper Trace and Etching Tolerances 75
Standard Hole Dimensions 76
Soldermask Tolerance 77
End Note 77
Suggested reading 77
Other items of interest 77

CHAPTER 5

INTRODUCTION TO DESIGN FOR MANUFACTURING 79
Introduction to PCB Assembly and Soldering Processes 79
Assembly Processes 79
    Manual assembly processes 79
    Automated assembly processes (pick and place) 80
Soldering Processes 81
    Manual soldering 81
    Wave soldering 82
    Reflow soldering 84
Component Placement and Orientation Guide 85
Component Spacing for Through-hole Devices 86
    Discrete THDs 86
    Integrated circuit through-hole devices 86
    Mixed discrete and IC through-hole devices 86
    Holes and jumper wires 86
    Component Spacing for Surface-Mounted Devices 86
    Discrete SMDs 86
    Integrated-circuit SMDs 86
    Mixed discrete and IC SMDs 86
Mixed THD and SMD Spacing Requirements 86
Footprint and Padstack Design for PCB Manufacturability 94
Land Patterns for Surface-Mounted Devices 94
    SMD padstack design 96
    SMD footprint design 99
Land Patterns for Through-hole Devices 101
    Footprint design for through-hole devices 101
    Padstack design for through-hole devices 103
    Hole-to-lead ratio 103
    PTH land dimension (annular ring width) 104
    Clearance between plane layers and PTHs 106
    Soldermask and solder paste dimensions 107

CHAPTER 6

PCB DESIGN FOR SIGNAL INTEGRITY 109
Circuit Design Issues Not Related to PCB Layout.................................109
  Noise 109
  Distortion..110
  Frequency response 111
  Issues Related to PBC Layout 111
  Electromagnetic Interference and Cross Talk.................................111
  Magnetic fields and inductive coupling 112
  Loop inductance...115
  Electric fields and capacitive coupling...117
Ground Planes and Ground Bounce 119
  What ground is and what it is not 119
  Ground (return) planes...122
  Ground bounce and rail collapse...123
  Split power and ground planes 125
PCB Electrical Characteristics...127
  Characteristic impedance 127
  Reflections 133
  Ringing...137
  Electrically long traces...139
  Critical length..142
  Transmission line terminations 143
PCB Routing Topics 144
  Parts placement for electrical considerations 145
  PCB layer stack-up 146
  Bypass capacitors and fanout 151
  Trace width for current carrying capability 151
  Trace width for controlled impedance 153
  Trace spacing for voltage withstanding..163
  Trace spacing to minimize cross talk (3w rule)..............................163
  Traces with acute and 90° angles 164

CHAPTER 7

MAKING AND EDITING CAPTURE PARTS 167

The Capture Part Libraries...167

Types of Packaging 168

- *Homogeneous parts 168*
- *Heterogeneous parts..169*

Pins..169

Part Editing Tools 170

- *The Select tool and settings...170*
- *The pin tools...170*
- *The graphics tools...171*
- *The zoom tools..171*

Constructing Capture Parts 171

Method 1: Constructing Parts Using the New Part Option (Design Menu)..172

- *Design example for a passive, homogeneous part 172*
- *Design example for an active, multipart, homogeneous component 180*
- *Assigning power pin visibility 183*
- *Design example for a passive, heterogeneous part.........................184*

Method 2: Constructing Parts with Capture Using the Design Spreadsheet...187

Method 3: Constructing Parts Using Generate Part from the Tools Menu...190

Method 4: Generating Parts with the PSpice Model Editor....................192

- *Generating a Capture part library from a PSpice model library...193*
- *Making and/or Obtaining PSpice Libraries for Making New Capture Parts..194*
- *Downloading libraries and/or models from the Internet 195*
- *Making a PSpice model from a Capture project...............................196*
- *Adding PSpice templates (models) to preexisting Capture parts 206*

Constructing Capture Symbols 208

CHAPTER 8

MAKING AND EDITING LAYOUT FOOTPRINTS 211

Introduction to the Library Manager 211
- Introduction to Layout's Footprint Libraries and Naming Conventions 212
- Layout's footprint libraries..213
- Naming conventions..213

The Composition of Footprints..217
- Padstacks 217
- Obstacles 218
- Text 220
- Datums and insertion origins..220

The Basic Footprint Design Process 221

Working with Padstacks..226
- Accessing existing padstacks 227
- Editing padstack properties from the spreadsheet..228
- Saving footprints and padstacks 229

Footprint Design Examples 231
- Design example 1: a surface-mount footprint design 232
- Design example 2: a modified through-hole footprint design 237

Using the Pad Array Generator..243
- Introduction..243
- Footprint design for PGAs..243
- Footprint design for BGAs..248
- Blind, buried, and microvias..258
- Mounting holes..259
- Printing a catalog of a footprint library..261

CHAPTER 9

PCB DESIGN EXAMPLES 263

Overview of the Design Flow 264

Example 1: Dual Power Supply, Analog Design 266
Initial design concept and preparation 267
Project setup and design in Capture 268
Defining the board requirements..285
Importing the design into Layout..288
Setting up the board 289
Prerouting the board..306
Autorouting the board..316
Finalizing the design...318
Example 2: Mixed Analog/Digital Design Using Split Power, Ground Planes...322
Mixed-signal circuit design in Capture..322
Power and ground connections to digital and analog parts.............324
Connecting separate analog and digital grounds to a split plane 324
Using busses for digital nets...327
Defining the layer stack-up for split planes 328
Establishing a primary power plane..330
Creating split ground planes...334
Creating nested power planes with copper pours............................336
Using anti-copper on plane layers...338
Setting up and running the autorouter 340
Moving a routed trace to a different layer..342
Adding ground planes and guard traces to routing layers 342
Defining vias for flood planes/pours...345
Setting the copper pour spacing 347
Stitching a ground plane manually 348
Using anti-copper obstacles on copper pours 349
Routing guard traces and rings 349
Example 3: Multipage, Multipower, and Multiground Mixed A/D PCB Design with PSpice...352
Project setup for PSpice simulation and Layout................................354
Adding schematic pages to the design 356

- Using off-page connectors with wires ... 358
- Using off-page connectors with busses ... 359
- Setting up multiple-ground systems ... 359
- Setting up PSpice sources ... 360
- Performing PSpice simulations ... 361
- Preparing the simulated project for Layout ... 364
- Assigning a new technology file ... 365
- Placing parts on the bottom (back) of a board ... 365
- Layer stack-up for a multiground system ... 365
- Net layer assignments ... 367
- Through-hole and blind via setup ... 367
- Fanning out a board with multiple vias ... 367
- Overriding known errors in Layout ... 370
- Autorouting with the DRC/route box ... 370
- Using forced thermals to connect ground planes ... 372
- Using the AutoECO to update a board from Capture ... 372

Example 4: High-Speed Digital Design ... 376
- Layer setup for microstrip transmission lines ... 380
- Via design for heat spreaders ... 381
- Constructing a heat spreader with copper area obstacles ... 382
- Using free vias as heat pipes ... 382
- Determining critical trace length of transmission lines ... 387
- Routing controlled impedance traces ... 388
- Moated ground areas for clock circuits ... 390
- Routing curved traces ... 390
- Gate and pin swapping ... 392
- Stitching a ground plane with the free via matrix ... 395

Miscellaneous Items ... 397
- Fixing bad pad exits ... 397
- Design cache—cleanup, replace, update ... 398
- Adding test points ... 400
- Types of AutoECOs ... 401

Making a custom Capture template....403
Making a custom Layout technology/template file....403
Using the Stackup Editor....404
Using the Stackup Editor with an active board design....404
Using the Stackup Editor to set up a custom technology or template file....407
Submitting stack-up drawings with Gerber files....408
Adding solder thieves....408
Printing a footprint catalog from a PCB design....409

CHAPTER 10

POSTPROCESSING AND BOARD FABRICATION....411
The Circuit Design with OrCAD....411
Schematic design in Capture....411
The board design with Layout....413
Postprocessing the design with Layout....414
Fabricating the Board....417
Choosing a board house....417
Setting up a user account....417
Submitting Gerber files and requesting a quote....418
Annotating the layer types and stack-up....419
Receipt inspection and testing....422
Nonstandard Gerber files....422

CHAPTER 11

ADDITIONAL TOOLS....423
Using PSpice to Simulate Transmission Lines....423
Simulating digital transmission lines....424
Simulating analog signals....427
Using Microsoft Excel with a Bill of Materials Generated by Capture....427
Using the SPECCTRA Autorouter with Layout....429

Introduction to GerbTool..437
Opening a Layout-generated Gerber file with GerbTool 437
Making a .DRL file for a CNC machine...438
Panelization...443
Using the IPC-7351 Land Pattern Viewer 449
Using CAD Tools to 3-D Model a PCB 452

APPENDICES

Appendix A: Layout Technology Files 455
Appendix B: List of Design Standards...457
Appendix C: A Partial List of Packages and Footprints and Some of the Footprints Included in OrCAD Layout............................459
Appendix D: Rise and Fall Times for Various Logic Families....................471
Appendix E: Drill and Screw Dimensions...473
Appendix F: References by Subject 475

BIBLIOGRAPHY AND REFERENCES 491

INDEX...495

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Introduction to Complete PCB Design Using OrCAD Capture and Layout

I did not write this book because I am an OrCAD guru. I wrote it because no up-to-date references were available when I was trying to learn how to use the software. This book is the one I wish I would have had. This book was born from notes I compiled as I learned (the hard way) to use the software. The initial intent of the book was to describe how to use OrCAD Layout specifically. Along the way, though, I realized also that I (and many of the engineers I talked to) had a lot to learn about the printed circuit board (PCB) design process itself. There was a significant amount of information available on PCB design from both the electrical and the manufacturing aspects, but there was not an easily accessible resource that covered those subjects with how to use the software. That is the intent of this book.

Chapter 1 introduces the reader to the basics of PCB design. The chapter begins by introducing the concepts of computer-aided engineering, computer-aided design, and computer-aided manufacturing. The chapter then explains how these tools are used to design and manufacture multilayer PCBs. Many 3-D pictures are used to show the construction of PCBs. Topics such as PCB cores and layer stack-up, apertures, D-codes, photolithography, layer registration, plated through-holes, and Gerber files are explained.

Chapter 2 leads new users of the software through a very simple design example. The purpose of the example is to paint a “big picture” of the design flow process. The example begins with a blank schematic page and ends with the Gerber files. The circuit is ridiculously simple so that it is not a distraction to understanding the process itself. Along the way some of Layout’s routing tools are briefly introduced along with some of the other tools, which sets the stage for Chap. 3.

Chapter 3 provides an overview of the OrCAD project files and structure and explains Layout’s tool set in detail. The chapter revisits and explains some of the actions performed and tools used during the example in Chap. 2. Gerber files are also explained in detail.

Chapter 4 introduces some of the industry standards organizations related to the design and fabrication of PCBs (e.g., IPC and JEDEC). PCB performance classes and producibility levels are also described along with the basic ideas behind standard fabrication allowances. These concepts are described here to help the reader realize some of the fabrication issues up front to help minimize board failures and to identify some of the guides and standards resources that are available for PCB design.

Chapter 5 addresses the mechanical aspect of PCB design—design for manufacturability (DFM). The chapter explains where parts should be placed on the board, how far apart, and in what orientation from a manufacturing perspective. OrCAD Layout's design rule checker is then considered relative to the manufacturing concepts and IPC's courtyard concepts. To aid in understanding the design issues, manufacturing processes such as reflow and wave soldering, pick-and-place assembly, and thermal management are discussed. The information is then used as a guide in designing plated through-holes, surface-mount lands, and Layout footprints in general. Tables summarize the information and serve as a design guide during footprint design and PCB layout.

Chapter 6 addresses the electrical aspect of PCB design. There are several good references available on signal integrity, electromagnetic interference, and electromagnetic compatibility. Chapter 6 provides an overview of those topics and applies them directly to PCB design. Topics such as loop inductance, ground bounce, ground planes, characteristic impedance, reflections, and ringing are discussed. The idea of "the unseen schematic" (the PCB layout) and its role in circuit operation on the PCB is introduced. Look-up tables and equations are provided to determine required trace widths for current handling and impedance as well as required trace spacing for high-voltage designs and high-frequency designs. Various layer stack-up topographies for analog, digital, and mixed-signal applications are also described. The design examples in Chap. 9 demonstrate how to apply the layer stack-ups described in this chapter.

Chapter 7 explains how to construct Capture parts using the Capture Library Manager and Part Editor and the PSpice Model Editor. Heterogeneous and homogeneous parts are developed in examples using four different methods. Different methods are used depending on whether a part will be used for simple schematic entry, design projects intended for PCB layout, PSpice simulations, or all of the above. The chapter also demonstrates how to attach PSpice models to Capture's schematic parts using PSpice models downloaded from the Internet and basic PSpice models developed from functional Capture projects. The Capture parts can then be used for both PSpice simulations and PCB layout as demonstrated in Chap. 9.

Detailed coverage of padstacks and footprints is covered in Chap. 8. The chapter introduces the Layout Library Manager, Layout's footprint naming conventions, and the basic composition of a footprint. Then a detailed description of the padstack (as it relates to PCB manufacturing described in Chaps. 1 and 5) is given, as it is the foundation of both footprint design and PCB routing. Design examples are provided to demonstrate how to design discrete through-hole and surface-mount devices and how to use the pad array generator to design footprints for pin grid arrays and ball grid arrays with dogbone fanouts included with the footprint.

Chapter 9 provides four PCB design examples that use the material covered in the previous eight chapters. The first example is a simple analog design using a single op-amp. The design shows how to set up multiple plane layers for positive and negative power supplies and ground. The design also demonstrates several key concepts in Capture, such as how to connect global nets, how to assign footprints, how to perform design rule checks, how to use the Capture part libraries, how to generate a bill of materials (BOM), and how to use the BOM as an aid in the design process in Capture and Layout. The design also shows how to perform important tasks in Layout such as how to load board technology files, locate specific parts, and modify padstacks. Intertool communication (such as annotation and back annotation) between Capture and Layout is also demonstrated. The second design is a mixed digital/analog circuit. In addition to the tasks demonstrated in the first example, the design also demonstrates how to set up and use split planes to isolate analog and digital power supplies and grounds. Other tasks include using copper pours on routing layers to make partial ground planes, using copper pours on plane layers to make nested power and ground planes, and defining anti-copper areas on plane and routing layers. The third example uses the same mixed digital/analog circuit from the second example but demonstrates how to use multiple page schematics and off-page connectors to add PSpice simulations to a Capture project used for PCB layout, all within a single project design. It also demonstrates how to construct multiple, separated power and ground planes and a shield plane to completely isolate analog from digital circuitry. The use of guard rings and guard traces is also demonstrated. The fourth example is a high-speed digital design, which demonstrates how to design transmission lines, stitch multilayer ground planes, perform pin/gate swapping, place moated ground areas for clock circuitry, and design a heat spreader.

Chapter 10 describes how to postprocess a PCB design and generate specific Gerber files. Through an example it is shown how to relate the OrCAD Layout design perspective and layer stack-up (including image polarity) to the board manufacturer's perspective by submitting Gerber files to an actual board manufacturer via the Internet. The discussion also provides an example fabrication quote. Nonstandard Gerber files are briefly discussed as well as Gerber files that are generated for PCBs with nonplated mounting holes.

Chapter 11 introduces other tools that can be used with OrCAD Capture and Layout to enhance the PCB design process. The chapter provides examples of how to use Microsoft Excel with the bill of materials generated by Capture to create parts lists and various other tracking documents that can be used during the PCB layout process to minimize design errors. Other examples include how to use PSpice to simulate transmission lines to aid in circuit design and PCB layout, how to use the SPECCTRA autorouter with Layout to route high-density PCB designs faster and with less manual cleanup, how to use GerbTool to panelize a board design, and how to use Layout to generate a .DXF file that can be used by a graphics program to construct a 3-D image of your board design. The IPC Land Pattern Viewer is also introduced in this chapter.

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Acknowledgments

The author would like to thank the following:

My wife Jody, son Stephen, and daughter Chelsey: thank you for your endless patience and understanding. This book is dedicated to you. Without your support this book could not have been completed.

Cadence Design Systems, Inc. for allowing Elsevier to distribute OrCAD software with this book.

Chuck Glaser (and everyone else) at Elsevier for enthusiastically taking on a first-time author.

Advanced Circuits for allowing me to use their Web site to write Chap. 10.

Dr. Jeff Will at Valparaiso University for his encouragement at “just the right time” and his invaluable feedback during the writing process.

Dr. David Galipeau at South Dakota State University for teaching me about the writing process and for giving me the courage to face criticism: “Good writing is not written, it is rewritten.”

And most importantly God for giving me the gift of curiosity, the drive to figure things out, and the desire to share that knowledge with others.

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CHAPTER 1

Introduction to PCB Design and CAD

Computer-Aided Design and the OrCAD Design Suite

Before digging into the details of Layout, we will take a moment to discuss computer-aided engineering (CAE) tools in general. Computer-aided engineering tools cover all aspects of engineering design from drawings to analysis to manufacturing. Computer-aided design (CAD) is a category of CAE that is related to the physical layout and drawing development of a system design. CAD programs specific to the electronics industry are known as electronic CAD (ECAD) or electronic design automation (EDA). EDA tools reduce development time and cost because they allow designs to be simulated and analyzed prior to purchasing and manufacturing hardware. Once a design has been proven through drawings, simulations, and analysis, the system can be manufactured. Applications used in manufacturing are known as computer-aided manufacturing (CAM) tools. CAM tools use software programs and design data (generated by the CAE tools) to control automated manufacturing machinery to turn a design concept into reality.

So how does OrCAD/Cadence fit into all of this? Cadence owns and manages many types of CAD/CAM products related to the electronics industry, including the OrCAD design suite. The OrCAD design suite can be purchased through resellers such as EMA Design Automation, Inc., who package different combinations of CAD/CAM applications, including Capture, PSpice, and Layout, to suit customers' needs. Although these applications can operate individually, bundling the individual tools into one suite allows for intertool communication. The OrCAD tools can also interact with other CAD/CAM tools such as GerbTool, SPECCTRA, or Allegro. Chapter 11 covers the use of these tools with OrCAD.

Capture is the centerpiece of the package and acts as the prime EDA tool. Capture contains extensive parts libraries that may be used to generate schematics that stand alone or that interact with PSpice, or Layout, or both simultaneously. A representation of a Capture part is shown in Fig. 1-1. The pins on a Capture part can be mapped into the pins of a PSpice model and/or the pins of a physical package in Layout. PSpice is a CAE tool that contains the mathematical models for performing simulations, and Layout is a CAD tool that converts a symbolic schematic diagram into a physical representation of the design. Netlists are used to interconnect parts within a design and connect each of the parts with its model and footprint. In addition to being a CAD tool, Layout also functions as a front-end CAM tool by generating the data on which other CAM

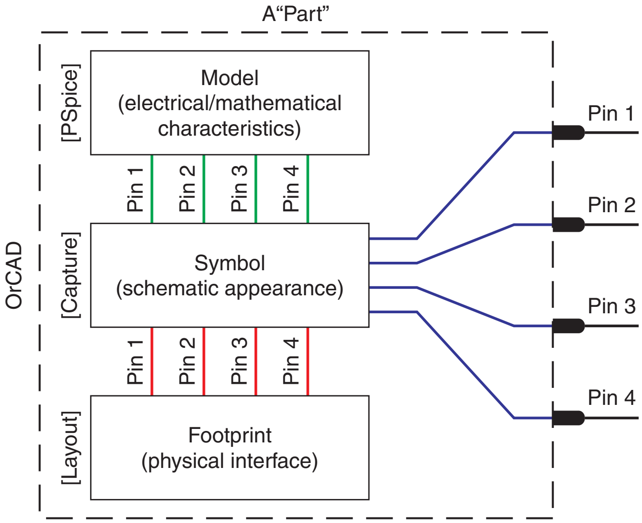


Figure 1-1 The pieces of a "part."

tools operate when manufacturing the printed circuit board (PCB) (GerbTool, for example). By combining all three applications into one package you have a powerful set of tools to efficiently design, test, and build electronic circuits. The key to successful project design and production is in understanding the PCB itself and knowing how to use the tools that build the PCB.

Printed Circuit Board Fabrication

We now look at how PCBs are manufactured so that we will have a better understanding of what we are trying to accomplish with Layout and why. A PCB consists of two basic parts: a substrate (the board) and printed wires (the copper traces). The substrate provides a structure that physically holds the circuit components and printed wires in place and provides electrical insulation between conductive parts. A common type of substrate is FR4, which is a fiberglass–epoxy laminate. It is similar to older types of fiberglass boards but is flame resistant. Substrates are also made from Teflon, ceramics, and special polymers.

PCB cores and layer stack-up

During manufacturing the PCB starts out as a copper clad substrate as shown in Fig. 1-2. A rigid substrate is a C-stage laminate (fully cured epoxy). The copper cladding may be copper that is plated onto the substrate or copper foil that is glued to the substrate. The thickness of the copper is measured in ounces (oz) of copper per square foot, where 1.0 oz/ft^2 of copper is approximately 1.2–1.4 mils (0.0012–0.0014 in.) thick. It is common to drop "/ft^2" and refer to the thickness only in oz. For example, you can order 1 oz copper on a $\frac{1}{8}$-in.-thick FR4 substrate.

A substrate can have copper on one or both sides. Multilayer boards are made up of one or more single- or double-sided substrates called cores. A core is a copper-plated epoxy laminate. The cores are glued together with one or more sheets of a partially cured epoxy as shown in

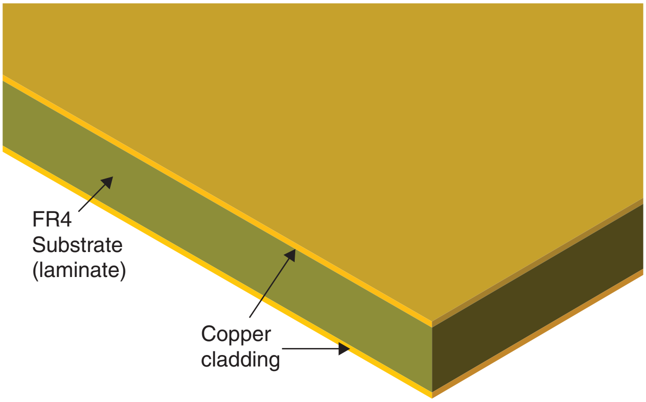

FR4
Substrate
(laminate)
Copper
cladding

Figure 1-2 A double-sided copper clad FR4 substrate.

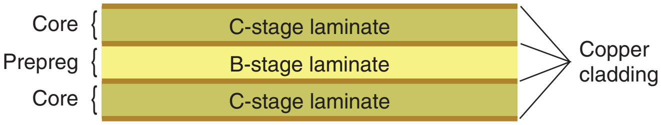

Core
Prepreg
Core
C-stage laminate
B-stage laminate
C-stage laminate
Copper
cladding

Figure 1-3 Cores and prepreg.

Fig. 1-3. The sheets are also referred to as prepreg or B-stage laminate. Once all of the cores are patterned (described below) and aligned, the entire assembly is fully cured in a heated press.

There are three methods of assembling the cores when making a multilayer board. Figure 1-4 shows the first two methods in an example with four routing layers and two plane layers. Figure 1-4(a) shows three (double-sided) cores bonded together by two prepreg layers, while Fig. 1-4(b) shows the same six layers made of two cores, which make up the four inner layers, bonded together by one prepreg layer. The outer layers in 1-4(b) are copper foil sheets bonded to the assembly with prepreg.

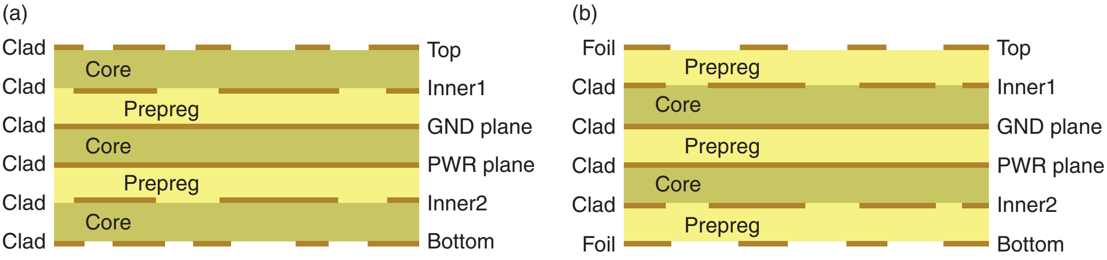

(a)
Clad
Core
Clad
Prepreg
Clad
Core
Clad
Prepreg
Clad
Core
Clad
Top
Inner1
GND plane
PWR plane
Inner2
Bottom
(b)
Foil
Prepreg
Clad
Core
Clad
Prepreg
Clad
Core
Clad
Prepreg
Foil
Top
Inner1
GND plane
PWR plane
Inner2
Bottom

Figure 1-4 Two stack-up methods for a six-layer board. (a) Multicore, outer clad. (b) Multicore, outer foil.

The routing layers in Fig. 1-4 are shown as patterned copper segments and the plane layers are shown as solid lines. The inner layers are patterned prior to bonding the cores together. The outer layers are patterned later in the process after the cores have been bonded and cured and most of the holes have been drilled. Because the outer layers are etched later and because copper foil is typically less expensive than copper cladding, the stack-up shown in Fig. 1-4(b) is more widely used.

The third method uses several fabrication techniques by which highly complex boards can be fabricated, as illustrated in Fig. 1-5. This circuit board may have a typical four-layer core stack-up at its center, but additional layers are built up layer by layer on the top and the bottom using sequential lamination techniques. The techniques can be used to produce blind and buried vias as well as typical plated through-hole vias and nonplated holes. Resistors and capacitors can also be embedded into the substrate. More will be discussed about blind vias in later chapters (8 and 9).

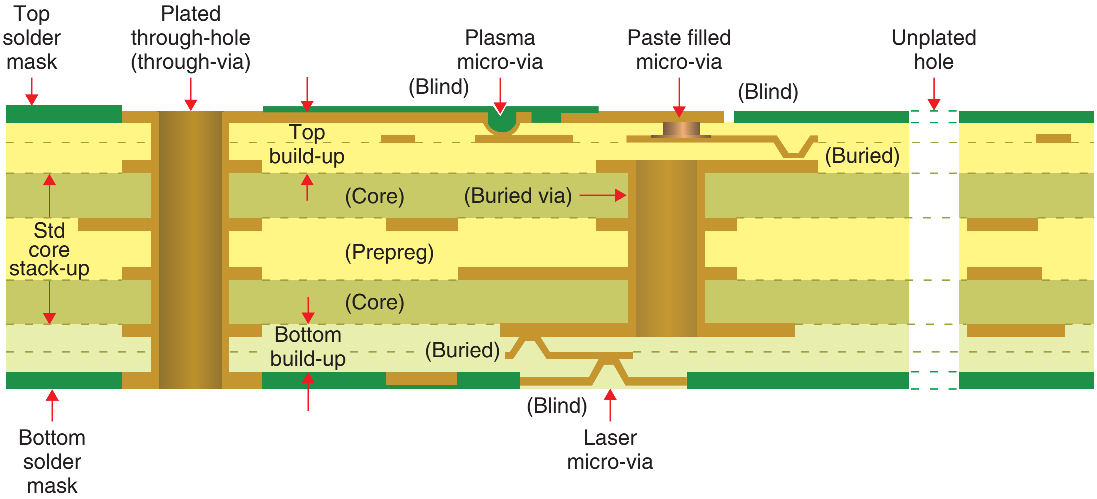

Top solder mask
Plated through-hole (through-via)
Plasma micro-via
(Blind)
Paste filled micro-via
(Blind)
Unplated hole
Top build-up
(Buried)
(Core)
(Buried via)
Std core stack-up
(Prepreg)
(Core)
Bottom build-up
(Buried)
(Blind)
Bottom solder mask
Laser micro-via

Figure 1-5 A built-up, multitechnology, PCB stack-up.

PCB fabrication process

The copper traces and pads you see on a PCB are produced by selectively removing the copper cladding and foil. There are two common methods for removing the unwanted copper: wet acid etching and mechanical milling. Acid etching is more common when manufacturing large quantities of boards because many boards can be made simultaneously. One drawback to wet etching is that the chemicals are hazardous and must be replenished occasionally, and the depleted chemicals must be recycled or discarded. Milling is usually used for smaller production runs and prototype boards. During milling, the traces and pads are formed by a rotating bit that grinds the unwanted copper from the substrate. With either method, a digital map is made of the copper patterns. The purpose of CAD software like OrCAD Layout is to generate the digital maps.

Note

- *Only one layer is considered in the following explanation of the fabrication process.*

Photolithography and chemical etching

Selectively removing the copper with etching processes requires etching the unwanted copper while protecting the wanted copper from the etchant. This protection is provided by a polymer coating (called photoresist) that is deposited onto the surface of the copper cladding as shown in Fig. 1-6. The photoresist is patterned into the shape of the desired printed circuit through a process called photolithography. The patterned resist protects selected areas of the copper from the etchant and exposes the copper to be etched.

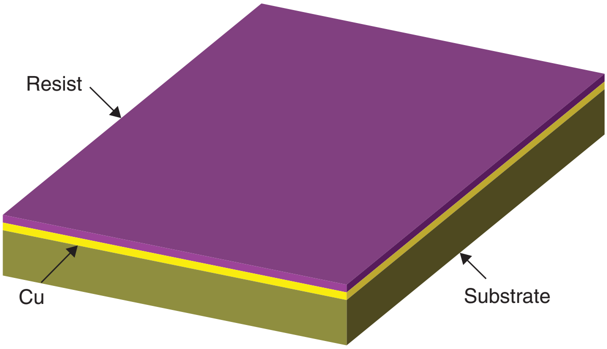


Figure 1-6 A copper clad board coated with photoresist.

There are two steps to photolithography, patterning the photoresist—exposing the resist to light (typically ultraviolet (UV) light) and developing it (selective removal in a chemical bath). There are two types of photoresist: positive resist and negative resist. When positive resist is exposed to UV light, the polymer breaks down and can be removed from the copper. Conversely, negative resist that is shielded from UV light is removed.

A mask is used to expose the desired part of the photoresist. A mask is a specialized black and white photographic film or glass photoplate on which a picture of the traces and pads is printed with a laser photoplotter. Two types of masks are shown in Fig. 1-7. The masks are examples of a trace connected to a pad. Figure 1-7(a) shows a positive mask used to expose positive photoresist, and Fig. 1-7(b) shows a negative mask used to expose negative photoresist. Masks that will be used repeatedly are sometimes produced on glass photoplates instead of film.

The mask is placed on top of the photoresist as shown in Fig. 1-8, and the assembly is exposed to the UV light. The dark areas block UV light and the white (transparent) areas allow the UV light to hit the photoresist, which imprints the circuit image into the photoresist. A separate mask is used for each layer of a circuit board. OrCAD Layout generates the data that the photoplotter uses to make these masks.

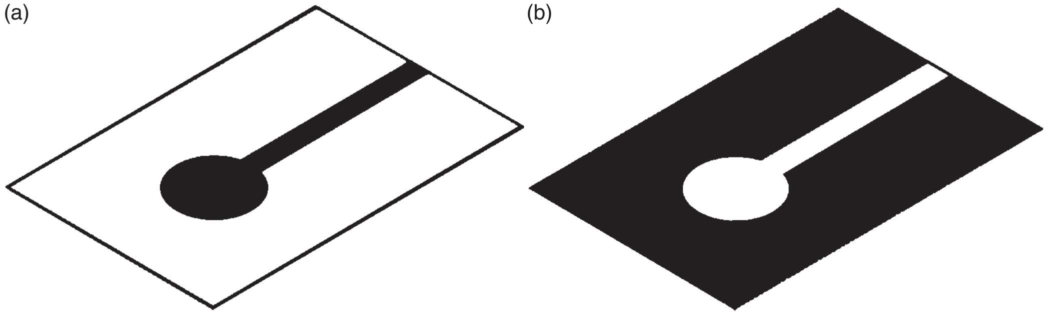


Figure 1-7 Photolithography masks. (a) A positive mask. (b) A negative mask.

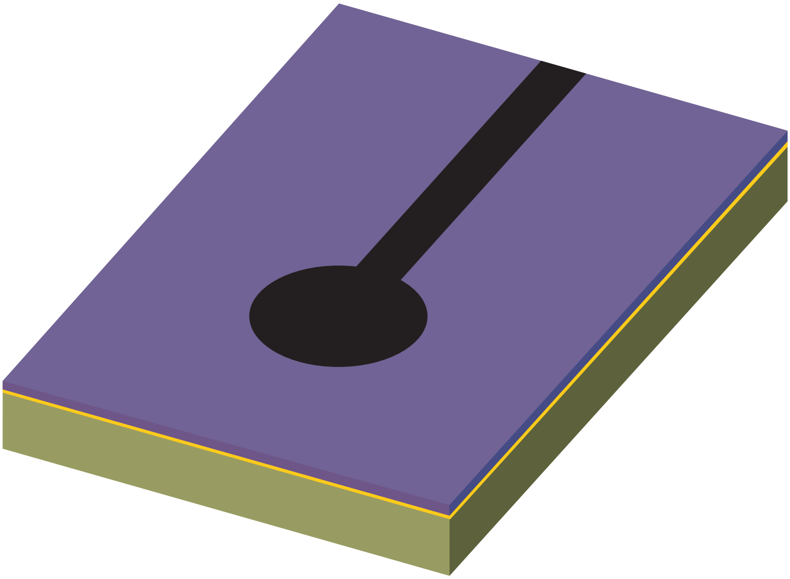


Figure 1-8 Positive photomask on photoresist-coated board.

Another way of exposing the photoresist is by using a programmable laser to “draw” the pattern directly onto the photoresist. This is a newer technique called laser direct imaging (LDI). A benefit of the LDI process is that it uses the same data as the photoplotters but no masks are required.

After the photoresist has been exposed (either with the mask and UV or with the laser) it is washed in a chemical called the developer. In the case of positive resist, the resist breaks down during exposure and is removed by the developer. In the case of negative resist, the UV light cures the resist, and only the unexposed resist is removed by the developer. Common developers are sodium hydroxide ($NaOH$) for positive resist and sodium carbonate (Na_2CO_3) for negative resist. Once the resist has been exposed and developed, a circuit image made of the photoresist is left on the copper as shown in Fig. 1-9.

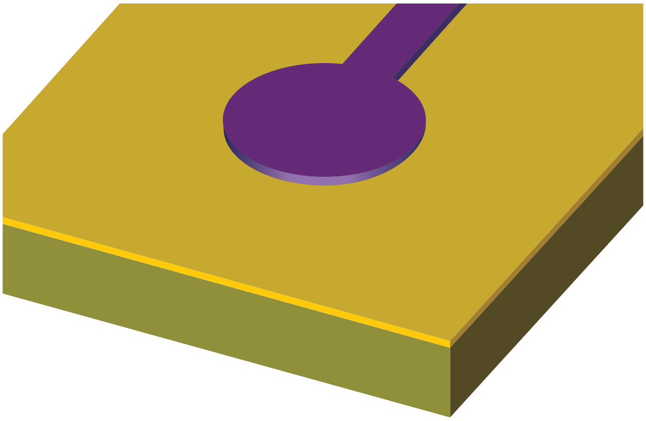


Figure 1-9 Developed photoresist on copper.

Next, the board is etched in an acid solution such as ferric chloride ($FeCl_3$) or sodium persulfate ($Na_2S_2O_8$). The etching solution does not significantly affect the photoresist but attacks the bare copper and removes it from the substrate, leaving behind the resist-coated copper as shown in Fig. 1-10.

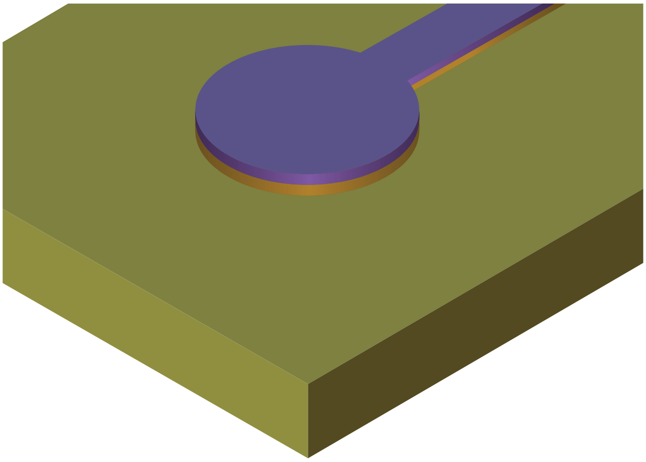


Figure 1-10 Unwanted copper removed after etching.

Some processes use a plated tin alloy as the etch resist. The tin alloy plating is more resistant to etchants and preprepares the copper surface for solder processes. In this case the photolithography processes are used to selectively plate the circuit pattern onto the copper surfaces prior to etching.

When polymer etch resists are used the photoresist is cleaned from the copper with a resist stripper, leaving behind the copper traces. Fig. 1-11 shows the final patterned copper. When

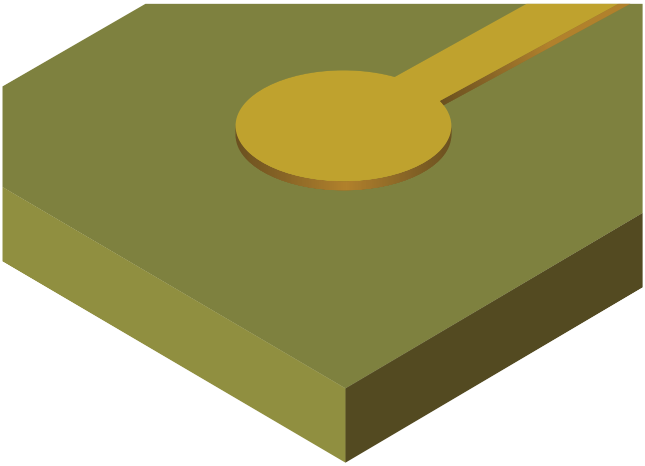


Figure 1-11 Copper pad and trace after etching and resist stripping.

metal etch resists are used the plating is typically left in place. Holes for the leads, etc., are not etched into the pads because they are drilled after all of the cores have been glued together (later in the process) to ensure proper alignment of the holes between board layers.

Mechanical milling

As mentioned above, milling is an alternative to etching. To mill the board, a computer numerical control (CNC) machine is programmed with the digital map of the board and grinds away the unwanted copper. The unwanted copper can be completely removed (like that in Fig. 1-11), or just enough copper may be removed to isolate the pads and traces from the bulk copper as shown in Fig. 1-12. Removing only enough copper to isolate the traces from the bulk copper reduces milling time but can affect the impedance of the traces.

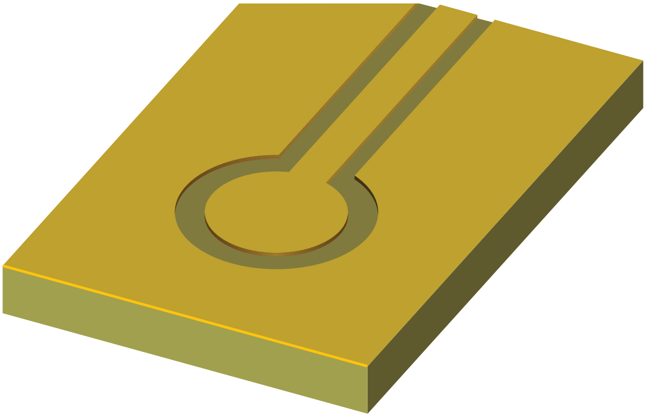


Figure 1-12 A mechanically milled trace.

Layer registration

After the inner layers have been patterned, the cores are aligned (called registration) and glued together. Registration is critical because the pads on each layer need to be properly aligned when the holes are drilled. Registration is accomplished using alignment patterns (called fiducials) and tooling holes in the board, which slide onto guide pins. With the cores in place and properly aligned, a heated press cures the assembly.

After the assembly is cured, holes are drilled for through-hole component leads and vias. The drilling process inevitably heats the laminate due to friction between the laminate and the high-speed drill bit. This tends to soften the laminate and smear it across the walls of the drilled copper. After the drilling processes are finished, the assembly is placed into a bath to etchback the laminate slightly and clean the faces of the copper pad walls. This is called laminate etchback or desmear.

Once the holes have been drilled and desmeared, a physical path exists between pads on different layers, but as Fig. 1-13(a) shows there is not an electrical connection between them. To make electrical connections between pads on different layers the board is placed into a plating bath that coats the insides of the holes with copper, which electrically connects the pads—hence the term “plated” through-holes. The plating thickness varies but is typically about 1 mil (0.001 in.) thick. The cutaway view of Fig. 1-13(b) shows a plated through-hole on an internal layer of a PCB. The top and bottom copper is actually patterned *after* the plating process is finished because the plating process would replate the areas where copper had been removed.

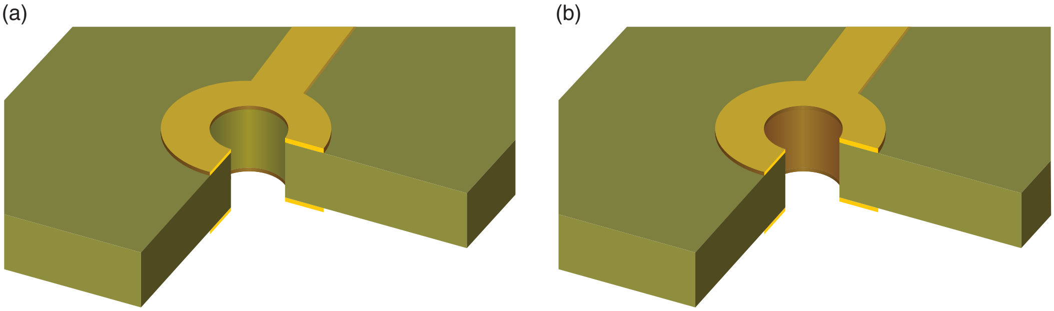


Figure 1-13 Holes are drilled into the board and then copper plated. (a) A nonplated through-hole. (b) A plated through-hole.

Not all layers have traces. Some layers are planes (see Fig. 1-14). Plane layers are typically used to provide low-impedance (resistance and inductance) connections to power and ground and to provide easy access to power and ground at any location on the board. Plane layers and impedance issues are discussed in Chap. 6. The leads of components are connected to ground or power by soldering them into plated through-holes. Since copper conducts heat well, soldering to a plane layer could require an excessive amount of heat that could damage the components or the plating in the hole (called the barrel). Thermal reliefs are used as shown in Fig. 1-14 to reduce the path for heat conduction but maintain electrical continuity with the plane.

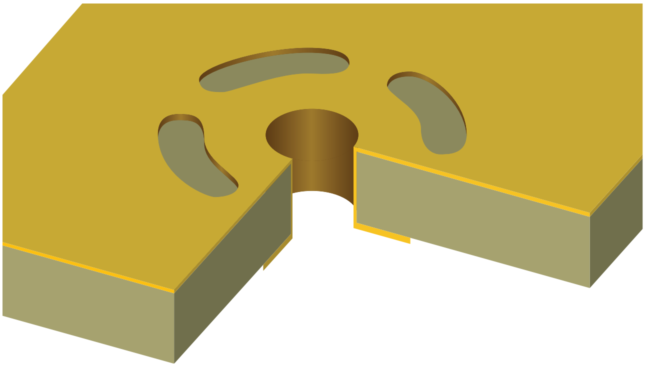


Figure 1-14 A connection to a plane layer through a thermal relief.

Since ground and power planes are often inner layers and signal layers will likely be above and below them, there will be instances in which a via will run through a plane layer but must not touch it. In this case a “clearance” area (shown in Fig. 1-15) is etched into the plane layer around the via to prevent a connection to the plane. The clearance is usually larger than the normal pad size to ensure that the plane stays isolated from the plated hole.

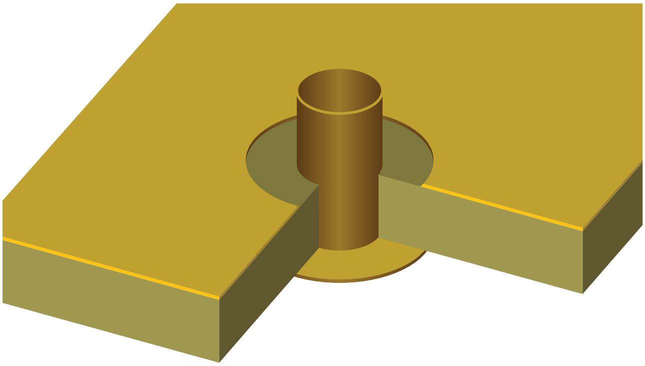


Figure 1-15 A clearance area provides isolation between a plated hole and a plane.

After the through-holes are plated, the top and bottom layers are patterned using the photolithography process as described for the inner layers. After the outer copper has been patterned, the exposed traces and plated through-holes can be tinned (although tinning is sometimes deferred until later). Nonplated holes (such as for mounting holes) may be drilled at this time.

Next, a thin polymer layer is usually applied to the top and bottom of the board. This layer (shown in green in Fig. 1-16) is called the soldermask or solder resist. Holes are opened into the polymer using photolithography to expose the pads and holes where components will be soldered to the board. The soldermask protects the top and bottom copper from oxidation and helps prevent solder bridges from forming between closely spaced pads. Sometimes openings in the soldermask are not made over small or densely placed vias (called tenting a via). Tented vias are protected from having chemicals such as flux from becoming trapped inside the hole. Tenting also prevents solder migration into the hole, which could lead to poor solder joints on small components that are close to and connected to the via.

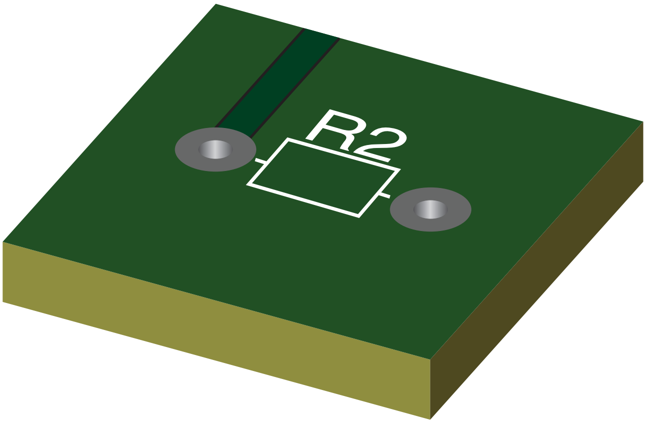


Figure 1-16 Final layers are the soldermask (green) and silk screen (white).

Finally, markings (called the silk screen) are placed on the board to identify where components are to be placed. The silk screen is shown in white in Fig. 1-16.

Function of OrCAD Layout in the PCB Design Process

Layout is used to design the PCB by generating a digital description of the board layers for photoplotters and CNC machines, which are used to manufacture the boards. There are separate layers for routing copper traces on the top, bottom, and all inner layers; drill hole sizes and locations; soldermasks; silk screens; solder paste; part placement; and board dimensions. These layers are not all portrayed identically in Layout. Some of the layers are shown from a positive perspective, meaning what you see with the software is what is *placed onto* the board, while other layers are shown from a negative perspective, meaning what you see with the software is what is *removed from* the board. The layers represented in the positive view are the board outline, routed copper, silk screens, solder paste, and assembly instructions. The layers represented in the negative view are copper plane layers, drill holes, and soldermasks. Figure 1-17 shows routed layers (top and bottom and inner for example) that Layout shows in the positive perspective. The background is black and the traces and pads on each layer are a different color to make it easier to keep track of visually. The drill holes are shown on a dedicated drill layer because, as mentioned above, the drilling process is a distinct step that is performed at a specific time during the manufacturing process.

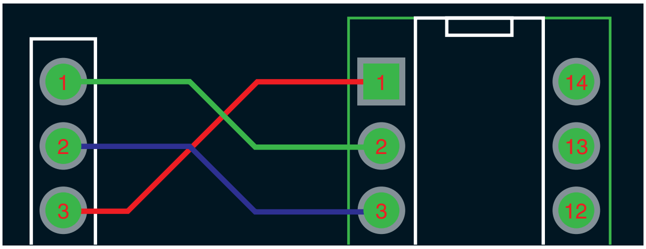


Figure 1-17 Copper in routed layers (positive view).

Figures 1-18(a) and 1-18(b) show the difference between a physical copper plane layer with a thermal via and the negative representation used by Layout. In this view the black background is actually the copper plane, and the yellow areas indicate were the copper is removed. As with the routed layers, the drill holes are visible on the drill layer.

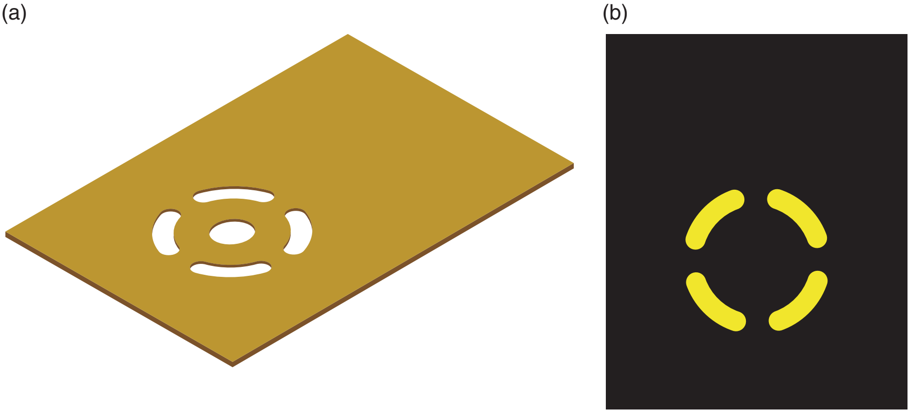


Figure 1-18 Copper in a plane layer (negative view without drill info). (a) Copper plane with thermal relief. (b) Negative view in Layout.

Figure 1-19(a) shows the soldermask with the patterned holes that allow access to pads, and Fig. 1-19(b) shows the negative representation used by Layout. Here, as with the negative perspective of the ground plane, the black background is actually the polymer film and the green circles are the holes in the soldermask.

Finally, Fig. 1-20 shows examples of drill patterns and silk-screen representations used by Layout (traces not shown). The dark red circles are the locations and sizes of the drill holes (a negative view) and the brighter red symbols are used in conjunction with a drill chart (see Fig. 1-21) to give ID numbers for the different drill tools. The white print is the silk screen discussed above.

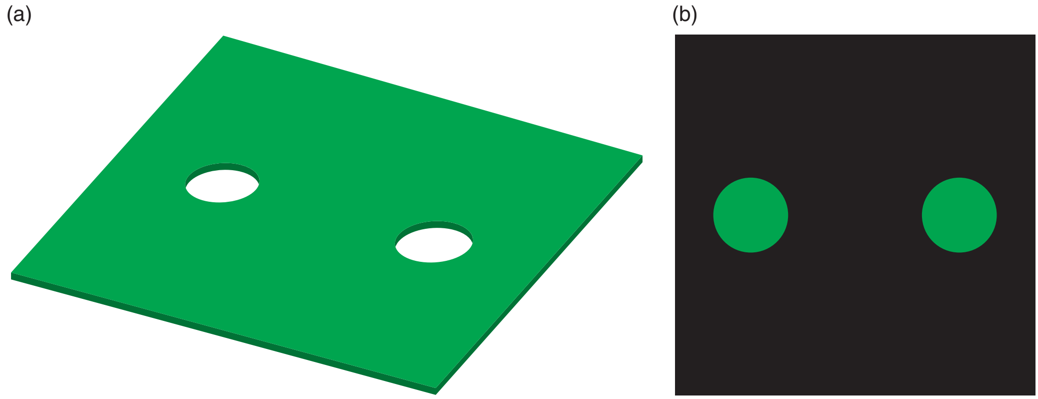


Figure 1-19 Soldermask layer and negative view. (a) Soldermask. (b) Negative view in Layout.

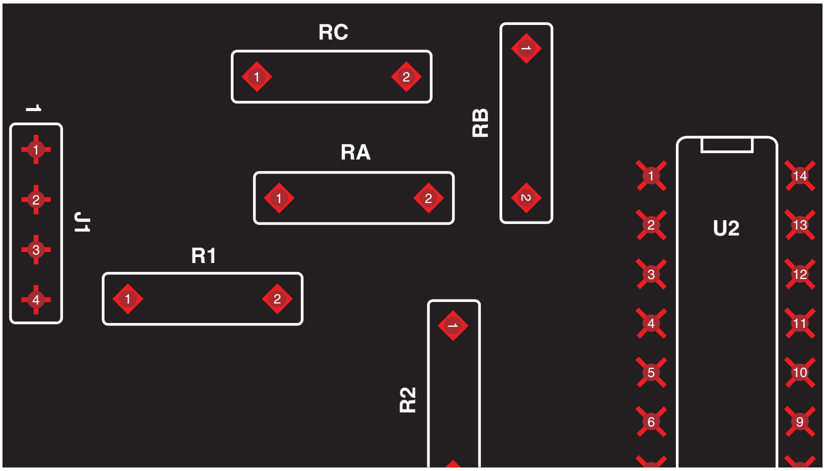
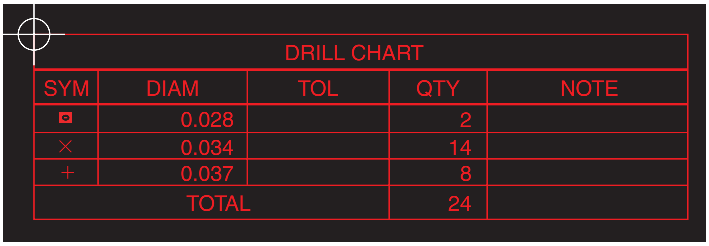

RC
1
2
RB
1
2
1
J1
1
2
3
4
RA
1
2
R1
1
2
U2
1
2
3
4
5
6
14
13
12
11
10
9
R2
1

Figure 1-20 Circuit layout with drill identifiers and silk screen on a PCB.



DRILL CHART

SYM	DIAM	TOL	QTY	NOTE
▣	0.028		2	
×	0.034		14	
+	0.037		8	
TOTAL			24	

Figure 1-21 Drill chart with drill IDs and specifications.

Design Files Created by Layout

Layout format files (.MAX)

When you are designing your board, Layout works with and saves your design in a format that is efficient for your computer. The Layout design file has a .MAX extension. When you are ready to fabricate your board, Layout postprocesses the design and converts it into a format that the photoplotters and CNC machines can use. These files are called Gerber files.

Postprocess (Gerber) files

Postprocessing creates a separate Gerber file for each of the layers discussed above. There can be as many as 30 or so different layer files that Layout generates to describe various manufacturing aspects of your PCB. Some examples of these files, their extensions, and their functions are listed in Table 1-1. These and other files that Layout generates will be discussed in greater detail in the next two chapters.

File name and extension	Function
BoardName .AST	Top side assembly
BoardName .SPT	Top side solder paste
BoardName .SST	Top side silk screen
BoardName .SMT	Top side soldermask
BoardName .TOP`	Top side copper (usually routing)
BoardName .IN1	Inner layer 1 (routing or plane)
BoardName .IN2	Inner layer 2 (routing or plane)
BoardName .Inx	Inner layer x (routing or plane)
BoardName .PWR	Power layer (a plane layer)
BoardName .GND	Ground layer (a plane layer)
BoardName .BOT	Bottom side copper (usually routing)
BoardName .SMB	Bottom side soldermask
BoardName .SSB	Bottom side silk screen
BoardName .SPB	Bottom side solder paste
BoardName .ASB	Bottom side assembly
BoardName .DRD	Board outline info
Throughhole .tap	Drill information

Table 1-1 Gerber (layer) files generated by layout

PCB assembly layers and files

There are several layer files generated by Layout that are not part of the actual fabrication process. These files are used for automated assembly of a finished board and are mentioned only briefly here. The first layer is the solder-paste layer. It is used to make a contact mask for selectively applying solder paste onto the PCB's pads so that components can be reflow soldered to the board. There may be a solder-paste layer for the top side of the board (.SPT) and one for the bottom side (.SPB) as shown in Table 1-1. The second layer file is the assembly layer, which contains information for automatic component placement machines (pick-and-place machines) as to the part type, its position, and its orientation on the board. As with the soldermask, there may be an assembly layer for the top side of the board (.AST) and one for the bottom side (.ASB). PCB design for the various soldering and assembly processes is discussed in Chap. 5.

The purpose of this chapter has been to introduce you to the process by which PCBs are manufactured. The purpose of the next chapter is to show you how to use OrCAD Layout to design your board and generate the files needed to manufacture your PCB.

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CHAPTER 2

Introduction to the PCB Design Flow by Example

Now that we have covered the construction of a PCB and know Layout's role in it, we will go through a simple design example so that you get a feel for the overall design process. This simple example sets the stage for Chap. 3, in which we will dig deeper into the details of the process and learn more about Layout itself, and Chap. 9, in which PCB design examples are presented.

Overview of the Design Flow

This section illustrates the basic procedure for generating a schematic in Capture and converting the schematic to a board design in Layout. The basic procedure is as follows:

1. Start Capture and set up a PCB project using the PC Board wizard.
2. Make a circuit schematic using OrCAD Capture.
3. Use Capture to generate a Layout netlist and save it as a .MNL file for Layout.
4. Start Layout and select a PCB technology template (.TCH file).
5. Save the Layout project as a .MAX project file.
6. Use Layout to import the .MNL netlist into the .MAX file.
7. Make a board outline.
8. Position the parts within the board outline.
9. Autoroute the board.
10. Run the postprocessor to generate files used to manufacture the PCB.

Creating a Circuit Design with Capture

If you do not have a full version of OrCAD you can install the version 10.5 Demo CD included with this book or go to the OrCAD Web site and download the latest demo. If you are using an older version of Layout most of the following information in this book still applies, but some of the dialog boxes and menu items may be different.

Starting a new project

Before you make a PCB layout, you need to have a circuit to lay out. You will use Capture to make the schematic, so the first step is to start the Capture application by clicking the

Windows Start button on your task bar and navigate to All Programs → OrCAD 10.5 Demo → Capture CIS Demo. Once Capture is running, you should have a blank Capture session frame and a session log. Go to the File dropdown menu and navigate to File → New and click Project as shown in Fig. 2-1.

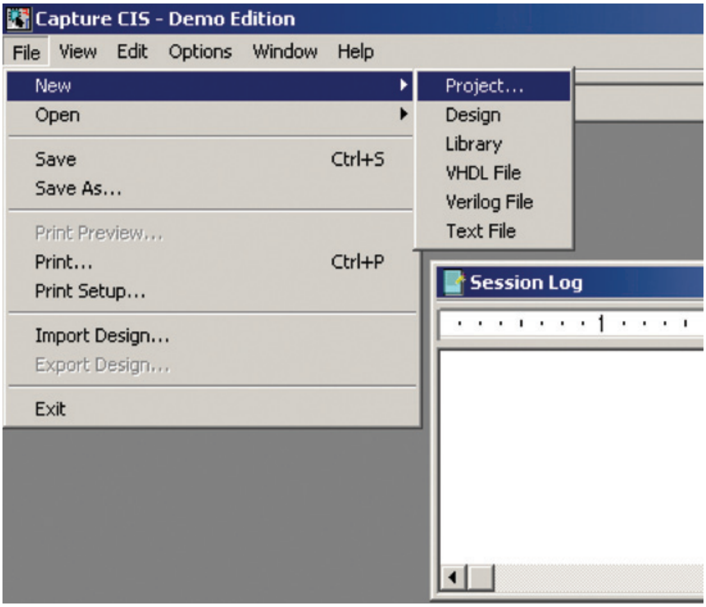

Capture CIS - Demo Edition
File
View
Edit
Options
Window
Help
New
Open
Save Ctrl+S
Save As...
Print Preview...
Print... Ctrl+P
Print Setup...
Import Design...
Export Design...
Exit
Project...
Design
Library
VHDL File
Verilog File
Text File
Session Log

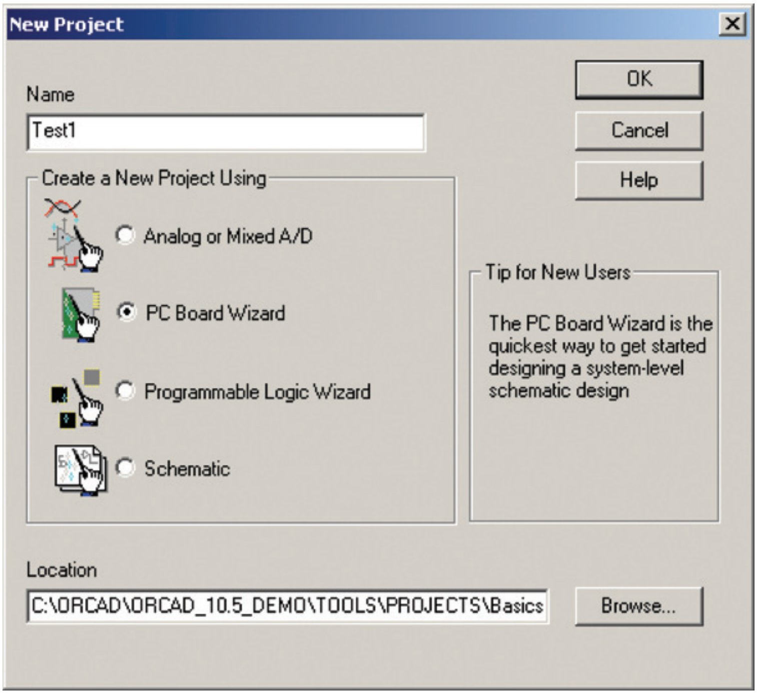
Figure 2-1 Starting a new project in Capture.

The New Project dialog box in Fig. 2-2 will pop up. Type a name for your project, and then select the PC Board Wizard radio button. If you feel comfortable selecting your own location to save the project, you can do that, or you can use the default location for now (just remember where it is as you will need to find it later on with Layout). Click OK.

After you click OK, the PCB Project Wizard dialog box shown in Fig. 2-3(a) will pop up. For now circuit simulation will not be performed, so leave the Enable project simulation box unchecked (we will take a look at circuit simulation in Chap. 9). Click Next.

After you click Next, the PCB Project Wizard dialog box shown in Fig. 2-3(b) will pop up. This box allows you to add specific libraries to your project. Scroll down until you find the Discrete.olb library, highlight it by clicking on it, and then click the Add>> button; then click Finish. This completes the project set up.

You should have a Project Manager window in the left side of the Capture session frame as shown in Fig. 2-4. You may also have a Schematic window in the work space. If the schematic is not open, expand the *projectname*.dsn directory by clicking the "+" box that is to the left of the *projectname*.dsn icon (where *projectname* is the name you gave your project while using the project setup wizard). Click the "+" box next to the Schematics folder, and



Name

Test1

Create a New Project Using

○ Analog or Mixed A/D

● PC Board Wizard

○ Programmable Logic Wizard

○ Schematic

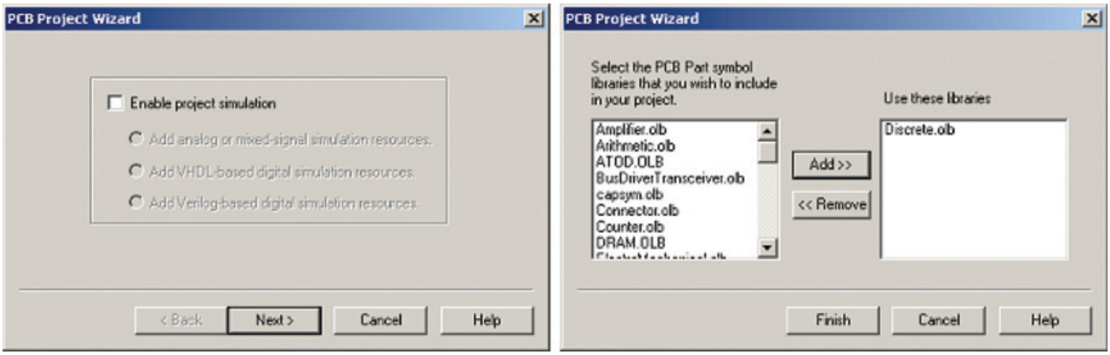
Tip for New Users

The PC Board Wizard is the quickest way to get started designing a system-level schematic design

Location

C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\Basics

Figure 2-2 ***New Project*** *dialog box.*



(a)

☐ Enable project simulation

○ Add analog or mixed-signal simulation resources.

○ Add VHDL-based digital simulation resources.

○ Add Verilog-based digital simulation resources.

(b)

Select the PCB Part symbol libraries that you wish to include in your project.

Amplifier.olb
Arithmetic.olb
ATOD.OLB
BusDriverTransceiver.olb
capsym.olb
Connector.olb
Counter.olb
DRAM.OLB

Use these libraries

Discrete.olb

Figure 2-3 PCB ***Project Wizard*** *dialog boxes. (a) Simulation selection. (b) Parts library selection.*

then double click the file called Page1. The Schematic page should open. If you do not see the dots, that means your grid is turned off. **The grid must be turned on to properly place and connect parts**. **To turn the grid on** click the button. If the grid is on, the grid dots will be visible and the grid button will be gray instead of red.

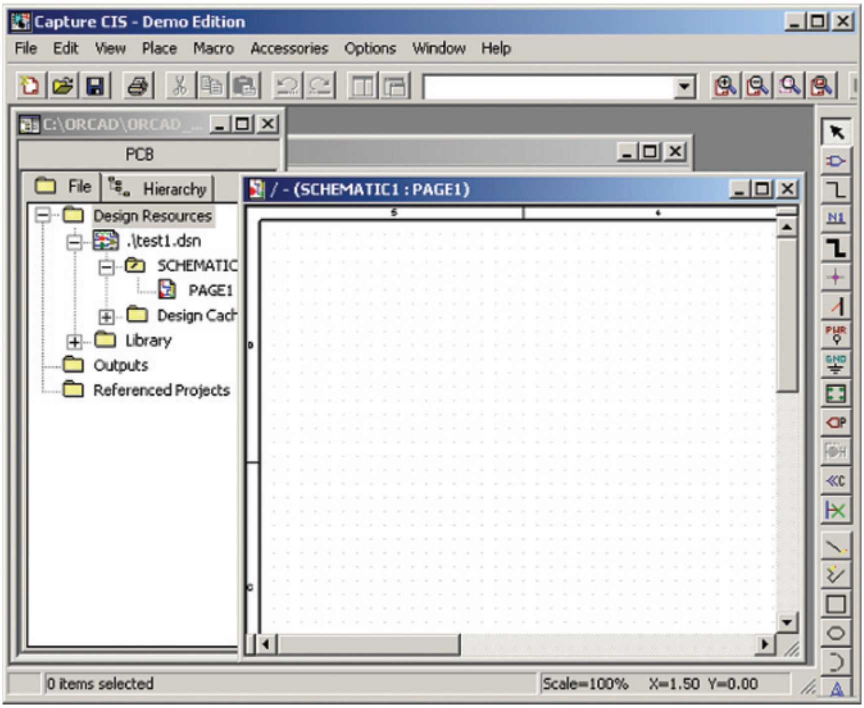

Capture CIS - Demo Edition
File
Edit
View
Place
Macro
Accessories
Options
Window
Help
C:\ORCAD\ORCAD_...
PCB
File
Hierarchy
Design Resources
.\test1.dsn
SCHEMATIC
PAGE1
Design Cach
Library
Outputs
Referenced Projects
/ - (SCHEMATIC1 : PAGE1)
0 items selected
Scale=100%
X=1.50 Y=0.00

Figure 2-4 Example view of a new project.

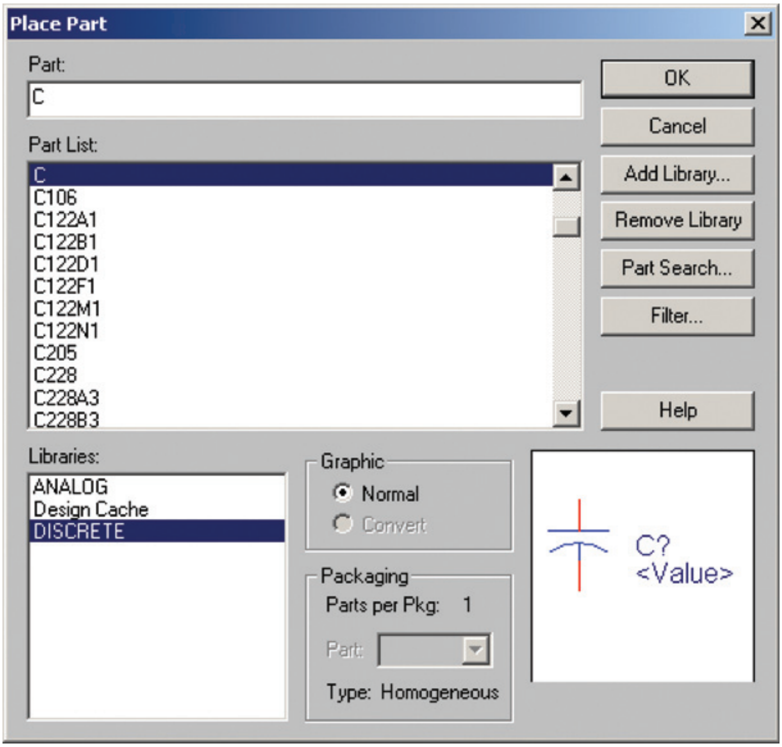
Note

- *The menu bar at the top of the Capture session frame changes depending on whether you are working with the Project Manager window or the Schematic Page window. If you need to access options or tools for the Project Manager (or Schematic page) you need to have that window active. To make the desired window active click on its title bar, or select the desired window from the* ***Window*** *menu. When it is inactive it will be gray, and when it is active it will be blue (or whatever colors you have set up in Windows). Also, for projects that have PSpice simulation capabilities, there is an additional toolbar displayed, which is not shown in Fig. 2-4.*

Placing parts

To add parts to your schematic, make the Schematic page active and select Place from the Part dropdown menu, or press the place part tool button, or press P on your keyboard. The Place Part dialog box shown in Fig. 2-5 pops up. In the Libraries selection box in the bottom left of the dialog box, click DISCRETE. Then in the Part List box click C (for capacitor). You should see its symbol in the Preview window on the lower right. Click OK. In the Libraries window you may have libraries different from what is shown in Fig. 2-5. At the very least you should have the DISCRETE library since you had the wizard include it. If for some reason you do not see any parts or the DISCRETE library is not there, you can follow along for now to get an overview of the process, or you can find and add the library to your project.

To add a part library to your project select Place from the Part dropdown menu as described above. In the Place Part dialog box shown in Fig. 2-5 press the Add Library… button to bring up the Browse File dialog box shown in Fig. 2-6. Find and select the Discrete.olb library and click Open. You can also find a capacitor in the pspice library folder. To add it, double click the pspice folder, select the Analog.olb library, and click Open. You should now be back to the Place Part dialog box, and the library you just added should be shown in the Libraries list box. Find and select C from the Part List selection box and click OK.



Place Part

Part: C

Part List:
C
C106
C122A1
C122B1
C122D1
C122F1
C122M1
C122N1
C205
C228
C228A3
C228B3

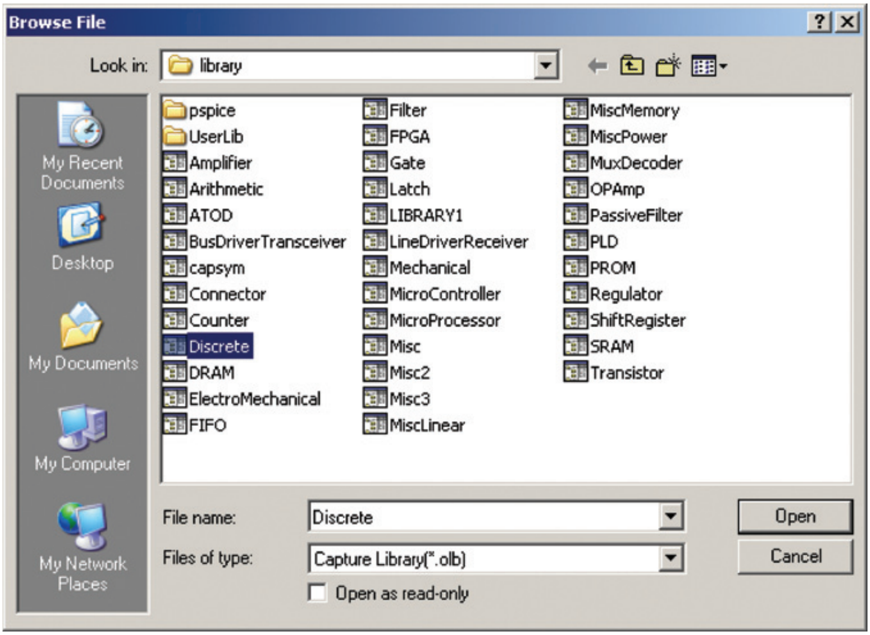
Libraries:
ANALOG
Design Cache
DISCRETE

Graphic
● Normal
○ Convert

Packaging
Parts per Pkg: 1
Part:
Type: Homogeneous

Figure 2-5 *Place Part* dialog box.

After you click OK, you should immediately return to the Schematic page and have a capacitor tagging along with your mouse pointer. Left click on the Schematic page **to place a part** as shown in Fig. 2-7. Place a couple of the capacitors on the page. When you are finished, hit the ESC key or right click the mouse and select End Mode from the pop-up menu.



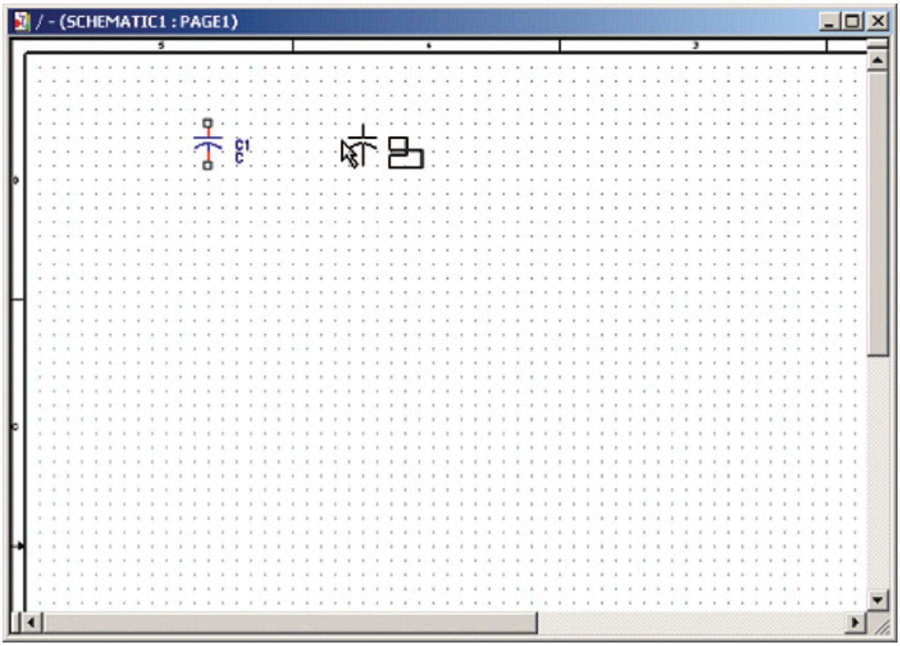
Look in: library

File name: Discrete

Files of type: Capture Library(*.olb)

Browse File
?
My Recent Documents
Desktop
My Documents
My Computer
My Network Places
pspice
UserLib
Amplifier
Arithmetic
ATOD
BusDriverTransceiver
capsym
Connector
Counter
Discrete
DRAM
ElectroMechanical
FIFO
Filter
FPGA
Gate
Latch
LIBRARY1
LineDriverReceiver
Mechanical
MicroController
MicroProcessor
Misc
Misc2
Misc3
MiscLinear
MiscMemory
MiscPower
MuxDecoder
OPAmp
PassiveFilter
PLD
PROM
Regulator
ShiftRegister
SRAM
Transistor
Open
Cancel
☐ Open as read-only

Figure 2-6 Add a library using the **Browse File** dialog box.



/ - (SCHEMATIC1 : PAGE1)
C1
C

Figure 2-7 Placing the parts.

Wiring (connecting) the parts

Next, connect the parts with wires. **To place wires** hit the W key, or select Place → Wire from the Place dropdown menu, or press the Place Wire tool button, . The cursor will turn into a cross hair. Place the cursor on a box at the end of one of the capacitor's leads and left click to start a wire (see Fig. 2-8). Click on the end of another capacitor lead to complete that wire. The cross hair will persist so you can continue placing wires. Finish connecting wires to the capacitors however you wish. Once you have finished connecting the circuit press the ESC key or right click and select End Wire to stop the place wire cursor and get the pointer back. If you inadvertently click near a lead but not on it, the wire may appear to be connected but may not be (that is why it is important to have the grid enabled). If the connections are not made properly, you will have problems when attempting to generate a netlist. You will be able to tell if a connection you made to a component was completed properly because the box at the end of the lead will disappear. At this point do not worry about power supplies or ground connections; this is just a "big picture" exercise to demonstrate the design flow process.

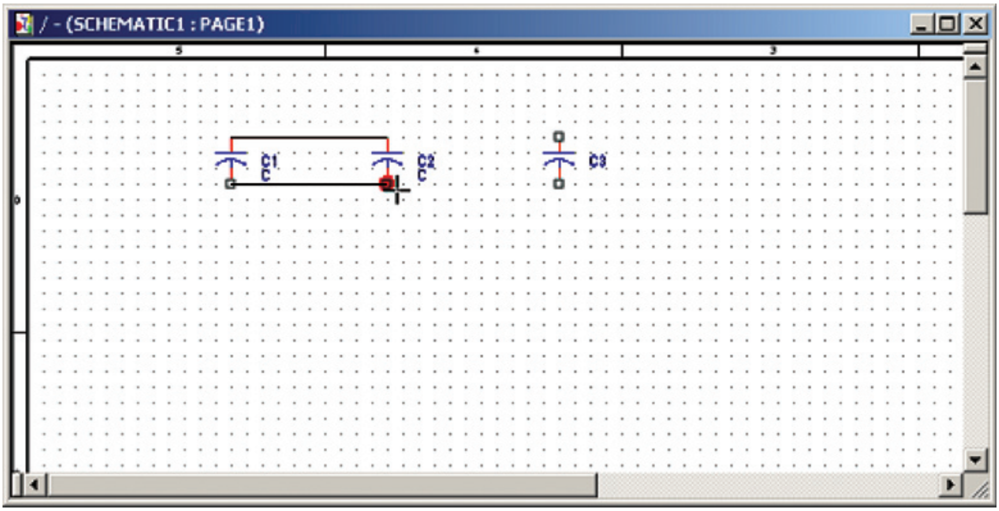


Figure 2-8 Placing wires to connect the components.

Creating the Layout netlist in Capture

Once all of the connections are complete the next step is to create a netlist (an ASCII text file that describes the circuit). There are several types of netlists, but you will want **to generate a Layout netlist**. Begin by making the Project Manager window active (instead of the Schematic Page window) and select the .dsn icon by left clicking it once. If the Schematic page is active the Tools menu will not be available. Minimize the Schematic page if necessary to get to the Project Manager. As shown in Fig. 2-9, select Tools → Create Netlist from the Tools menu. The Create Netlist dialog box will pop up as shown in Fig. 2-10.

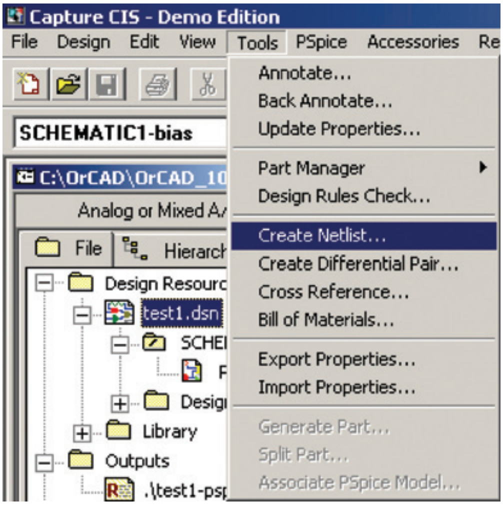
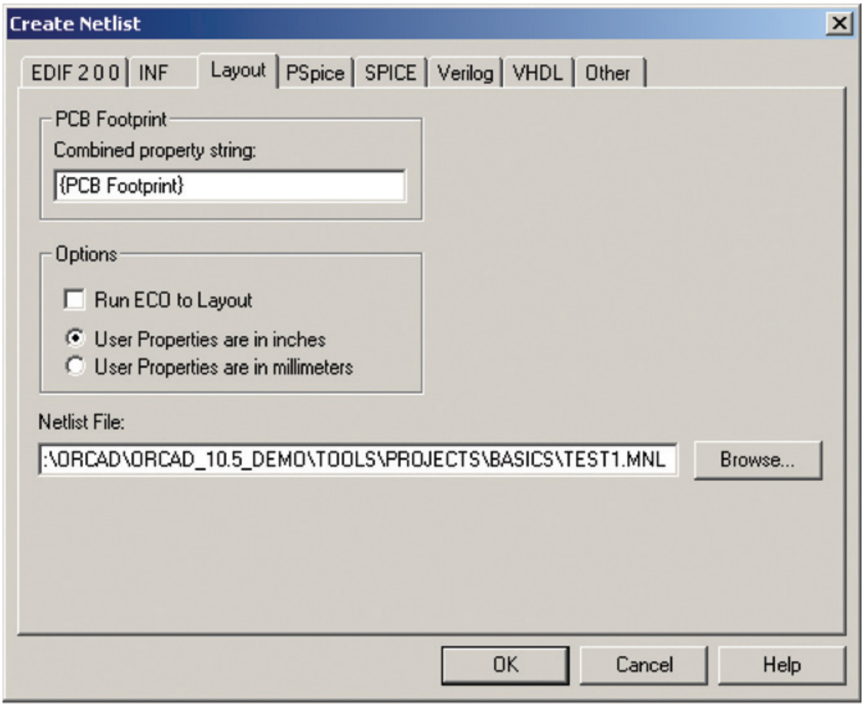

Capture CIS - Demo Edition
File
Design
Edit
View
Tools
PSpice
Accessories
Re
SCHEMATIC1-bias
C:\OrCAD\OrCAD_10
Analog or Mixed A
File
Hierarch
Design Resourc
test1.dsn
SCHE
F
Desig
Library
Outputs
.\test1-psp
Annotate...
Back Annotate...
Update Properties...
Part Manager
Design Rules Check...
Create Netlist...
Create Differential Pair...
Cross Reference...
Bill of Materials...
Export Properties...
Import Properties...
Generate Part...
Split Part...
Associate PSpice Model...

Figure 2-9 Create the Layout netlist.


Create Netlist
EDIF 2 0 0
INF
Layout
PSpice
SPICE
Verilog
VHDL
Other
Browse...
OK
Cancel
Help

PCB Footprint

Combined property string: {PCB Footprint}

Options

☐ Run ECO to Layout

● User Properties are in inches

○ User Properties are in millimeters

Netlist File: :\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\BASICS\TEST1.MNL

Figure 2-10 ***Create Netlist*** *dialog box.*

From the Create Netlist dialog box, select the Layout tab. Later, you will see how to set up file structures to organize your projects, but for now just save it to the current (default) directory and remember where the netlist file (with the .MNL extension) is saved. Leave the Run ECO to Layout radio button unchecked for now. You will use the ECO (engineering change order) tool in Chap. 9. Click Finish to generate the netlist.

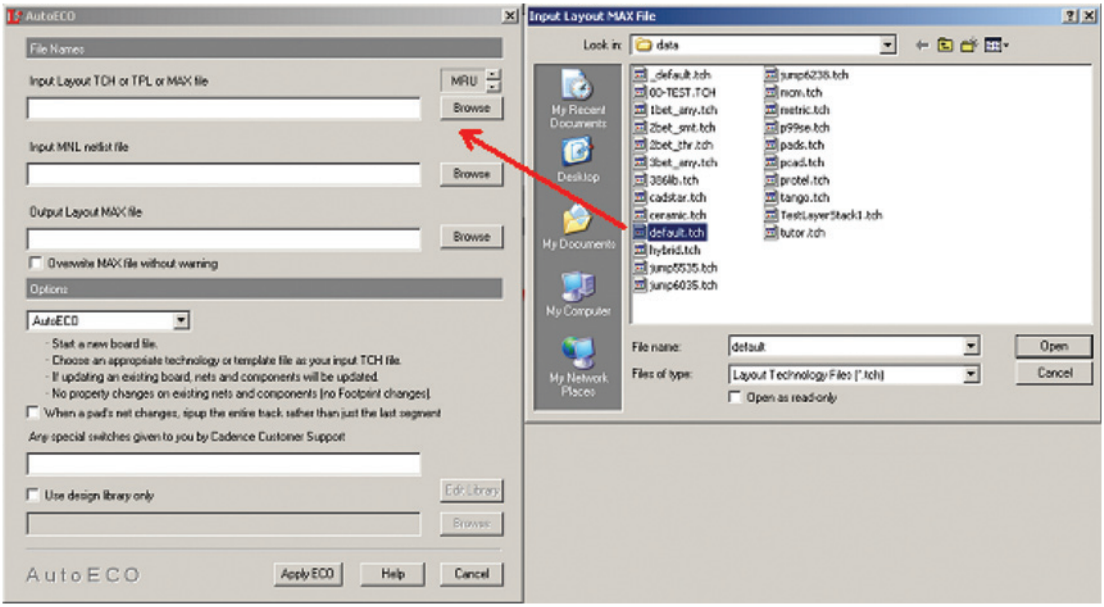
Capture will display a warning text box stating, "Design *Path/Yourname*.dsn will be saved prior to netlisting." Click OK. Capture will then generate the netlist and report the results in the Session log. At this point you have generated a netlist file with a .MNL extension that Layout can use. You could close Capture now, but leave it open so that Capture and Layout can communicate with each other if necessary. This will allow you to go back and review the circuit if you need to when you are working in Layout.

Designing the PCB with Layout

Starting Layout and importing the netlist

Now you will use the netlist to route a board using Layout. Begin by clicking the Windows Start button on your task bar and navigate to All Programs → OrCAD 10.5 Demo → Layout Demo.

Once Layout is up and running, you will be presented with a blank session frame initially. To begin working on your board you need to tell Layout what kind of board you want to use and then import the netlist file you generated with Capture into that board type. Begin by selecting New from the session frame's File menu. An AutoECO (automatic engineering change order) dialog box will pop up as shown in Fig. 2-11. There are three pieces of information that


AutoECO
File Names
Input Layout TCH or TPL or MAX file
MRU
Browse
Input MNL netlist file
Browse
Output Layout MAX file
Browse
Overwrite MAX file without warning
Options
When a pad's net changes, ripup the entire track rather than just the last segment
Any special switches given to you by Cadence Customer Support
Use design library only
Edit Library
Browse
AutoECO
Apply ECO
Help
Cancel
Input Layout MAX File
Look in:
My Recent Documents
Desktop
My Documents
My Computer
My Network Places
_default.tch
00-TEST.TCH
1bet_any.tch
2bet_smt.tch
2bet_thr.tch
3bet_any.tch
386lib.tch
cadstar.tch
ceramic.tch
default.tch
hybrid.tch
jump5535.tch
jump6035.tch
jump6238.tch
mom.tch
metric.tch
p99se.tch
pads.tch
pcad.tch
protel.tch
tango.tch
TestLayerStack1.tch
tutor.tch
File name:
Files of type:
Open as read-only
Open
Cancel

Options: AutoECO
- Start a new board file.
- Choose an appropriate technology or template file as your input TCH file.
- If updating an existing board, nets and components will be updated.
- No property changes on existing nets and components (no Footprint changes).

Look in: data

File name: default

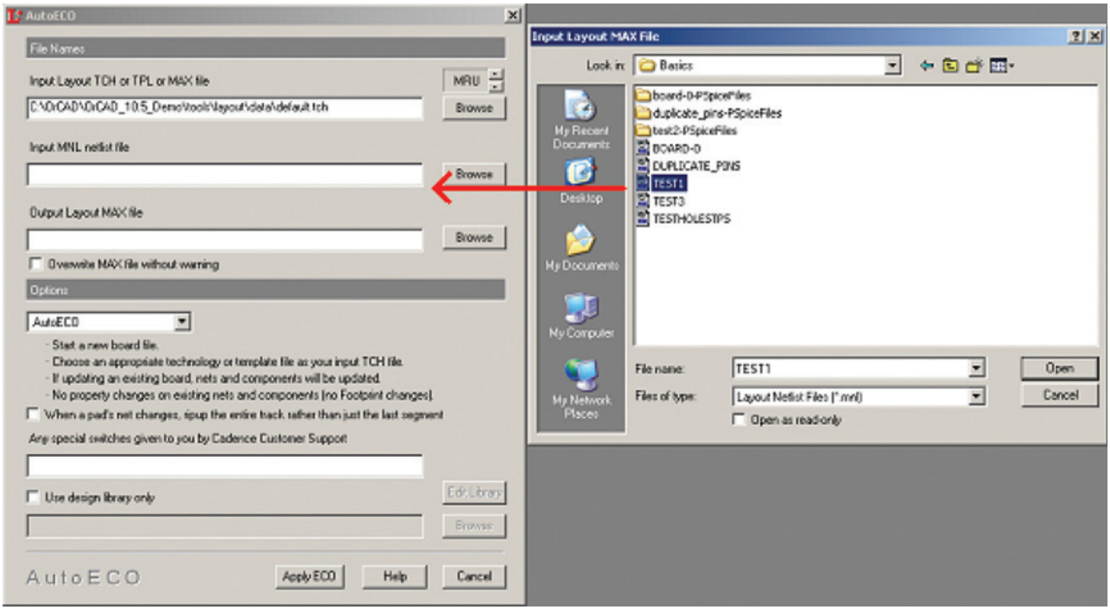
Files of type: Layout Technology Files (*.tch)

Figure 2-11 Assigning a PCB technology file.

need to be entered into the AutoECO dialog box. You will add the first two pieces of information in the TCH and the MNL text boxes, and Layout will enter a default value into the third (MAX) text box.

The first step is **to select a board technology template** (a *.TCH file). Click the Browse button across from the TCH text box and navigate to the Tools/Layout/Data folder (Layout should go there automatically) and select the default technology template (default.tch) as shown in Fig. 2-11. We will use some of the other technology files in Chap. 9. Click Open. The wizard will type the path and name of the technology file into the text box for you.

Once the technology file is assigned, you need **to select the Layout netlist (.MNL) file** you generated in Capture. To do so, click the Browse button across from the MNL text box and locate the .MNL file you created in Capture (Fig. 2-12). You probably will not see it at first since you will likely be in the Data folder from which you selected the technology file. Navigate to where you saved the project. Once you find your file, select it and click Open. The wizard will type the path and name of the netlist file into the text box for you.



Input Layout TCH or TPL or MAX file: C:\OrCAD\OrCAD_10.5_Demo\tools\layout\data\default.tch

Input MNL netlist file

Output Layout MAX file

☐ Overwrite MAX file without warning

AutoECO
- Start a new board file.
- Choose an appropriate technology or template file as your input TCH file.
- If updating an existing board, nets and components will be updated.
- No property changes on existing nets and components (no Footprint changes).

☐ When a pad's net changes, ripup the entire track rather than just the last segment

Any special switches given to you by Cadence Customer Support

☐ Use design library only

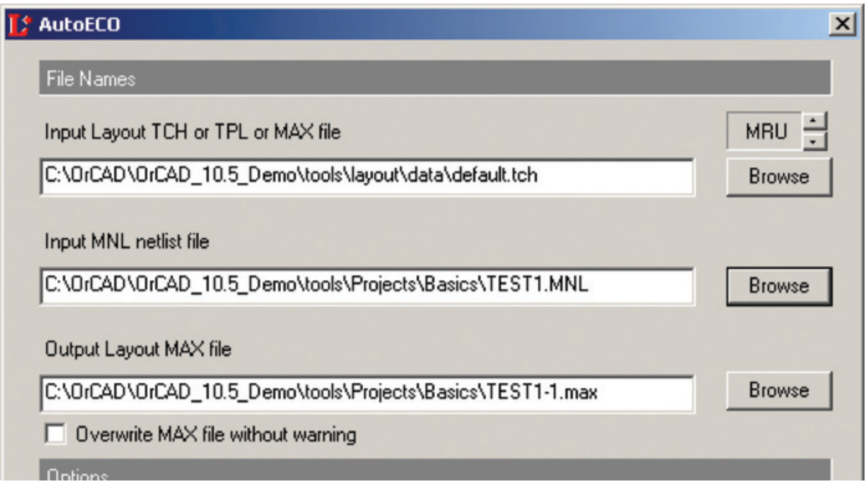
Look in: Basics

board-0-PSpiceFiles
duplicate_pins-PSpiceFiles
test2-PSpiceFiles
BOARD-0
DUPLICATE_PINS
TEST1
TEST3
TESTHOLESTPS

File name: TEST1
Files of type: Layout Netlist Files (*.mnl)
☐ Open as read-only

Figure 2-12 Opening the netlist.

Once you have entered these first two pieces of information, the wizard will fill in the MAX file information for you with a default name as shown in Fig. 2-13. The MAX file is Layout's project file that contains the information needed to build your board. You can use the default name (recommended for now) or save it with a different name. Click the Apply ECO button at the bottom of the dialog box. You do not need to make any changes to the Options settings at this point. Layout will immediately go about setting up the project environment.


AutoECO
File Names
MRU
Browse
Browse
Browse
Options

Input Layout TCH or TPL or MAX file
C:\OrCAD\OrCAD_10.5_Demo\tools\layout\data\default.tch

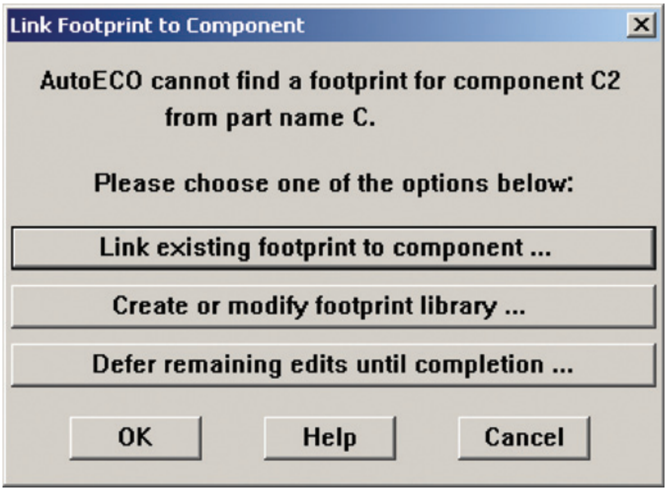
Input MNL netlist file
C:\OrCAD\OrCAD_10.5_Demo\tools\Projects\Basics\TEST1.MNL

Output Layout MAX file
C:\OrCAD\OrCAD_10.5_Demo\tools\Projects\Basics\TEST1-1.max

☐ Overwrite MAX file without warning

Figure 2-13 Save the MAX Layout file.

When setting up the project Layout checks for footprint assignments for each part in the netlist. If no footprint was assigned, or if a footprint that Layout does not know about is assigned to a part, Layout will ask you to choose a footprint with the Link Footprint to Component dialog box shown in Fig. 2-14. Most likely this will be the case since no footprints were assigned to these parts in Capture (you will see how to do that in Chaps. 3 and 9). If you get the Link Footprint dialog box, click on the Link existing footprint to component button.


Link Footprint to Component
Link existing footprint to component ...
Create or modify footprint library ...
Defer remaining edits until completion ...
OK
Help
Cancel

AutoECO cannot find a footprint for component C2 from part name C.

Please choose one of the options below:

Figure 2-14 The AutoECO ***Link Footprint to Component*** *dialog box.*

Layout will initiate the Footprint Library utility shown in Fig. 2-15. Depending on how (or if) Layout has been used before, you may have libraries different from those shown in the figure. If you are using the Demo version, you should, at the very least, have the Ex_gui library; which you should select. In the Footprints box below the Libraries box, find the SIP/TM/L.200/2 footprint. If you are using the full version find and select the TM_AXIAL.LLB and select a footprint that has two pads. A picture of the footprint will be displayed in the Preview window on the right of the dialog box. In Chap. 8 you will see how to add other libraries and footprints and also how to make our own footprints if the one you need does not exist. For now click OK once you have selected a footprint. Layout will assign this footprint to all of the capacitors in the design by default. If you added other components in addition to the capacitors, you will probably have to repeat this procedure for each type of component. Right now it is not important what the footprint is because we just want to get an overview of the overall process.

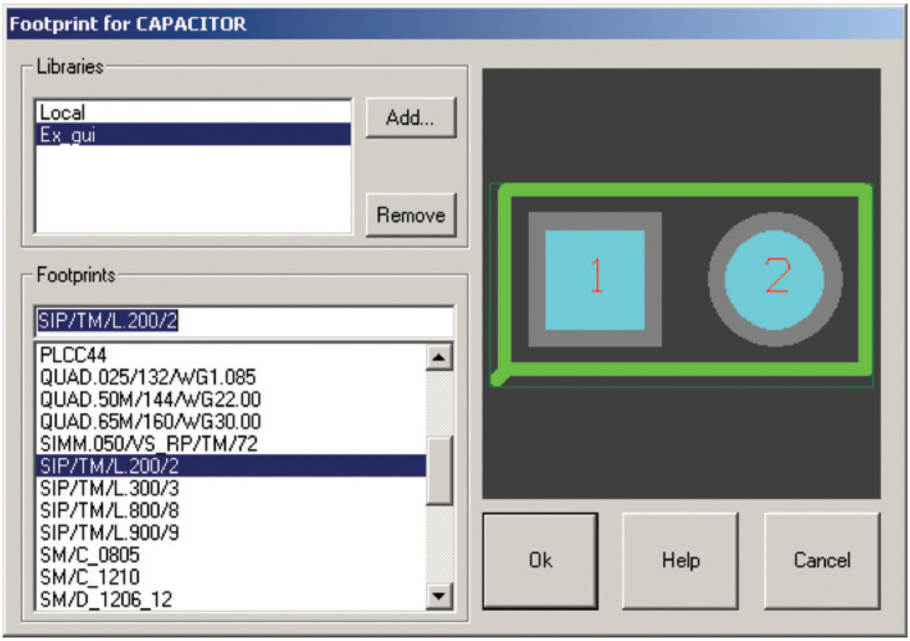

Footprint for CAPACITOR
Libraries
Local
Ex_gui
Add...
Remove
Footprints
SIP/TM/L.200/2
PLCC44
QUAD.025/132/WG1.085
QUAD.50M/144/WG22.00
QUAD.65M/160/WG30.00
SIMM.050/VS_RP/TM/72
SIP/TM/L.200/2
SIP/TM/L.300/3
SIP/TM/L.800/8
SIP/TM/L.900/9
SM/C_0805
SM/C_1210
SM/D_1206_12
1
2
Ok
Help
Cancel

Figure 2-15 Layout Footprint Library utility.

Once the AutoECO utility has completed assigning the footprints, you should end up in the board layout environment shown in Fig. 2-16. This is the Design window for your board. Here you can see the component footprints as well as the silk screen and assembly details. Also visible is the board origin and the board drill symbol table. We will look at those items in greater detail later, but right now we will concentrate on making a board outline, placing the parts, and routing the traces.

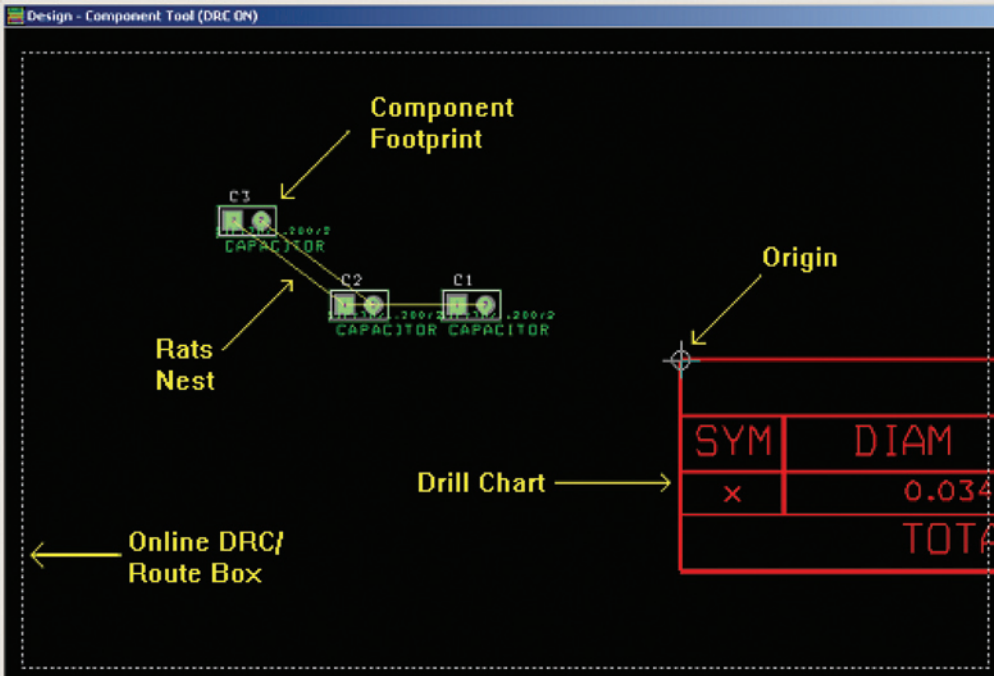


Figure 2-16 Layout initial view.

Notice that on the Windows task bar that there are two Layout applications. The initial one is the Layout session frame and the other is the Design window that was just opened.

To get a better view of what you are trying to work on, you may want to zoom in or out or move the viewing area up, down, left, or right. **To zoom out**, place the cursor at the location you would like the center of view to be and then hit the letter O on the keyboard. **To zoom in**, place the cursor at the location you would like the center of view to be and hit the letter I on the keyboard. **To re-center the view without zooming in or out**, place your cursor at the desired center and hit the letter C on the keyboard. Figure 2-17 shows some of the other "viewing" features you can use from the View dropdown menu. If you ever get to a view that you cannot get out of and want to get back to the Layout work space, select the Design option from the View dropdown menu. You can also hit the Zoom All button (or hit Shift + Home on the keyboard) to see the whole board.

Making a board outline

Next, we will add a board outline. It is good practice to place the board's lower left corner at the origin (see Fig. 2-16). If you have not already done so, zoom out so that you can see the entire drill table and have it located near the bottom of the window. Next, make sure that the online Design Rule Check (DRC) box is off. If you do not see it, it is already off, but if you see a dashed (or solid) white box in the work space, the DRC box is on. **To turn off the DRC box**, click the DRC button. There is another DRC button that looks like DRC, but it is

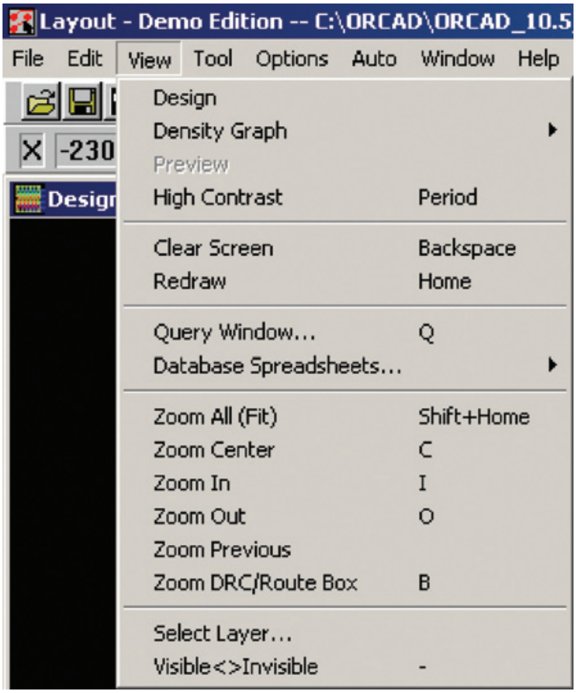
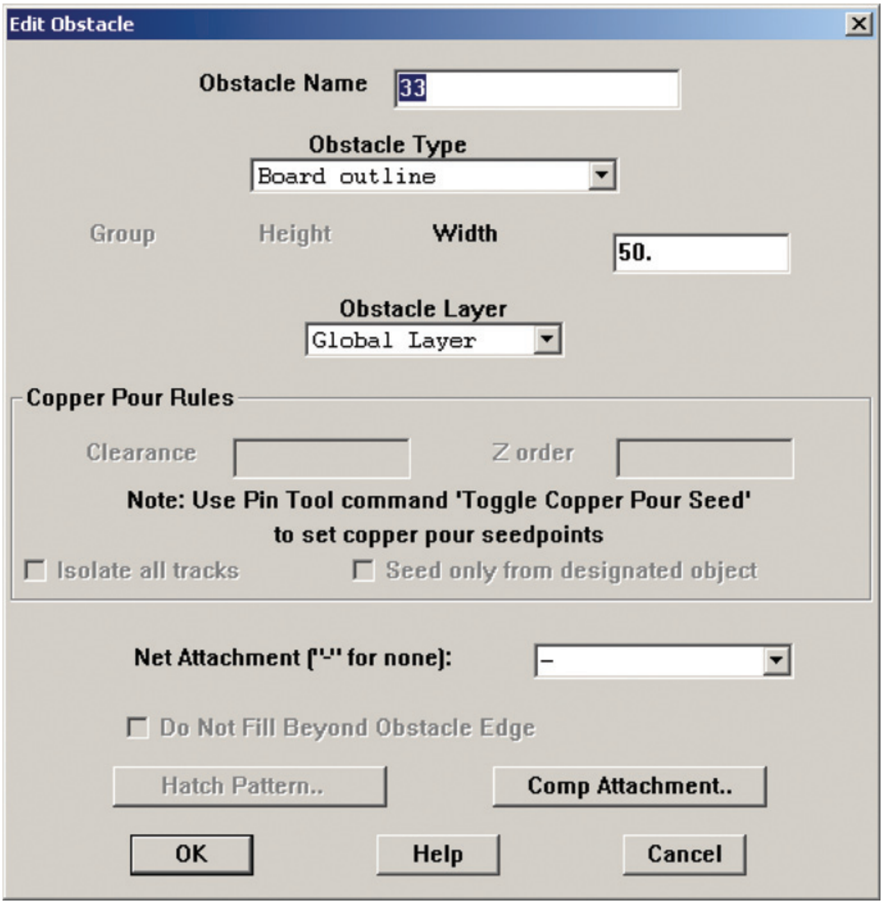

Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5
File
Edit
View
Tool
Options
Auto
Window
Help
-230
Design
Design
Density Graph
Preview
High Contrast Period
Clear Screen Backspace
Redraw Home
Query Window... Q
Database Spreadsheets...
Zoom All (Fit) Shift+Home
Zoom Center C
Zoom In I
Zoom Out O
Zoom Previous
Zoom DRC/Route Box B
Select Layer...
Visible<>Invisible -

Figure 2-17 View/zoom dropdown menu.

for checking the entire design for errors prior to sending the design out for fabrication. The online DRC checks the area within the box while you work. Sometimes it can get in the way of doing what you need to do while you are moving things around, so turn it off for now. **To make a board outline**, click on the Obstacle button—it looks like . Move your cursor to the work area and right click with the mouse; click the New option from the pop-up menu. The cross hair cursor will be smaller now, indicating that it is poised to do something. Right click on the work area again and select the Properties option from the pop-up menu. The Edit Obstacle dialog box will pop up as shown in Fig. 2-18. Make sure that Board Outline is selected in the Obstacle Type dropdown list and that Global Layer is selected in the Obstacle Layer dropdown list. Click OK.

Create a board outline similar to the one shown in Fig. 2-19. Place the cursor over the origin mark in the drill chart's upper left corner (position 1). Click and release the left mouse button once. This begins the first vertex of the board outline. Next move the cursor to position 2. The border will stretch from the last place you clicked to the cursor. At position 2 left click and release again. Continue in the same manner to positions 3 and 4. After you have placed the final vertex at position 4, right click to bring up a menu box and click Finish to complete the board outline. The board outline does not have to be rectangular, but for now it will help keep things simple.



Edit Obstacle

Obstacle Name: 33

Obstacle Type: Board outline

Width: 50.

Obstacle Layer: Global Layer

Copper Pour Rules

Clearance

Z order

Note: Use Pin Tool command 'Toggle Copper Pour Seed' to set copper pour seedpoints

☐ Isolate all tracks ☐ Seed only from designated object

Net Attachment ("-" for none): –

☐ Do Not Fill Beyond Obstacle Edge

Figure 2-18 ***Edit Obstacle*** *properties box.*

Placing the parts

The components are initially placed by Layout in the area to the left of the origin. Typically they are placed in order by component number, and it may be hard to see what they are and how they are connected. You can move the components around to see them better until you are ready to place them within the board outline. Make sure the Component Selection tool is selected, and then left click once and release over a component. The component will be attached to the cursor so that you can move it to the desired location. As you move the part around, you will be able to see the yellow netlist lines (rat's nest) stretch and follow the pads. Click the left mouse button again to place the component inside the board outline. Once you have the parts where you want them, you are ready to route the board.

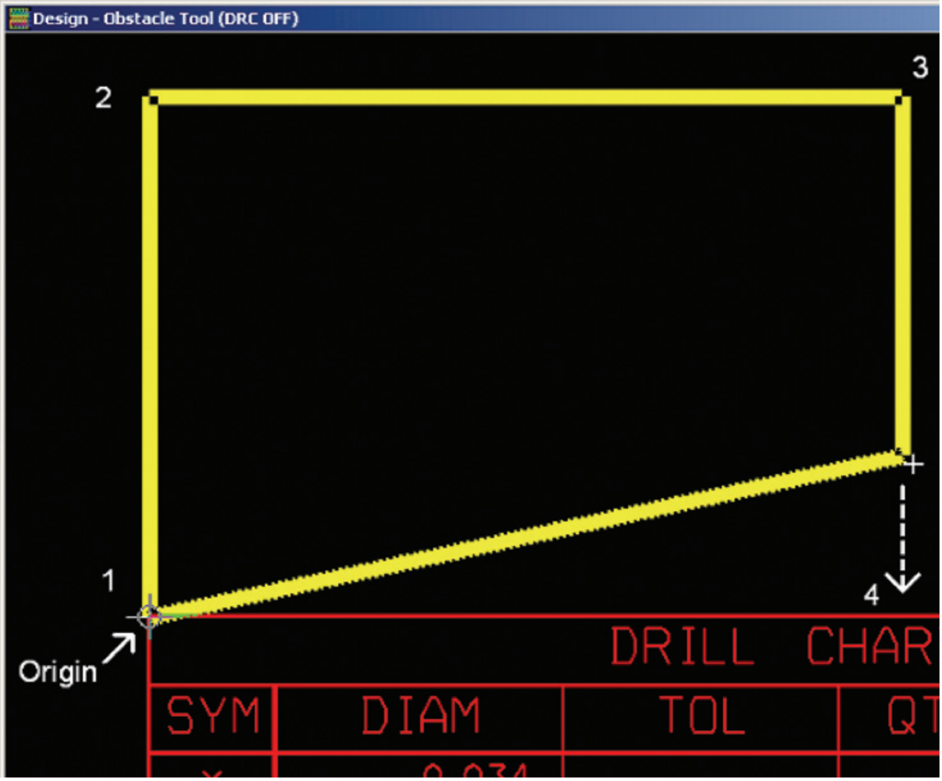


Figure 2-19 Placing the board outline.

Autorouting the board

To route the board automatically, pull the Auto menu down, as shown in Fig. 2-20, and select Auto → Autoroute → Board. Layout will automatically choose the "best" paths and layers to route the entire board. Once the routing is finished, an information dialog box pops up telling you so. Click OK.

Figure 2-21 shows an example of a routed board. Depending on how you placed your parts, Layout may have used layers different from those shown in the figure. In the demo version of Layout, there are 4 default layers that are enabled: Top, Inner1, Inner2, and Bottom. Altogether there are 16 routing layers that you can enable and control. You will learn how to control the different layers in Chaps. 3 and 9.

Manual routing

In Chaps. 3 and 9, we will take an extensive look at manually routing traces, so the manual routing will only be introduced here. There are four manual routing modes. The manual route selection buttons are located on the tool button bar and look like this . Respectively they are the Auto Path Route, Shove Track, Edit Segment, and Add/Edit Route modes.

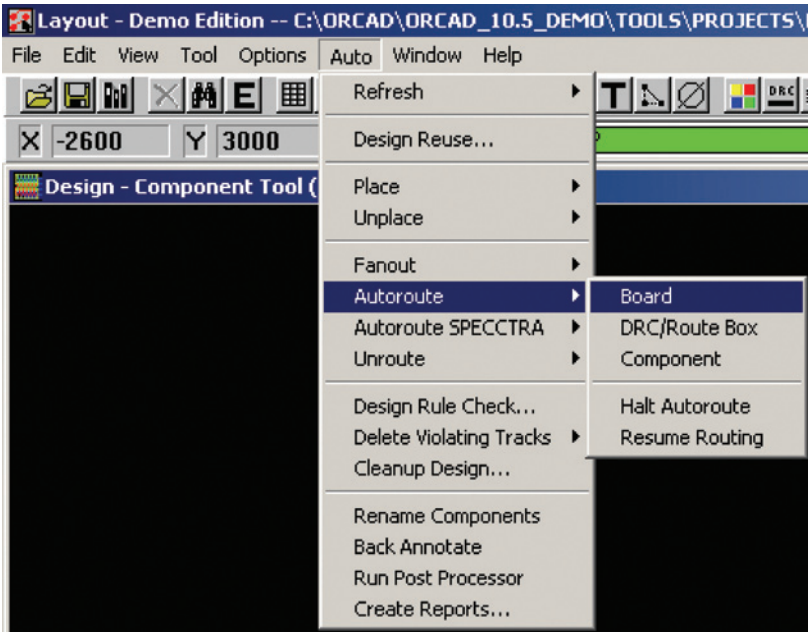

Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\
File
Edit
View
Tool
Options
Auto
Window
Help
X -2600
Y 3000
Design - Component Tool (
Refresh
Design Reuse...
Place
Unplace
Fanout
Autoroute
Autoroute SPECCTRA
Unroute
Design Rule Check...
Delete Violating Tracks
Cleanup Design...
Rename Components
Back Annotate
Run Post Processor
Create Reports...
Board
DRC/Route Box
Component
Halt Autoroute
Resume Routing

Figure 2-20 Autorouting your board.

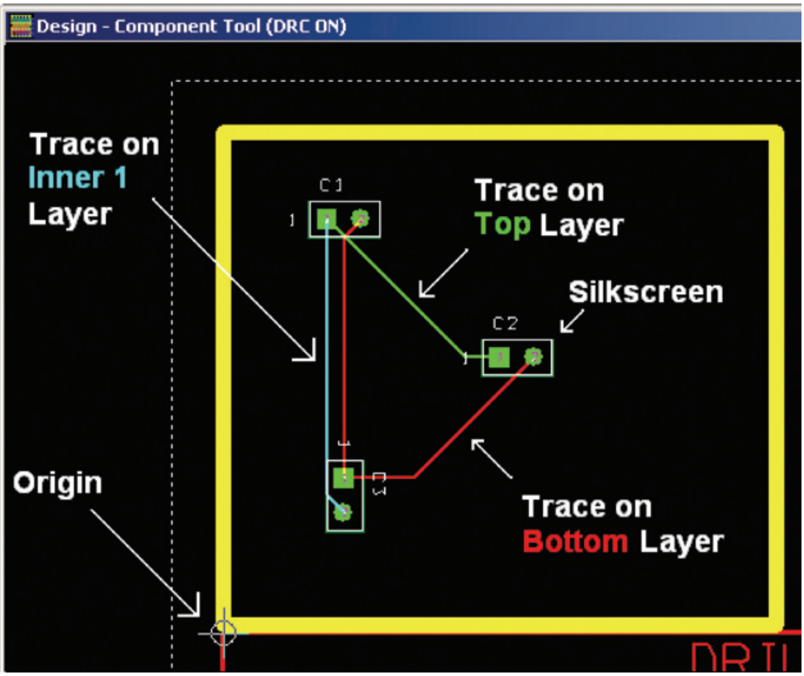
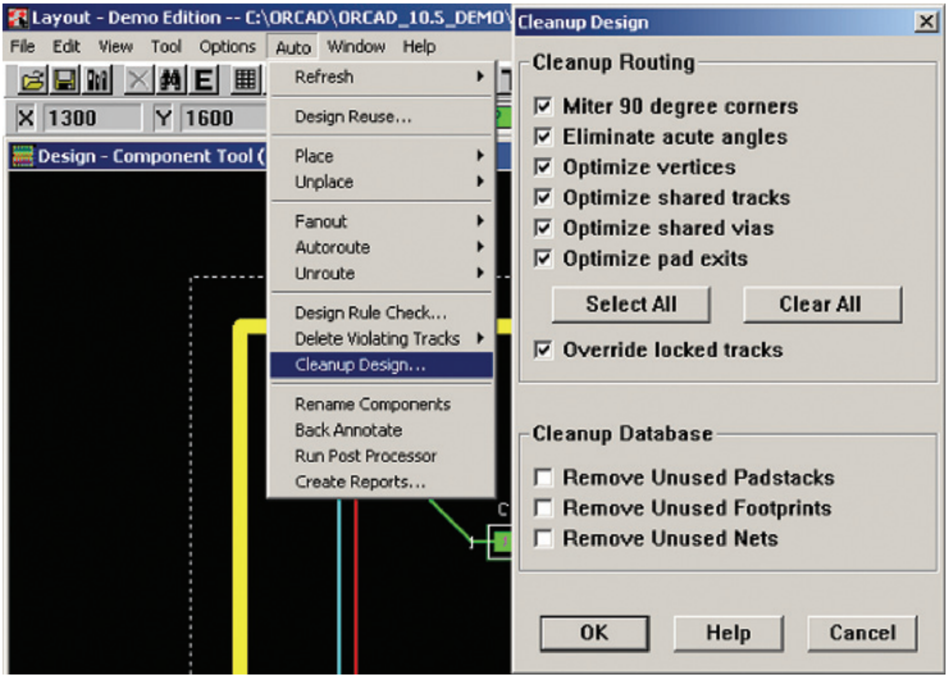

Design - Component Tool (DRC ON)
Trace on Inner 1 Layer
Trace on Top Layer
Silkscreen
Origin
Trace on Bottom Layer
C1
C2
C3

Figure 2-21 Autoroute finished.

The first two tools use some of the autorouting features to assist you when you are manually routing traces. The last two are strictly manual tools and allow direct control of the routing process. You can try the tools out now to see what they do. Do not worry about messing up the board. If things get out of hand you can always start over by unrouting the board from the Auto menu. You can manually unroute (rip up) a trace by selecting a trace by holding down the Shift or Ctrl key on the keyboard while left clicking on the trace. The trace will become highlighted; right click and select one of the unrouting options from the pop-up menu. You can also do an automated cleanup as discussed below.

Cleanup

To perform a cleanup go to Auto → Cleanup Design as shown in Fig. 2-22. Next, check the items you want cleaned up using the Cleanup Design dialog box. Cleanup checks for routing problems such as off-grid or acute angles, bad pad exits, and overlapping vias. If you have certain traces that you do not want altered during a cleanup or any other action, you can lock the traces so that they are protected.


Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEMO\
File
Edit
View
Tool
Options
Auto
Window
Help
X 1300
Y 1600
Design - Component Tool (
Refresh
Design Reuse...
Place
Unplace
Fanout
Autoroute
Unroute
Design Rule Check...
Delete Violating Tracks
Cleanup Design...
Rename Components
Back Annotate
Run Post Processor
Create Reports...
Cleanup Design
Select All
Clear All
OK
Help
Cancel

Cleanup Routing

☑ Miter 90 degree corners
☑ Eliminate acute angles
☑ Optimize vertices
☑ Optimize shared tracks
☑ Optimize shared vias
☑ Optimize pad exits
☑ Override locked tracks

Cleanup Database

☐ Remove Unused Padstacks
☐ Remove Unused Footprints
☐ Remove Unused Nets

Figure 2-22 Cleaning up the board design.

Locking traces

To lock a trace, activate one of the manual routing tools (either the Edit Segment mode or Add/Edit Route mode) and then select the trace by holding the Ctrl button and left clicking the trace. Then right click and select Lock from the pop-up menu, or press L on the keyboard.

Performing a design rule check

After you have completed routing and cleaning up your board, you should check for errors. **To check for errors**, run the project DRC by pressing the DRC button. This DRC is different from the online DRC, DRC. The online DRC checks for errors as you go and checks only whatever it is you are doing at the moment. The project DRC checks the entire board for errors. More will be discussed in Chaps. 3 and 9 on how to set up the DRC.

Postprocessing the board design for manufacturing

At this stage, Layout has generated a design file that fully describes your board. This file is optimized for viewing, editing, and saving on your computer, but it is not in the format that many PCB manufacturers use for fabricating boards. The most common type of file system used in PCB manufacturing is the Gerber file system. Layout has the capability of translating its .MAX file structure to a Gerber file system. This is called postprocessing the design. Normally you would postprocess the design from its existing location, but for this example it will be much easier to see which files the postprocessor generates if you copy the .MAX to an empty folder. So, save the current .MAX design into a new folder all by itself. To do so select Save As… from the File dropdown menu. Click the Create New Folder button in the Save As dialog box and enter a name for the folder. Hit Enter and then double click on the new folder to navigate into it. Click the Save button.

The next step is **to set up the postprocessor**. Select Post Process Settings from the Options menu (see Fig. 2-23). A postprocess spreadsheet will pop up (shown in the background of Fig. 2-24). You can use the spreadsheet to enable specific layers and define the Gerber file format. **To modify a layer's settings**, left click once on the layer in the spreadsheet to select it and then right click on it and choose Properties from the pop-up menu (or double click the layer name). From the Post Process Settings dialog box (Fig. 2-24) you can edit the desired properties. The most important thing to do is to make sure that the Enable for Post Processing box is checked for the layers you used to route the board. If you leave this box unchecked, a Gerber file will not be generated for that layer. When you are finished setting up the postprocessor, click OK to complete the setup process for this example.

To start the postprocessor, select Auto → Run Post Processor from the main menu bar as shown in Fig. 2-25. Layout translates its .MAX file into separate Gerber files for each layer that you enabled.

Once postprocessing is completed, a dialog box pops up telling you "Created Gerber design file *name*.GTD." Click OK. Immediately, another dialog box pops up telling you "Drill tape 1 written to throughole.tap." Click OK again. Finally, a text file automatically opens up in Notepad (e.g., *name*.lis). This is the postprocessor report, which tells you what layers were generated and some information about them. At the bottom, look for the words "No warnings or errors," which means that the process was completed properly. Now look at the folder in which you saved the copied .MAX file. Depending on your postprocess settings, you should see several new files in addition to the .MAX file. These are the Gerber files (digital maps) that were described in Chap. 1 and the files that you would send to a board house to have your board manufactured.

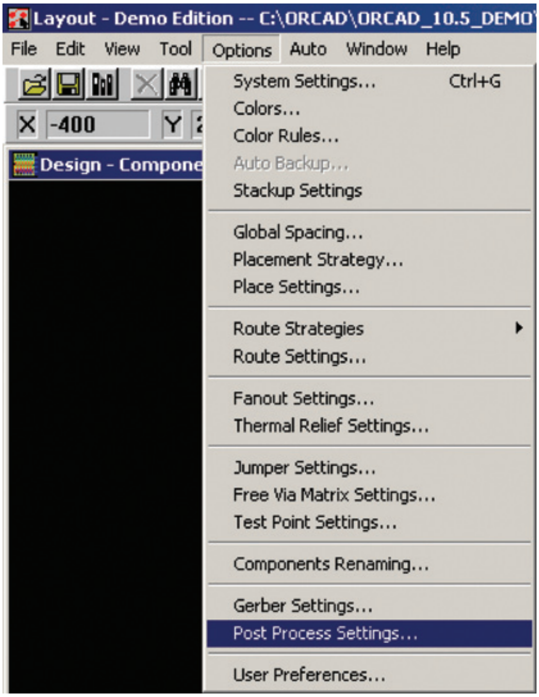
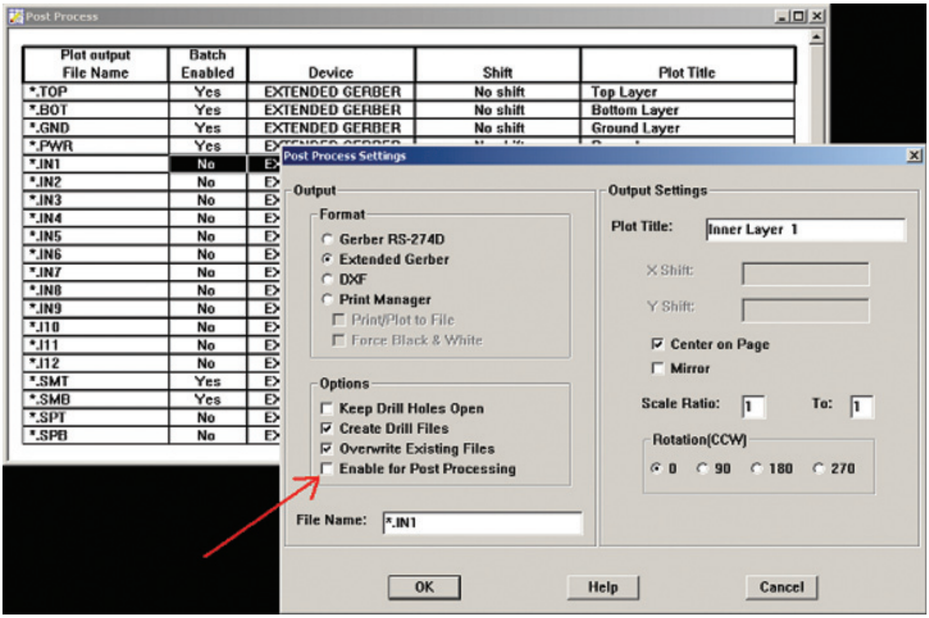

Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEMO
File
Edit
View
Tool
Options
Auto
Window
Help
X -400
Y
Design - Compone
System Settings... Ctrl+G
Colors...
Color Rules...
Auto Backup...
Stackup Settings
Global Spacing...
Placement Strategy...
Place Settings...
Route Strategies
Route Settings...
Fanout Settings...
Thermal Relief Settings...
Jumper Settings...
Free Via Matrix Settings...
Test Point Settings...
Components Renaming...
Gerber Settings...
Post Process Settings...
User Preferences...

Figure 2-23 Postprocess settings from the **Options** menu.


Post Process
Post Process Settings
OK
Help
Cancel

Plot output File Name	Batch Enabled	Device	Shift	Plot Title
*.TOP	Yes	EXTENDED GERBER	No shift	Top Layer
*.BOT	Yes	EXTENDED GERBER	No shift	Bottom Layer
*.GND	Yes	EXTENDED GERBER	No shift	Ground Layer
*.PWR	Yes			
*.IN1	No			
*.IN2	No			
*.IN3	No			
*.IN4	No			
*.IN5	No			
*.IN6	No			
*.IN7	No			
*.IN8	No			
*.IN9	No			
*.I10	No			
*.I11	No			
*.I12	No			
*.SMT	Yes			
*.SMB	Yes			
*.SPT	No			
*.SPB	No			

Output

Format

○ Gerber RS-274D
● Extended Gerber
○ DXF
○ Print Manager
☐ Print/Plot to File
☐ Force Black & White

Options

☐ Keep Drill Holes Open
☑ Create Drill Files
☑ Overwrite Existing Files
☐ Enable for Post Processing

File Name: *.IN1

Output Settings

Plot Title: Inner Layer 1

X Shift:
Y Shift:

☑ Center on Page
☐ Mirror

Scale Ratio: 1 To: 1

Rotation(CCW)

● 0 ○ 90 ○ 180 ○ 270

Figure 2-24 Postprocess spreadsheet and **Post Process Settings** dialog box.

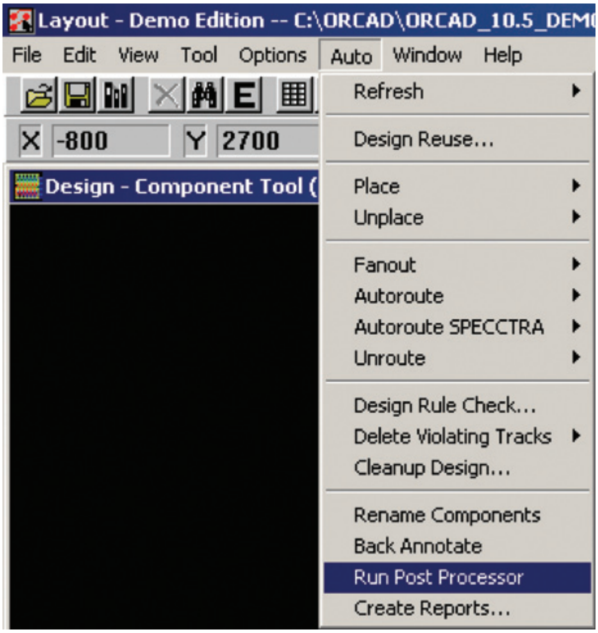

Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEM
File Edit View Tool Options Auto Window Help
X -800 Y 2700
Design - Component Tool (
Refresh
Design Reuse...
Place
Unplace
Fanout
Autoroute
Autoroute SPECCTRA
Unroute
Design Rule Check...
Delete Violating Tracks
Cleanup Design...
Rename Components
Back Annotate
Run Post Processor
Create Reports...

Figure 2-25 Starting the postprocessor.

Congratulations, you have routed your first PCB and postprocessed the design using OrCAD Layout! The objectives of this chapter were to demonstrate the basic steps of designing a circuit schematic, use Layout to create a PCB, and generate the files used to manufacture the PCB. The following is a summary of the process:

1. Start Capture and set up a PCB project using the wizard.
2. Design the circuit using OrCAD Capture.
3. Generate a Layout netlist using Capture and save it as a .MNL file.
4. Start Layout and select a PCB technology (.TCH file) template.
5. Save the Layout project as a .MAX file.
6. Import the .MNL netlist from Capture.
7. Make a board outline.
8. Position the parts.
9. Autoroute the board.
10. Postprocess the board to make the Gerber files used to manufacture the PCB.

In the next chapter we will cover the design flow in greater detail and learn more about the Layout tool set.

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CHAPTER 3

Project Structures and the Layout Tool Set

This chapter explains what you did when making the simple design in Chap. 2 and why. It also introduces and describes the Layout tool set in greater detail so that you will be well equipped to lay out more complicated boards in Chap. 9.

Project Setup and Schematic Entry Details

Capture projects explained

When you set up your project by following the File → New → Project menu path, there were five options to choose from: a project, a design, a library, a VHDL file, or a Text file. The options we will be most interested in are projects and libraries, and we will be looking at those in great detail throughout the book. VHDL files are used in field programmable gate array projects and will not be discussed here. A text file is simply a text file (for making project notes for example).

After you selected the New Project option to begin setting up your project, there were four more options available to you in the New Project dialog box: Analog or Mixed-Signal A/D, PC Board Wizard, Programmable Logic Wizard, or Schematic. A flow diagram of these options and suboptions is shown in Fig. 3-1 (see also Fig. 2-2). Analog or Mixed-Signal A/D is used to simulate analog and/or digital circuits using PSpice. PSpice will be used to develop and test models (Chap. 7), perform circuit simulations (Chaps. 7 and 9), and to simulate transmission lines (Chap. 11). For now we will be working mostly with the second option, the PC Board Wizard, while we focus on designing PCBs. The next option, Programmable Logic Wizard, is for working with programmable devices and will not be discussed in this text. A Schematic is basically just a design file with only a schematic and a parts cache. The thick green line in Fig. 3-1 shows the path you followed in Chap. 2, i.e., File → New → Project → PC Board Wizard → No Simulation.

There are four types of OrCAD libraries. As shown in Fig. 3-2, these four libraries have three different file extensions. There are two types of OLB libraries, an LLB library, and an LIB library. Inside the capture folder there is a library folder, which contains one of the types of OLB files and a folder called pspice, which contains the other types of OLB files. The OLB files located directly in the capture library folder contain simple schematic part symbols and are the ones we used in Chap. 2. The libraries located in the pspice folder contain parts

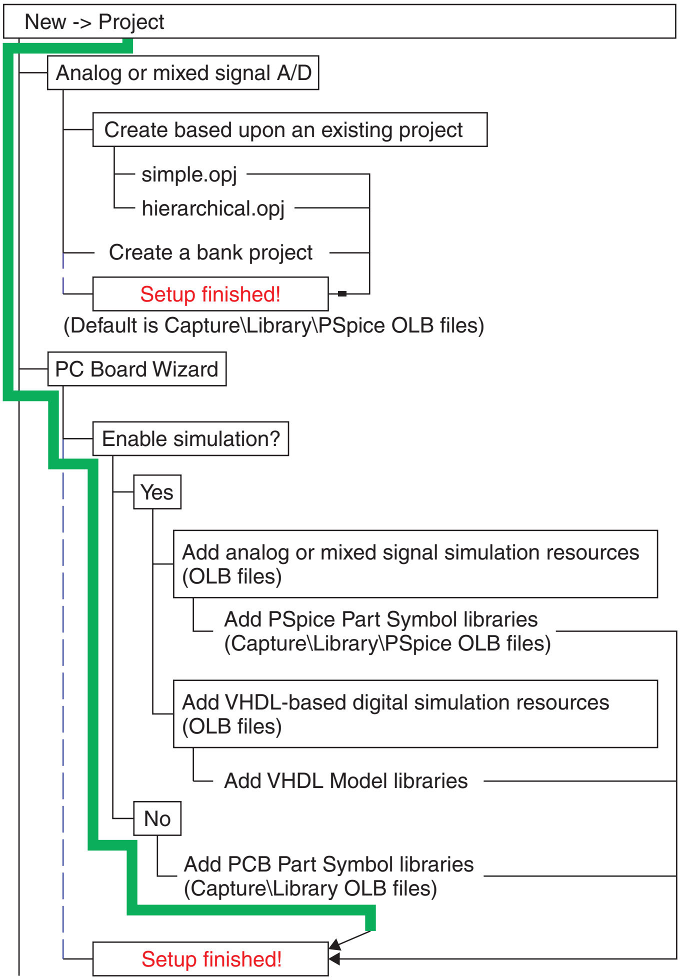

New -> Project
Analog or mixed signal A/D
Create based upon an existing project
simple.opj
hierarchical.opj
Create a bank project
Setup finished!
(Default is Capture\Library\PSpice OLB files)
PC Board Wizard
Enable simulation?
Yes
Add analog or mixed signal simulation resources (OLB files)
Add PSpice Part Symbol libraries (Capture\Library\PSpice OLB files)
Add VHDL-based digital simulation resources (OLB files)
Add VHDL Model libraries
No
Add PCB Part Symbol libraries (Capture\Library OLB files)
Setup finished!

Figure 3-1 New Project design flow and options.

with schematic symbols too, but the parts also contain PSpice templates, which are links to specific PSpice models, and many of the parts also have Layout footprints assigned to them. The PSpice models to which templates point are located in the main OrCAD pspice folder (shown at the bottom of Fig. 3-2). Individual models are grouped into various PSpice library files, which contain the .LIB extensions. The layout library folder contains the footprint libraries, which are files with the .LLB extensions. Most parts in Capture are capable of having a PSpice template or a footprint assigned to them, but only some parts have them preassigned. It may seem backward, but only parts from the PSpice part library (located in the capture library folder) have preassigned templates and footprints. So, in Chap. 2 when you worked with the PCB Project Wizard you selected libraries from the capture/library folder that had parts with schematic symbols but that did not have any PSpice simulation capabilities or footprints assigned to them.

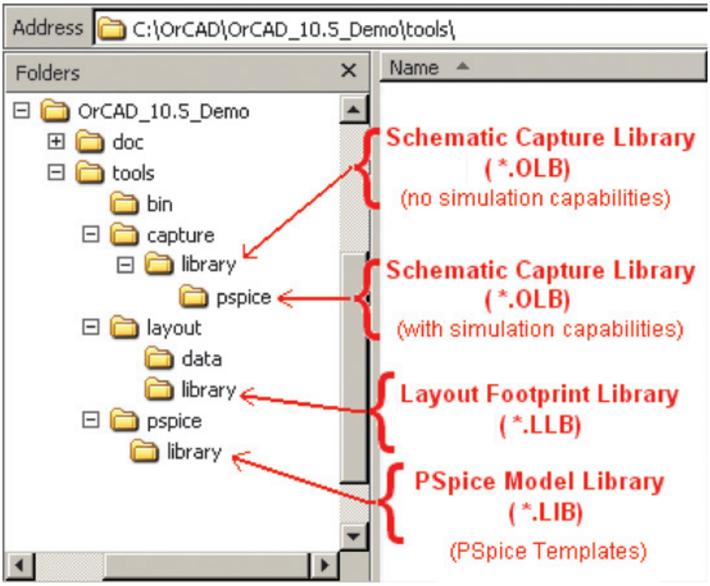
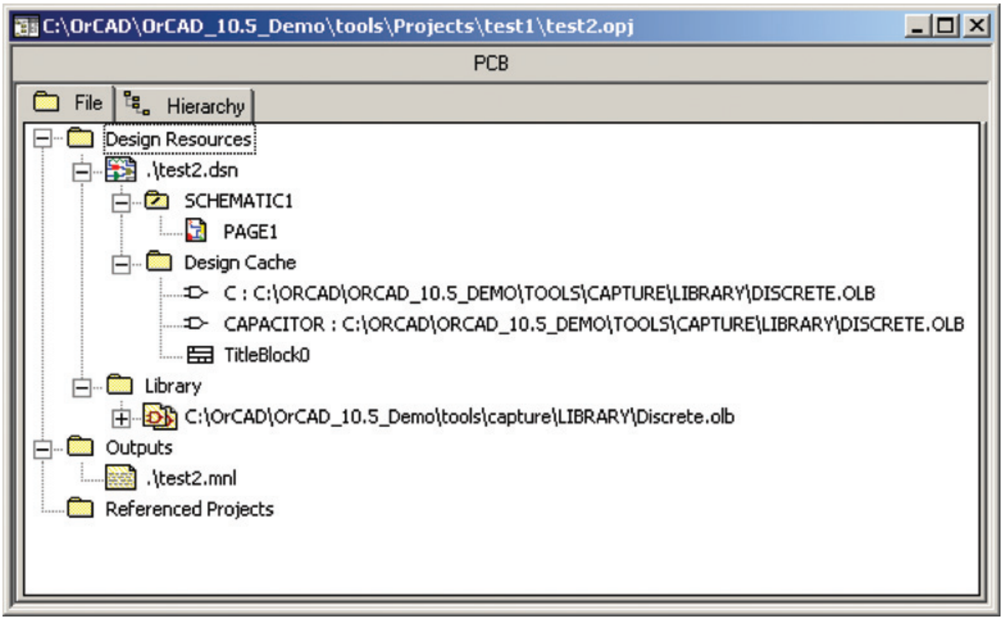

Address
C:\OrCAD\OrCAD_10.5_Demo\tools\
Folders
Name
OrCAD_10.5_Demo
doc
tools
bin
capture
library
pspice
layout
data
library
pspice
library
Schematic Capture Library
(*.OLB)
(no simulation capabilities)
Schematic Capture Library
(*.OLB)
(with simulation capabilities)
Layout Footprint Library
(*.LLB)
PSpice Model Library
(*.LIB)
(PSpice Templates)

Figure 3-2 OrCAD libraries (extraneous files not shown).

Once you clicked Finish in the PCB Project Wizard box, Capture opened up the Project Manager window shown in Fig. 3-3. Behind the scenes, Capture generated two files: an


C:\OrCAD\OrCAD_10.5_Demo\tools\Projects\test1\test2.opj

PCB

File
Hierarchy

Design Resources
  .\test2.dsn
    SCHEMATIC1
      PAGE1
    Design Cache
      C : C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\CAPTURE\LIBRARY\DISCRETE.OLB
      CAPACITOR : C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\CAPTURE\LIBRARY\DISCRETE.OLB
      TitleBlock0
  Library
    C:\OrCAD\OrCAD_10.5_Demo\tools\capture\LIBRARY\Discrete.olb
Outputs
  .\test2.mnl
Referenced Projects

Figure 3-3 Project Manager window.

OrCAD project file (*name*.OPJ) and a design file (*name*.DSN). These files will be in the directory you chose when you set up the project.

As you look at the Project Manager window you can see that a project contains three folders labeled Design Resources. Outputs, and Referenced Projects. Initially, the Outputs and Referenced Projects folders will be empty; we will look at those folders in greater detail in Chap. 9. The Design Resources folder contains one design (represented by the icon) and a Library folder. A project can have only one design, but a design can have several subfolders, which in turn may contain several different items. The Library folder contains links to the libraries that are used by your design. We will discuss library management in Chap. 7. The design contains at least one schematic folder (the root folder) and a Design Cache folder. A design can contain multiple schematic folders, and each schematic folder can contain multiple schematic pages. The Design Cache folder contains a record of each part that you have used in your design. If you modify one of the parts on a schematic page, Capture makes a copy of it (leaving the original part in the library unchanged) and adds a record of the modified part to the design cache. A design with one schematic folder and one or more schematic pages that are connected together by off page connectors is called a flat design. A design with more than one schematic folder and one or more schematic pages per folder or that contains hierarchical blocks is called a hierarchical design. Hierarchical designs are not discussed here since they are not used with PCB design projects. For more information on project details see Chap. 2 of the *Capture User's Guide* under Starting a New Project (cap_ug.pdf in the OrCAD_10.5_Demo/DOC folder).

Capture part libraries explained

Once the project was setup, the next step was to open the Schematic page (if it was not already open) and begin placing parts from the Place dropdown menu. When the Pace Part dialog box opened (see Fig. 3-4(a) or 3-4(b)), it showed a list of libraries (in the Libraries window) and a list of the parts (in the Part List window) within a library. If you select a part within one of the libraries, you can see what the part looks like in the preview window as pointed out in Fig. 3-4(a). The libraries that are listed in the Libraries window are ones that were added by the PC Board Wizard when you set up the current project and libraries that were added to the list during previous projects. You can add other libraries to the list by clicking the Add Library… button. Likewise you can remove a library from the list by selecting it and clicking on the Remove Library button. The libraries that are listed may be from the Capture or the PSpice library. It is not obvious which library it is from just by looking at the name (compare Figs. 3-4(a) and 3-4(b)). However, if you have Windows ToolTips turned on and hold your mouse over the library name, the ToolTips text box will show the path of the library (see Fig. 3-4(a)). From the path, you can tell which type of library it is. Another important note is that if a PSpice or Layout library is associated with the Capture part, you will see one or both of the icons below the part preview window as shown in Fig. 3-4(b). If no icons are present, it means that it is just a Capture schematic part that does not have any footprints or PSpice templates (models) assigned to it.

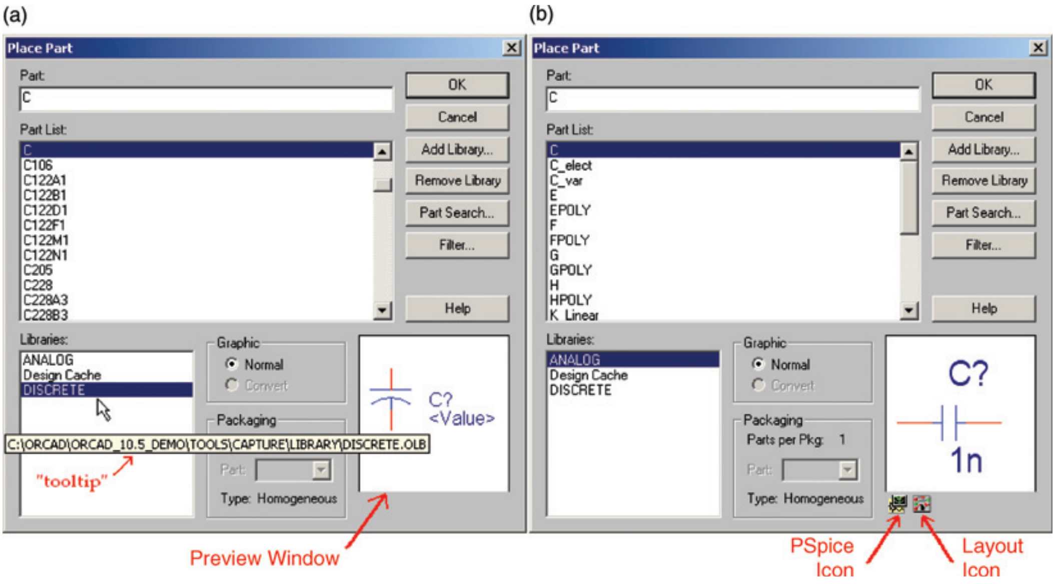

(a)
Place Part
Part:
C
OK
Cancel
Add Library...
Remove Library
Part Search...
Filter...
Help
Part List:
C
C106
C122A1
C122B1
C122D1
C122F1
C122M1
C122N1
C205
C228
C228A3
C228B3
Libraries:
ANALOG
Design Cache
DISCRETE
C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\CAPTURE\LIBRARY\DISCRETE.OLB
"tooltip"
Graphic
Normal
Convert
Packaging
Part:
Type: Homogeneous
C?
<Value>
Preview Window
(b)
Place Part
Part:
C
OK
Cancel
Add Library...
Remove Library
Part Search...
Filter...
Help
Part List:
C
C_elect
C_var
E
EPOLY
F
FPOLY
G
GPOLY
H
HPOLY
K_Linear
Libraries:
ANALOG
Design Cache
DISCRETE
Graphic
Normal
Convert
Packaging
Parts per Pkg: 1
Part:
Type: Homogeneous
C?
1n
PSpice Icon
Layout Icon

Figure 3-4 ***Place Part*** *from Capture or Capture/PSpice library. (a) Capture parts. (b) PSpice parts.*

As you place parts in your design, Capture keeps track of the parts and stores the information in a database file that is generated the moment you place your first part. This file has a .DBK extension. After you finished your design and told Capture to make the Layout netlist, Capture generated a fourth file (the netlist itself) that describes which parts were used and how they were connected in the format that Layout uses. The Layout netlist file has a .MNL file extension and is added to the directory with the other project files unless you specify otherwise. Later in the design process you can back annotate PCB information into the Capture design through the use of a .SWP file that Layout creates. The PCB information is imported into Capture and added to the .MNL file so that when you can update a PCB design later with new information from Capture (using the AutoECO) changes made to the PCB design in Layout are not unintentionally undone by Capture (i.e. they stay synchronized). More will be discussed on back annotation in Chap. 9.

Understanding the Layout Environment and Tool Set

Board technology files

At this point in Chap. 2, you started Layout. It would seem that the next logical step would be to open the .MNL netlist file. But Layout needed to know what type of board technology to use first. That is why you selected New from the File menu and searched for a .TCH file (technology template) before opening the .MNL file. You used the default.tch template to start with, but there are 21 different templates (in the version 10.5 Demo) from which you could have chosen. There are also board templates (which have a .TPL file extension) that have been set up for custom boards. The technology files set the number of allowed layers, the pad and drill sizes for IC pin pads, and the dimension units (e.g., metric or mils). The `default` technology file assigns a Level A multilayer board. There are three design levels specified by the Institute for Printed Circuits (IPC) (described in more detail in Chap. 4); they are Levels A, B, and C. The design levels in OrCAD Layout are related to the IPC design levels but do not necessarily map directly into them. In both Layout and IPC, Level A is a general design complexity. Standard IPC-2221A contains tables related to what are known as standard fabrication allowances (SFAs). Layout uses the SFAs to set baseline routing and spacing rules. For example, a Level A technology file in Layout allows only one trace between DIP IC pins and uses 62-mil (0.062-in.) pads and 38-mil drill holes for IC pins, a 25-mil routing and via grid, a 100-mil component placement grid, and 12-mil route spacing. Technology files using Level B and C design complexity allow two and three traces between pins, respectively, so the IC pin pads are smaller to make room for the additional traces. A summary of a few of the technology files is given in Table 3-1. Technology templates are discussed in the *Layout User's Guide* (lay_ug.pdf) in Chap. 4 under Technology Templates and in Appendix A.

After you selected the technology file, Layout asked you for the netlist file—the .MNL file—that you generated in Capture. Layout adds additional information, puts it in a specialized format, and saves it as a .MAX file. The .MAX file contains information such as board size, where the components will be physically located, and the size and location of the traces along with the information that Capture put into the original .MNL file.

Technology	Application	Design complexity
Default	Typical non-RF frequency FR4-type boards using surface mount and/or through-hole components	A
1BET_ANY	Same as Default, one trace between IC pins	A
2BET_SMT	Similar to Default but geared toward surface mount boards as the routing parameters are more compact	B
2BET_THR	Through-hole boards, two traces between IC pins	B
3BET_ANY	High-density mixed package boards, three traces between IC pins	C
Tutor	Used with the Layout tutorial	A

Table 3-1 Technology files

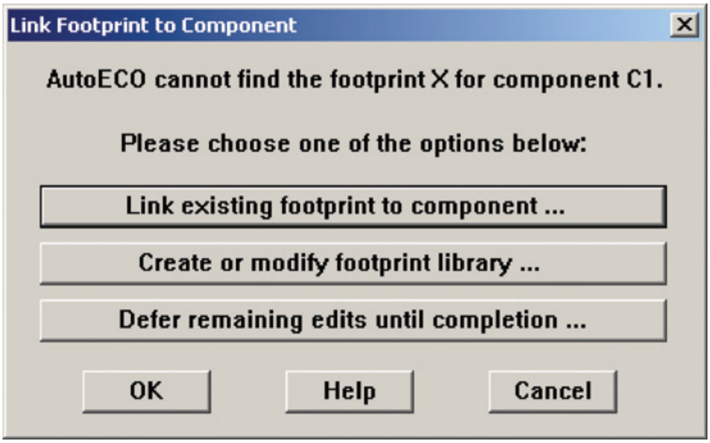
The AutoECO utility

After saving the basic design information in the new .MAX file, Layout's AutoECO (automatic engineering change order) utility works to link footprints from the Layout library to packages/footprints listed in the original .MNL file. It also generates other files such as *name*.log, *name*.ERR, and *name*.lis.

Note

- *From the time you start your design in Capture to the time you postprocess your board in Layout you could have nearly 40 files that are generated, which together fully describe your design. If you save more than one project in the same folder, it can become very cluttered. It is a good idea to set up a "MyProjects" folder that contains subfolders for each project.*

If no footprints were assigned to parts in Capture or if one was assigned that does not exist in the Layout footprint library, the AutoECO brings up the Link Footprint to Component dialog box (shown in Fig. 3-5) and gives you three options: (1) link a footprint to one of the Layout libraries, or (2) make a new footprint now and link it to the part, or (3) do not do anything right now.


Link Footprint to Component
Link existing footprint to component ...
Create or modify footprint library ...
Defer remaining edits until completion ...
OK
Help
Cancel

AutoECO cannot find the footprint X for component C1.

Please choose one of the options below:

Figure 3-5 ***Link Component to Footprint*** *dialog box.*

In Chap. 2 you selected the first option and looked through the Ex_gui.LLB library to find the SIP/TM/L.200/2 footprint. Once you selected the footprint, the AutoECO utility automatically linked that footprint to all the components of the same type that were in the netlist (i.e., every capacitor—C1, C2, and C3—from the discrete library that you placed into the schematic). The AutoECO utility brings up the linking dialog box for every type of component for which it could not find a known footprint. Layout keeps a record of this information and automatically uses that footprint as the default footprint for that component type for all future projects. You can prevent this by making sure you assign a footprint in Capture before you generate the .MNL netlist. If you forget to assign a footprint ahead of time and Layout assigns the default footprint, you can always change it in Layout or Capture afterward.

If you choose the second option, Create or modify footprint library…, the Layout footprint Library Editor will automatically open. From there you can alter an existing footprint or make a new footprint. Once you save the new footprint, you can close the Footprint Editor and you will be taken back to the AutoECO utility with the same three options you started with. However, now you can click on Link existing footprint to component… and link the footprint you just made to the part the AutoECO utility is asking about.

If you choose the third option, Defer remaining edits until completion…, the AutoECO utility will continue on with the rest of the .MNL netlist looking for parts with valid footprints. If all footprints have not been assigned by the time the AutoECO utility has finished the AutoECO will fail and a board will not be generated, and you will have to start the whole process over again.

Once the AutoECO utility finished linking footprints to the parts in the schematic, Layout opened the Design window. The parts are automatically placed to the left of the origin, connected with thin yellow lines (called a "rat's nest"). From this point you made a board outline, placed the parts on your board, autorouted the board, and postprocessed it. To be fluent at these tasks, you need to know how to use the Layout tools. We will now take a tour of the Layout environment and tool set.

The session frame and Design window

First, we will back up a step and take a second look at Layout's session frame and Design window. When you first start Layout (before importing the .MNL file) the first thing that you see is the session frame shown in Fig. 3-6(a). After you imported the .MNL file, and the AutoECO utility finished creating the .MAX file, Layout opened a Design window for your project as shown in Fig. 3-6(b). It is possible to close the session frame and leave only the Design window open, but it is best to leave the session frame open with the Design window because the session frame acts as a "director" and helps your design interface with other applications such as Capture. It is also possible to have more than one Design window open, but it is best

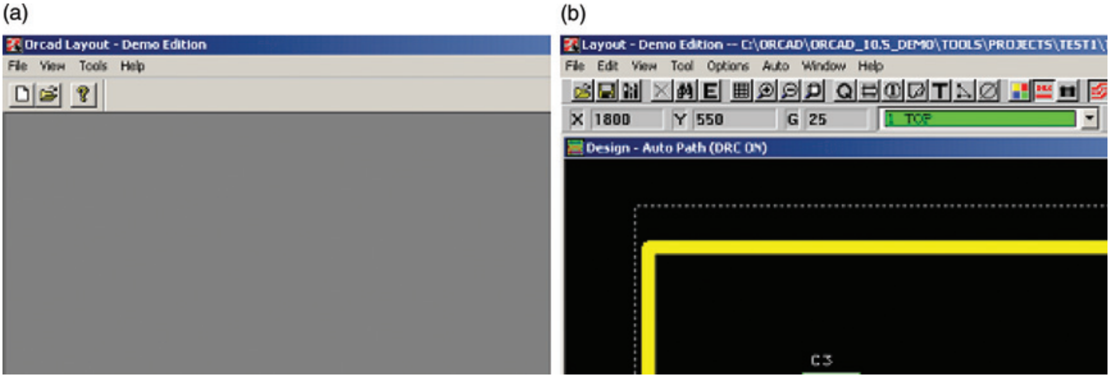

(a)
Orcad Layout - Demo Edition
File View Tools Help
(b)
Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TEST1\
File Edit View Tool Options Auto Window Help
X 1800
Y 550
G 25
1 TOP
Design - Auto Path (DRC ON)
C3

Figure 3-6 The Layout project environment. (a) The session frame. (b) The Design window.

to have only one open at a time because you can inadvertently make undesirable changes to one design while working with one of the others. This is especially true when performing design updates from Capture to Layout using the AutoECO tool (more on that in Chap. 9).

The session frame

The session frame is the starting point for working in Layout. From the session frame's File menu on the menu bar, you can start a new design or open an existing one or import a design file from another application (PADS, Protel, etc.). From the session frame's Tools pulldown menu you can access the Layout initialization file (LSESSION.ini) to change your application settings, and you can access the Library Manager (the footprint library). You can also create or print a footprint catalog of a particular library or design (see Chap. 7 for an example). The Tools menu also provides a connection to other applications such as OrCAD Capture and GerbTool (depending on the options that came with your package).

From the Tools menu you can select the type of forward annotation (design update from Capture to Layout) you want to perform using the AutoECO tool. There are seven types of ECOs; six types are used to transfer data from Capture to Layout during forward annotation, and the seventh (AutoECO/Net Attrs) transfers information between printed circuit boards. The seven types of ECOs are discussed in detail in Getting Started (Chap. 2) in the *Layout User's Guide* and are discussed in the AutoECOs section at the end of Chap. 9 of this book.

The Design window

The Design window is the working environment for a board design. From the Design window you have access to the tools that you need to handle parts, route traces, and perform back annotations (design updates from Layout to Capture). There are about 200 tasks that can be executed from the Design window menus. Since they are covered in detail in Chap. 20 of the *Layout User's Guide* (see the Layout Commands section), a detailed discussion of the menus will not be given here. A few key menu options will be discussed in Chap. 9 as the need arises. The toolbar is discussed below.

The toolbar

The toolbar is shown in Fig. 3-7. Although the *User's Guide* does not describe the tools on the toolbar in the following way, you can think of the toolbar as being divided into four functional sections: general project tools (11 tools), object selection tools (6 tools), manual routing tools (4 tools), and environmental control tools (5 tools). These tools are described below and

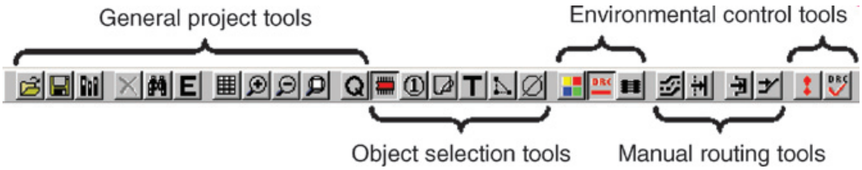


Figure 3-7 Toolbar tools.

additional information about the toolbar can be found under The Layout Design Environment, User Interface, The Toolbar, and in Table 3-1 of Chap. 3 of the *Layout User's Guide.*

General project tool buttons

The general project tool buttons are related to actions that pertain to the project as a whole or general actions that can be applied to multiple object types (e.g., components or text) within your project. Most of these tools exhibit common Windows functions, but there are a couple of functions unique to Layout. The general project tools are as follows:

Open File

The Open File tool is similar to a Windows Open File tool but is geared toward files used in Layout. It can be used to open a .MAX project (default), a template file (.TPL or .TCH), a strategy file (.SF), or a footprint library (.LLB). The same action can also be performed from the File → Open dropdown menu on the menu bar.

Save Project

The Save Project tool saves the current .MAX file (no surprises there). The same action can also be performed from the File → Save dropdown menu on the menu bar. From the File dropdown menu you can also select Save As… to save the current project as a .MAX file with a different name. You can also save the project properties by saving the project as a template (.TPL or .TCH), a strategy file (.SF), a library (.LLB), a postprocess setting file (.PPS), a color setup file (.COL), or an aperture list file (.APP). Additional details and examples of generating templates are covered in Chap. 9 of this book.

Library Manager

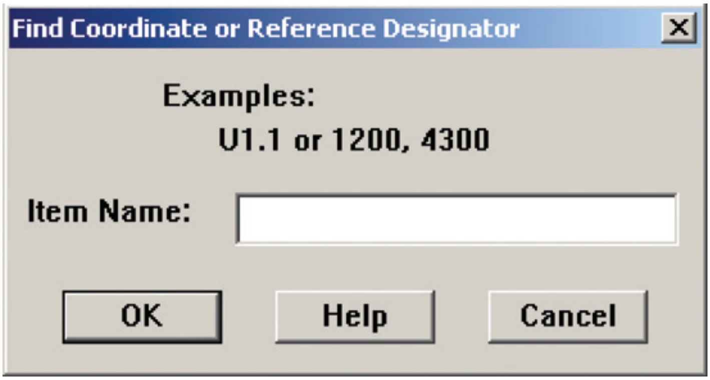
The Library Manager is used to edit or construct footprints and padstacks. You can invoke the Library Manager with this button or by selecting Library manager from the Tools menu in the main Layout session frame. Design of footprints and padstacks is covered in detail in Chap. 8.

Delete

The Delete tool button is grayed out (inactive) if you have nothing selected. It becomes active when something has been selected with the mouse. Then if you press the Delete button, the selected object will be deleted. You can do the same thing with the Delete key on your keyboard. If the action of deleting the selected object could cause a significant change (or problem) with the project, Layout will stop and ask you if that is in fact what you want to do.

Find

When you click the Find tool, a Find Coordinate or Reference Designator dialog box pops up (Fig. 3-8). When you enter a part, a specific pin on a part, or a specific location, the Find tool moves the cursor to that spot and centers the view there. There are other types of search tools, which will be described in detail in Chap. 9.



Find Coordinate or Reference Designator

Examples:
U1.1 or 1200, 4300

Item Name:

*Figure 3-8 The **Find** dialog box.*

E Edit

If you have an object (component or net, etc.) selected, clicking the Edit tool brings up the Edit Properties dialog box. It performs the same function as selecting an object, right clicking on it, and selecting Properties from the pop-up.

▦ Spreadsheets

Spreadsheets are used extensively in Layout for interacting with and manipulating many types of parameters. The reason that spreadsheets are used is that they provide a convenient way of organizing and displaying large amounts of properties at one time, and through various user interfaces, they provide a convenient means for modifying the properties. Figure 3-9 shows the various spreadsheets that are accessible from the dropdown list that appears when you click the Spreadsheet button. The spreadsheets will be used and discussed often throughout this book, and you can read more in Chap. 3 of the *Layout User's Guide* in the Layout Design Environment, Spread Sheets section.

Zoom buttons

Pressing the Zoom In or Zoom Out buttons changes the cross-hair cursor to the zoom cursor—Z. If you press the Zoom In button and click a spot in the work space, the click point becomes the center of view, and the view will automatically zoom in. The same thing is true with the Zoom Out button. If you drag a box around an area the view will zoom in to encompass as much of the box as possible regardless of whether the Zoom In or Zoom Out button was pressed. Zoom All centers the board and zooms in or out as needed to fit the entire board within the screen. This enables you to see the entire board as large as possible. You can also zoom in by pressing the I key on the keyboard, or zoom out by pressing the O key on the keyboard. You can also pan the board with the keyboard by placing the pointer where you want the center of the view to be and then pressing the C key.

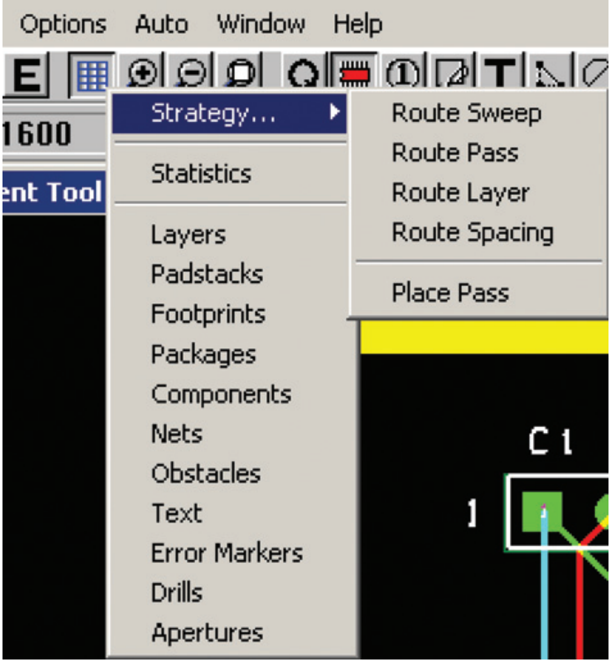

Options
Auto
Window
Help
E
1600
ent Tool
Strategy...
Statistics
Layers
Padstacks
Footprints
Packages
Components
Nets
Obstacles
Text
Error Markers
Drills
Apertures
Route Sweep
Route Pass
Route Layer
Route Spacing
Place Pass
C1
1

Figure 3-9 The ***Spreadsheet*** *menu from the Spreadsheet tool button.*

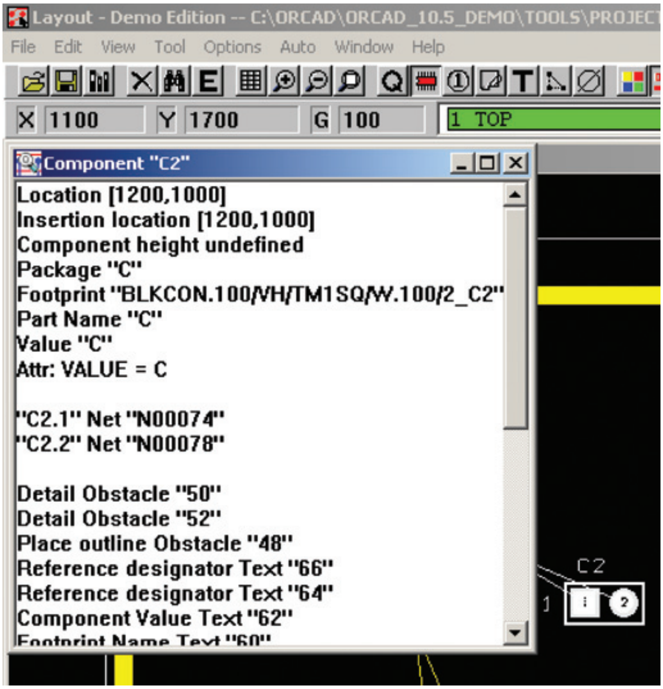
Query

Use the Query window in combination with the Object Selection tools to view an object's properties. An example Query window is shown in Fig. 3-10. The Query window is quite powerful as it does more than just display text. The Query window is interactive. You can right click on keywords and lines of text within the window to bring up pop-up menus that are unique to queries. For example, if you have the simple board project from Chap. 2 open, click the Query button to open a blank Query window. Inside the window right click (with the Q cursor) and select Find/Goto from the pop-up menu. Type a "C" and click OK to find capacitors. The query window will list all capacitors in the design. Next, right click again and select Properties from the pop-up menu. Click on C2 within the Used by component "C2" text string, and the Query window will show information specific to C2 (such as location and package type) as shown in Fig. 3-10.

Selection tools

Component

The Component selection tool button is quite powerful. It provides numerous options when working with the footprints on your board. As Fig. 3-11 shows, if you have the Component tool button active and right click on the background without having a component selected, you get a pop-up menu (Fig. 3-11(a)) that is different from right clicking when you have a


Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECT
File Edit View Tool Options Auto Window Help
X 1100
Y 1700
G 100
1 TOP
Component "C2"
C2
1
2

Location [1200,1000]
Insertion location [1200,1000]
Component height undefined
Package "C"
Footprint "BLKCON.100/VH/TM1SQ/W.100/2_C2"
Part Name "C"
Value "C"
Attr: VALUE = C

"C2.1" Net "N00074"
"C2.2" Net "N00078"

Detail Obstacle "50"
Detail Obstacle "52"
Place outline Obstacle "48"
Reference designator Text "66"
Reference designator Text "64"
Component Value Text "62"
Footprint Name Text "60"

Figure 3-10 The Query window.

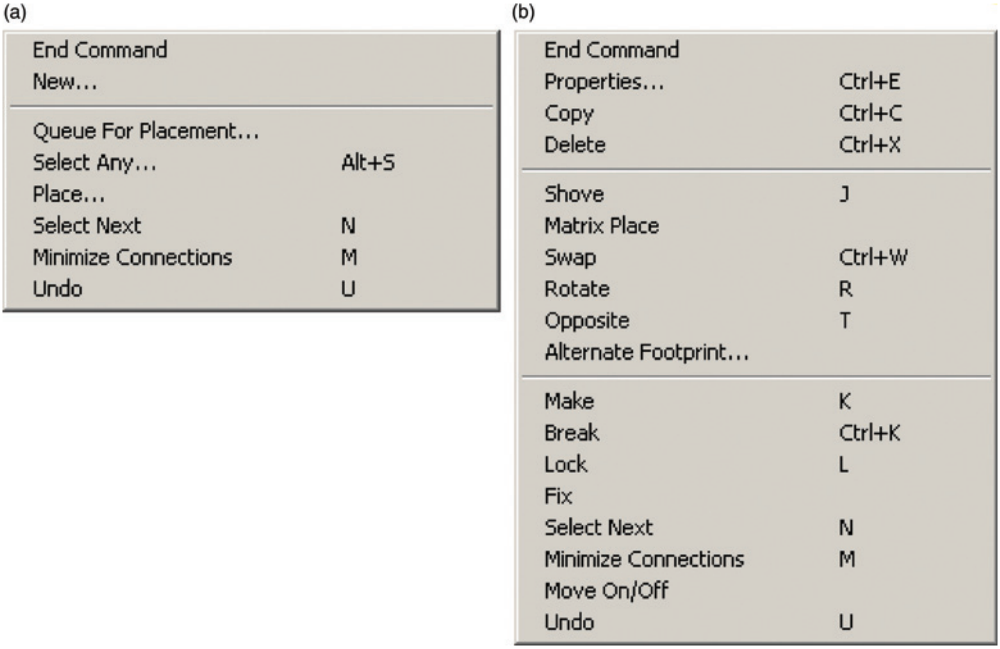

(a)
End Command
New...
Queue For Placement...
Select Any... Alt+S
Place...
Select Next N
Minimize Connections M
Undo U
(b)
End Command
Properties... Ctrl+E
Copy Ctrl+C
Delete Ctrl+X
Shove J
Matrix Place
Swap Ctrl+W
Rotate R
Opposite T
Alternate Footprint...
Make K
Break Ctrl+K
Lock L
Fix
Select Next N
Minimize Connections M
Move On/Off
Undo U

Figure 3-11 Component selection tool options. (a) Without a component selected. (b) With a component selected.

component selected (Fig. 3-11(b)). The basic purpose of the Component selection tool is to select, move, modify, or delete a component (footprint), but it possesses many other capabilities. Examples of how to use many of the functions are given in Chap. 9 with the design examples. If you want to read more about the Component tool functions, please see the *Layout User's Guide*, Chap. 9, Placing and Editing Components, in the Placing Components Manually section.

Pin

The basic purpose of the Pin selection tool is to select, move, modify, or delete a pin within a footprint. As with the Component selection tool, when you right click you get different pop-up menus depending on whether you have a pin selected or not. You will use some of the advanced functions of the Pin tool in Chap. 9. One example of the use of the Pin tool is to modify a footprint or pin on a board without opening the Library Manager. This is allowed only when you check the "Allow Editing of Footprints" box in the User Preferences dialog box, which you access when you select User Preferences… from the Options menu. If the "Allow Editing of Footprints" box is left unchecked, you will not be able to edit any of the board's footprints (or pins within the footprint).

Obstacles

The Obstacles selection tool allows you to select and then edit, move, copy, or delete obstacles. Obstacles are graphical objects that define the appearance of parts and restrict where components and traces can be placed on a board. Common obstacles are silk-screen part outlines, board outlines, copper pour areas, insertion outlines, and place outlines.

There is a trick to moving obstacles. To move an obstacle without stretching or distorting it, press Ctrl + left click on the obstacle, then left click (and hold) on the obstacle to drag it to its new position. If you just click on an object by its edge, you will stretch the obstacle's segment (and sometimes adjacent segments). Use the left click without Ctrl to resize an obstacle. To copy or edit an obstacle, Ctrl + left click on it; then right click and select the desired action from the pop-up menu. If you want to paste more than one copy of an obstacle (or any object for that matter), position the cursor at the desired location and press the Insert key on your keyboard. In older versions of Layout if you right click and then select Paste, you will be able to paste only one copy of the object. To paste additional copies, you would then have to copy the object repeatedly. In the newer versions of Layout you can use the Paste command repeatedly as you would in other Windows applications. You can select more than one obstacle at a time by holding down the Ctrl key and then left clicking on each obstacle you want to select.

Text

The Text selection tool is straightforward. You can use it to select and then move, edit, copy, or delete text. As with obstacles, you can use the Insert key on your keyboard or use Ctrl + V to repeatedly paste copies of text objects.

Connection

The Connection tool is used to create nets for a PCB that are not in the Capture schematic/netlist. It is also used to split nets, add and delete pins connected to nets, and disconnect pins from nets. An example in which you would use this is in adding guard traces to your PCB as described in the design examples in Chap. 9. Changes to nets or pins made using the Connection tool cannot be back annotated to the schematic design.

Error Marker Selection

The Error Marker Selection tool allows you to select an error marker to find out what the error is and its location. Error markers are generated by running a DRC (see Project DRC below) and help you identify design rule violations. You can use the error marker tool with the query window to display more information about the error.

Environmental control tools

Color Settings

The Color Settings control button is straightforward; it is used to control the color of any layer or object (obstacles, pin names, etc.) in your design. It is also one of the tools used to make layers visible or invisible. Examples of using the color settings button to change the color of nets and thermal reliefs are given in Chap. 9.

Online Design Rule Check (DRC)

The online DRC encompasses an area defined by a rectangular box. The rectangular area is called the Route Box or the DRC Box. When the online DRC is inactive it is not visible; when it is active it is a rectangle that is made of either dotted lines or solid lines. The appearance and function of the box depend on what you are doing on your board at the time. When the Route Box is dotted it is in “standby” mode, but when actions are being performed that stimulate the online DRC to monitor what is going on, the boundaries become solid lines. One of the functions of the DRC is to prevent you from performing certain actions (e.g., routing traces or placing components) that will violate spacing rules. Another function is to focus the autorouter to particular areas of the board during various stages (called sweeps and passes) of autorouting. You can usually toggle the online DRC on or off at any time except when performing certain manual functions such as Autopath Route Mode or Shove Track Mode as discussed below.

Reconnect Mode

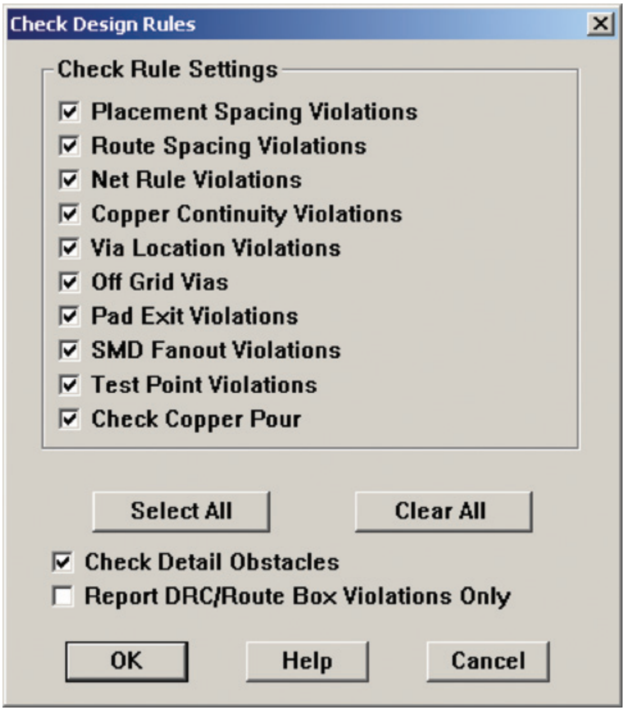
This tool shows or hides rat’s nest lines (it does not really disconnect or reconnect things, it just makes it look like it). It simplifies your view when placing parts on a board. It can also be used in conjunction with the Component tool and the Select Any command from the Edit drop down menu.

Refresh

Pressing the Refresh button not only repaints the traces and copper areas in the current view on your display, it also redraws unrouted connections (the rat’s nest) to minimize their lengths and updates thermal relief connections to plane layers. Refresh also causes board statistics to be recalculated (see the statistics spreadsheet for examples of statistics calculations). **When in doubt hit the Refresh button.**

Project DRC

When you press the Project DRC tool button Layout checks your entire design for design rule violations that are set in the Check Design Rules dialog box (see Fig. 3-12). To access the Check Design Rules box, go to the Auto menu and click Design Rule Check. Any errors that are found after running the DRC are marked with error markers (circled X's) and can be investigated using the Error Marker selection tool and the Query window as discussed above.



Check Rule Settings

☑ Placement Spacing Violations
☑ Route Spacing Violations
☑ Net Rule Violations
☑ Copper Continuity Violations
☑ Via Location Violations
☑ Off Grid Vias
☑ Pad Exit Violations
☑ SMD Fanout Violations
☑ Test Point Violations
☑ Check Copper Pour

☑ Check Detail Obstacles
☐ Report DRC/Route Box Violations Only

Figure 3-12 ***Check Design Rules*** *dialog box.*

Manual board route/Edit Mode tools

There are four manual routing tools. Two can be used in a completely manual mode with or without the online DRC box. The other two manual routing tools are actually semimanual because they use the online DRC function and interact with the autorouter.

Manual routing tools

The manual routing tools—Edit Segment Mode and Add/Edit Mode—are used when you want to have complete control over where traces are routed. These tools can be used with or without the online DRC tool.

Add/Edit Route Mode

Use the Add/Edit Route Mode to route new tracks from a rat's nest, edit existing traces one segment at a time, or automatically finish a partially routed trace. When automatically finishing a trace Add/Edit Mode will try to route a trace from the current location through the shortest path possible if it can do so without violating design rules. It may temporarily enter Edit Segment Mode to do so. In Add/Edit Route Mode you can also add vias by typing the number of the new layer on which you want to continue routing. Add/Edit Route Mode does not automatically use autoroute algorithms; but you can activate the online DRC if you want. If the online DRC is not active, you can route traces wherever you want—even if it violates design rules. If the online DRC is active, the autorouter functions will automatically add vias or shove traces to prevent major design rule violations.

Edit Segment Mode

The primary purpose of the Edit Segment Mode is to move routed segments and vertices easily. You can also use Edit Segment Mode on unrouted nets on which it behaves similar to the Add/Edit Mode. If you select the center of a routed segment, it moves vertical segments left or right, and it moves horizontal segments up or down. If you select a routed segment's endpoint you can move its vertex. When moving segments, Layout creates angles based on the manual route settings and maintains legal routing patterns. The Edit Segment Mode can also be used to combine (or remove) segments, route unrouted nets, and move vias tied to nets that are not locked.

Interactive manual routing tools

The interactive (semimanual) routing tools—Autopath Route Mode and Shove Track Mode—use the automatic routing algorithms on traces or nets that you select. When you select one of these routing tools the online DRC is automatically activated.

Autopath Route Mode

When you select a completely unrouted net, Autopath Route Mode calculates the best path and suggests what the entire trace should or might look like. A suggested trace is a thin trace of the same color as the active layer. Then, with one click, it autoroutes the trace within the boundaries of the route box. If the trace is already routed and you click on it, it suggests a new routing path depending on where you move your mouse. As you click in various places it temporarily adds vertices or vias and suggests new routing paths until you click in the same spot twice or right click and select Finish from the pop-up menu. Layout then reassesses the proposed routing path and automatically adjusts it for a "best fit" using the routing strategy settings and the push-and-shove capabilities of the autorouter. Since it performs a final "best fit," the final track may end up looking completely different from what it had originally suggested. If you click the End command from the pop-up before completely routing a trace, it stops the autorouter and leaves any unrouted part of the trace as a rat's nest line.

Shove Track Mode

Shove Track Mode is similar to Add/Edit Route Mode except that autorouter is active. The autorouter assumes that the trace you are currently routing has the highest priority and automatically shoves existing traces out of the way. This allows you to force the trace you are working on to be routed in the place of existing traces and at the same time ensures that none of the traces violate design rules. If there are no traces to shove out of the way, the Shove Track Mode behaves like the Add/Edit Route Mode.

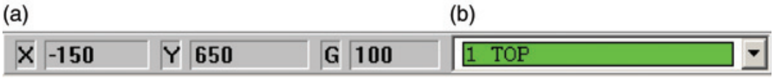
Other indicators and controls

Postage Stamp View

The Postage Stamp View is located in the upper right-hand corner of the Design window and gives you a bird’s eye overview of large boards. The red square represents your monitor, and the yellow outline represents the PCB’s outline. The Postage Stamp View is interactive. If you double click inside of it, it will perform a Zoom All function. If you click once inside of it, it will center the main view at that point. You can also draw a box inside of the postage stamp to zoom in to that area of your board.

Cursor Coordinates and Place Grid Indicators

Below the toolbar are the cursor coordinates and place grid resolution display (Fig. 3-13(a)) and the active layer control dropdown list (Fig. 3-13(b)). The cursor’s coordinates (the default is mils for most boards) are in relation to the board origin. The place grid setting determines how fine your control is when placing your parts. The smaller the grid number the finer the control. You should use the default value for the board technology of your board when possible. If you use a smaller grid setting there is an increased risk of introducing design or manufacturing errors. But there are times when you will need to set a smaller grid (e.g., working with footprints with pins that are not a standard pitch). See Chaps. 5 and 9 for guidelines on grid settings.



X -150 Y 650 G 100

1 TOP

Figure 3-13 Cursor location and grid indicators and layer controls. (a) Cursor coordinates and placement grid. (b) Active layer dropdown list.

The layer control list allows you to select which layer is active so that you can work on it, and it allows you to disable (make invisible) or enable layers. In addition to using the layer control list, each layer has a “hotkey” that you can actuate from the number keys on your keyboard. To see the full list of hotkeys, click on the Spreadsheets tool button and select Layers. You can use one of the hotkeys or the layer control list to select a layer and then use the “-” key to toggle the layer on or off. Another way of controlling layers is by pressing the Color Settings button on the tool bar to bring up the Color Spreadsheet. Left click on a layer cell in the spreadsheet to select it and then right click on it to bring up an edit layer list. From there you can turn a layer on/off, change its color, or even delete it.

Now that you know about the tools for moving parts, and working with obstacles and text, the next task is to learn about the autorouter.

Controlling the autorouter

There are three general types of CAD autorouters: grid-based, shape-based, and topological. OrCAD Layout is a grid-based router (although SmartRoute—an optional add-on to Layout—is a shape-based router). Simply put, grid-based routing characterizes a board space in terms of grid coordinates, starting and ending points (pins) for each net, and locations of obstacles. The grid-based router attempts to route traces on the grid while avoiding obstacles and obeying specific design rules. After routing a trace, the autorouter checks to see if the trace it just routed violates any rules. If any rules are violated it will shove the trace to nearby grid locations and recheck for new violations. If it cannot simply shove the trace without causing violations, it may rip up the trace and try a completely different path. The autorouter will try several iterations of routing, checking, and rerouting until either the trace is legally routed or it gives up. These iterations are called sweeps and passes and are discussed in more detail below.

The design needs for a high-current, power supply board are significantly different from the needs of a low-power, high-frequency (RF or digital) board. The width and spacing of traces, and the number of vias, etc., can significantly affect the power handling ability and cross talk of a board. There are two files that are initially loaded with (copied into) your design that set the routing rules for the autorouter. The two files are the board technology template file (*.TCH) and the strategy file (*.SF). These files are located in the Data folder within the OrCAD/Layout file path. The board technology file, which was discussed above (see Table 3-1), sets the baseline board complexity—the number of allowed layers, the pad sizes, the drill sizes, the trace width and spacing, and units, etc. The strategy file dictates which of the allowed layers are routing layers, how/when to use vias, the general trace requirements (such as direction (horizontal/vertical), colors, etc.), and the routing window size. A default strategy file (STD.SF) is automatically loaded with each new design but can be changed by going to the File → Load dropdown menu and selecting the *.SF file you want. There are 37 different routing strategy files provided with the OrCAD Layout 10.5 Demo version. If you have one of the full versions of Layout with the autoplacement utility (e.g., Layout Plus), there will also be component placement strategy files with the .SF extension, but they will have a file name with a PL prefix (e.g., PLBEST.SF). Autoplacement will not be discussed here, but you can go to the *Layout User’s Guide*, Chap. 9, for more information.

If one of the routing strategy files provided with Layout does not suite your needs you can make your own and load it into your design, or (preferably) you can simply modify the current strategy file settings. You can modify the strategy file settings through the use of three dialog boxes. Access to all three of these dialog boxes is through the Options menu. Specifically:

- Options → System Settings;
- Options → Routing Strategies;
- Options → Route Settings.

There is some overlap between the dialog box controls. An overview of the controls is provided in Table 3-2. You can find more information on routing controls in Chap. 4 of the *Layout User's Guide* under Design Files.

Option	Primary functions
System settings	Units (mils, mm, etc.)
	Grid settings (display, detail, placement, routing, via)
Routing strategies	
Manual route	Via cost
	Retry cost
	Route limit
	Attempts
Route layers	Routing enabled
	Layer cost
	Primary direction
	Routing between pins
Route sweeps	Diagonal routing control
	Sweep direction
	Rote box size
	Route box % overlap
Route passes	Pass status (enabled, done)
	Pass type
	Pass options
	Setting (same as system settings)
Route settings	Route mode
	Interactive autoroute settings
	Manual route settings

Table 3-2 Routing options and controls

Sweeps vs passes

During the autorouter's numerous iterations, it will perform sweeps and passes. The autorouter breaks a board up into smaller areas defined by the Route Box to make it easier for the autorouter algorithm. Sweeps contain the routing objectives that are followed when within a given Route Box. There are seven different sweep types (see Chap. 18 of the *Layout User's Guide* under Sweep Edit Dialog Box and Chap. 20 under Route Sweep Command for details). Various sweep types are executed for each route box. A pass is a routing session that uses a particular routing algorithm while within a given sweep. There are six different algorithms, but not every algorithm is used during a pass (see the *Layout User's Guide*, Chap. 10, under Edit Route Pass Dialog Box, and Chap. E, under Route Pass Command). The type and number of routing algorithms used in each pass depend on the particular routing objectives defined by the sweep. Fortunately, unless you are designing a highly complicated board, the only parameter you will likely need to adjust is the grid settings. But you can adjust the sweep and route settings if you need that much control over your design.

Automatic vs manual routing

If your board has special routing requirements, and you are intimately familiar with those requirements, you can fine-tune the autorouter using different strategy files and the dialog boxes described above. However, a considerable amount of time can be spent setting up the sweeps and passes for a particular board or trace type. In order for fine-tuning to pay off, there needs to be quite a few traces with the same or similar routing requirements (e.g., digital boards with wide data busses). If, however, there are only one or two traces with special requirements, you would probably be ahead by manually prerouting the traces. You can then lock the trace and autoroute the rest of the board using the standard settings. You will see an example of this in Chap. 9 of this book.

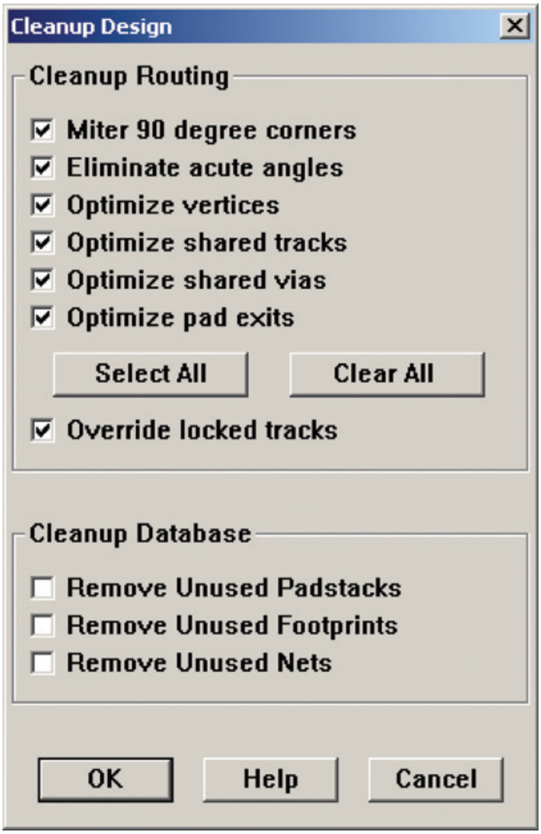
Cleanup

During the routing process some traces or vias do not violate design rules but could present general manufacturing problems. These types of problems include traces with "bad" angles, traces or vias that are off-grid, bad pad exits, and problems with copper areas. The cleanup function checks for these issues and automatically corrects them. It can also be set up to miter corners and clean up the project database of unused padstacks and footprints. A cleanup action can be performed as many times as necessary and at any time during the design process.

To perform a cleanup, select Cleanup Design… from the Auto dropdown menu. The dialog box shown in Fig. 3-14 will pop up. Remember to leave Override locked tracks *unchecked* if you have traces that you want left alone.

Locking traces

To protect a trace from being disturbed during the cleanup or other automatic actions, you can lock the trace by choosing one of the manual routing tools, selecting the trace you want to lock by holding down the Ctrl button on the keyboard and left click on the trace. Next, right click and select Lock from the pop-up menu (also see the *Layout User's Guide,* Chap. 10, Manual Routing Techniques, Locking Routed Tracks). You can unlock a trace using the same basic procedure.



Cleanup Design

Cleanup Routing

☑ Miter 90 degree corners
☑ Eliminate acute angles
☑ Optimize vertices
☑ Optimize shared tracks
☑ Optimize shared vias
☑ Optimize pad exits

☑ Override locked tracks

Cleanup Database

☐ Remove Unused Padstacks
☐ Remove Unused Footprints
☐ Remove Unused Nets

Figure 3-14 The ***Cleanup Design*** *settings dialog box.*

Postprocessing and layer details

Once the board is laid out and routed the board must be postprocessed. The information in the .MAX file is separated into specific data files (Gerber files) that are used by the board manufacturer to make the different parts of your board. Most of the postprocessor files correspond to the layers that you work with in the Layout environment, but some of the files do not. Table 3-3 shows the Gerber files that are generated by the postprocessor. Except for the documentation files listed at the bottom, the files are listed in the order you might see them if you were to cross section a board. Most board manufacturers allow you to specify the order of the inner and plane layers when you order your board.

The key to understanding the connections between the files you use in laying out your board and the files that the postprocessor generates is in understanding how Layout handles and organizes layers. There are six different types of layers that Layout maintains; these are Routing, Plane, Documentation, Drill, Jumper, and Padstack layers (see Chap. C of the *Layout User's Guide* under Edit Layer Dialog Box). There are 17 layer templates (15 plus 2 spares) that are based on the six layer types. The layer templates (also called layer libraries) are

Layer name	Layer nickname	Layer lib name	Layer typer	Postprocess file name	Description
ASYTOP	AST	ASYTOP	Documentation	*your_file*.AST	Top assembly drawing.
SSTOP	SST	SSTOP	Documentation	*your_file*.SST	Top silk screen.
SPTOP	SPT	SPTOP	Documentation	*your_file*.SPT	Top solder paste.
SMTOP	SMT	SMTOP	Documentation	*your_file*.SMT	Top soldermask.
TOP	TOP	TOP	Routing	*your_file*.TOP	Top copper and/or component layer.
POWER	PWR	PLANE	plane	*your_file*.PWR	Power plane.
GND	GND	PLANE	plane	*your_file*.GND	Ground plane.
INNER1	IN1	INNER	Routing	*your_file*.IN1	Inner copper layer 1.
INNER2	IN2	INNER	Routing	*your_file*.IN2	Inner copper layer 2.
…	…	INNER	Routing	…	Inner copper layer ***n***.
INNER12	I12	INNER	Routing	*your_file*.I12	Inner copper layer 12.
BOTTOM	BOT	BOTTOM	Routing	*your_file*.BOT	Bottom copper and/or component layer.
SMBOT	SMB	SMBOT	Documentation	*your_file*.SMB	Bottom soldermask.
SPBOT	SPB	SPBOT	Documentation	*your_file*.SPB	Bottom solder paste.
SSBOT	SSB	SSBOT	Documentation	*your_file*.SSB	Bottom silk screen.
ASYBOT	ASB	ASYBOT	Documentation	*your_file*.ASB	Bottom assembly drawing.
DRILL	DRL	DRILL	Drill	throughole.tap	Drill TAPe file. Describes drill hole sizes and locations (same for RS-274D or RS-274X).

(Continued)

Layer name	Layer nickname	Layer lib name	Layer typer	Postprocess file name	Description
DRLDWG	DRD	DRLDWG	Documentation	*your_file*.DRD	Drill drawing file. An ASCII file indicating drill sizes and ***X*** and ***V*** locations. In RS-274X format, it also contains FAB and APP info.
FABDWG	FAB	COMMENT LAYER	Documentation	*your_file*.FAB	Fabrication drawing. A file that contains board outline co-ordinates (RS-274D and RS-274X) and aperture D-Codes (RS-274X only). All FAB information is also included in the RS-274XDRD file.
NOTES	NOT		Documentation	(none)	Documentation.
		SPARE2		Y*our_file*.lis	Post processor report. An ASCII report file listing layers generated and photoplotting details (same for RS-274D or RS-274X).
		SPARE3		*your_file*.GTD	(GerbTool Database) Gerber design file in either Gerber RS-274D or RS-274X format.
				your_file.DTS	Drill Tape summary report. Provides info on tooling, number of holes, photoplotter info (same for RS-274D or RS-274X).
				your_file.APP	Gerber aperture file (for Gerber RS-274D formate only). For RS-274X, these data are placed into the DRD file.

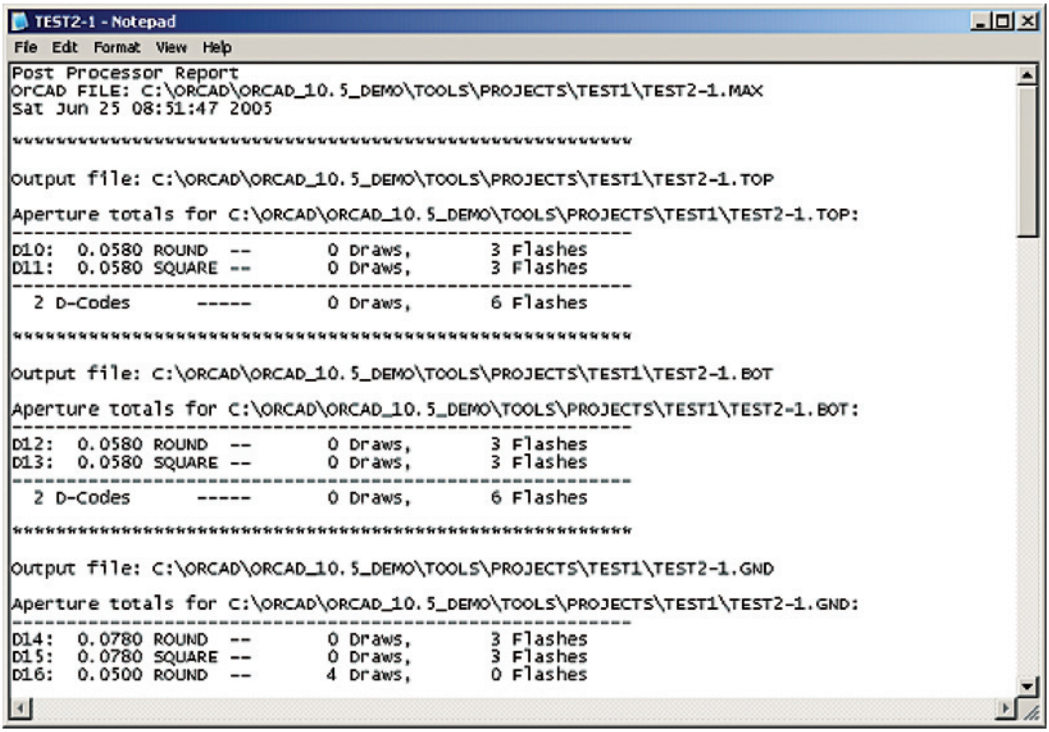
Table 3-3 Gerber and documentation files generated during postprocessing (Continued)

listed in the "Layer lib name" column in Table 3-3. The technology and strategy files provide specific characteristics with regard the general layer types. When you start a new board, a default set of layers (listed in the "Layer name" column in Table 3-3) is automatically created based on these templates; that is, your board's layers inherit their properties from the layer templates. You can modify your board's layers, but the original templates remain unaltered. For example, internal layers are based on the INNER layer template and automatically named incrementally as INNER1, INNER2, etc. (see Chap. C of the *Layout User's Guide*). Each layer you use also has a nickname (listed in the "Layer nickname" column of Table 3-3) that is an alias for the layer name (e.g., IN2 for the 2nd inner layer or I12 for the 12th inner layer). Application-wise, Layout uses the nicknames more so than the layer names themselves. If you look in the Data folder within the Layout directory structure, you will see files with .PPF extensions and names based on the layer nicknames. These are binary database files that define the layer templates. **You should not change the name of a nickname** because Layout will not know what it is since there is not a template for it. However, it is OK to change the layer name and other layer properties to suit the specific needs of your board.

The number and types of files generated by the postprocessor depend on how you set up the postprocessor, which depends on the complexity of your board and the requirements of your board manufacturer. For example, files are generated only for layers that were enabled, and different numbers and types of files are generated depending on the output format that you chose. The two most common types of output formats are RS-274D and RS-274X (a.k.a. Excellon). The Excellon format is typically used, but your board manufacturer should tell you which specific files they need and which format they prefer. The postprocessor is set up from the Post Processor Setting spreadsheet under the Options menu, and we will look at specific settings in Chaps. 9 and 10.

Understanding the documentation files

Some of the terminology used in the PCB fabrication business is left over from the early PCB manufacturing days. Drill tapes and apertures are such terms. Nowadays a drill tape is just an electronic file that describes drill holes and sizes just like any of the other files describes its data (see the "Description" column in Table 3-3). However, originally the drill tape was actually a role of paper or Mylar with holes punched into it that described hole sizes and locations for early computer numerical control (CNC) machines, but it is still called a drill tape today. Here is another example. In Chap. 1, the current technology of photoplotting and laser direct imaging was discussed. In contrast, the older technology used a xenon flash lamp and a shutter to expose photosensitive films or glass plates. The shutter controlled the exposure and an aperture controlled the size of the exposed area. Any shape or drawing could be made by having apertures of different sizes and shapes. Light would be shone through the selected aperture and moved in the $+/-$ x direction, and the film was moved in the $+/-$ y direction. Opening and closing the shutter in one area (to make a pad) was called a flash, while holding the shutter open and moving the light source or film in the x and y directions (to make a trace) was called a draw. The technology today is more advanced, but the concept is the same, and the same terminology is used. Figure 3-15 shows a postprocessor report in which you can



```
Post Processor Report
OrCAD FILE: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TEST1\TEST2-1.MAX
Sat Jun 25 08:51:47 2005

*********************************************************

Output file: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TEST1\TEST2-1.TOP

Aperture totals for C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TEST1\TEST2-1.TOP:
---------------------------------------------------------
D10:  0.0580 ROUND  --       0 Draws,       3 Flashes
D11:  0.0580 SQUARE --       0 Draws,       3 Flashes
---------------------------------------------------------
  2 D-Codes      -----       0 Draws,       6 Flashes

*********************************************************

Output file: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TEST1\TEST2-1.BOT

Aperture totals for C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TEST1\TEST2-1.BOT:
---------------------------------------------------------
D12:  0.0580 ROUND  --       0 Draws,       3 Flashes
D13:  0.0580 SQUARE --       0 Draws,       3 Flashes
---------------------------------------------------------
  2 D-Codes      -----       0 Draws,       6 Flashes

*********************************************************

Output file: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TEST1\TEST2-1.GND

Aperture totals for C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TEST1\TEST2-1.GND:
---------------------------------------------------------
D14:  0.0780 ROUND  --       0 Draws,       3 Flashes
D15:  0.0780 SQUARE --       0 Draws,       3 Flashes
D16:  0.0500 ROUND  --       4 Draws,       0 Flashes
```

Figure 3-15 Postprocessor report.

see the “draws” and “flashes.” You will also notice “D-Codes.” A Gerber D-Code is a just a chronological number that specifies the size and shape of the aperture used on a given layer.

Other tools used with Layout

You should now be familiar with the PCB design flow and Layout tool set. In the following chapters we will look at how to assign footprints to parts from within Capture, how to make your own Capture parts, how to make new footprints using the Library Manager in Layout, and how to set up the Layout environment to route complex boards. After you have mastered those tasks, other tools such as GerbTool and SPECCTRA that interact closely with and enhance the capabilities of Layout will be introduced.

CHAPTER 4

Introduction to Industry Standards

In the previous chapters we looked at how to use the OrCAD tools to design circuit schematics in Capture, route PCBs with Layout, and postprocess the design for fabricating the board. We have not, as of yet, taken a look at how to design the PCB itself. Chapters 4 through 6 provide an introduction to PCB design. Chapter 4 introduces industry standards related to PCB design.

Not every PCB that is manufactured makes it into service. The ratio of the number of PCBs that enter service to the number of PCBs manufactured is called yield (in %). The higher the yield the better because failed boards cost time and money and produce waste. There are several failure points that can be addressed to increase yield. To have high yield we need three things. First the board has to be manufacturable, second it has to perform properly (signal integrity and quality), and third it has to be reliable (it has to work for the full length of its expected life span).

Being manufacturable means two things. The bare board has to be able to be *fabricated* given standard fabrication allowances (SFA) and the board also has to be able to be *assembled*, that is, parts need to be able to be attached to the board with proper solder joints without damaging the parts or the board.

Performance refers to both mechanical and electrical considerations. Mechanically, the board must physically fit into its enclosure and it must be able to handle its environment with respect to ambient temperature, vibration, and humidity. Electrical performance refers to whether it meets the operational design constraints (power, I/O, etc.), is immune to outside interference, and does not cause interference to neighboring equipment.

Being reliable means it meets the above considerations over the expected life of the device. If it is designed correctly it should not fail before the expected end of life unless the user exceeds specified operational design criteria. If the user stays within the operational guidelines and the unit still fails, then there was a bare board defect (a manufacturing defect that was not caused by your design), or there was a circuit or PCB design defect that resulted in a poor assembly process, which resulted in damage to components or board, or the circuit was operating too close to limits, which stressed the system, and failed early due to accelerated stress aging. If reliability problems exist then a failure analysis is conducted and the board is redesigned.

Introduction to the Standards Organizations

When you begin a new PCB design you may be asking: how big and what shape should the board outline be, where should the parts be placed and in what order, what kind of layer stack-up should be used, how wide and far apart should the traces be routed, and what grounding and shielding techniques should be used? Is there a "right" way to do it, and who says so?

There are several standards related to PCB design. The organizations below set standards that may be guides, rules for certification, or even laws. To cover all aspects of these standards would fill an entire book by itself. Some of the standards organizations that you may have heard of or will hear of are listed below with a brief description of who they are and what they do. The discussion in this chapter is limited to the basic standards for PCB design. A listing of applicable design standards is presented in Appendix B.

Institute for Printed Circuits (IPC-Association Connecting Electronics Industries)

The IPC is a global trade association consisting of more than 2300 member companies. It is an organization made up of contributors from industry and includes designers, board manufacturers, assembly companies, suppliers, and original equipment manufacturers. Contributing members bring lessons learned and known good practices to the table, and they document and disseminate the knowledge base through industry-accepted standards. Over the past several years the IPC standards have replaced many of the military standards (MIL-STD) and are sources that you should be familiar with. A list of IPC standards is provided in Appendix B. You can also visit the IPC Web site (www.ipc.org), where you can download a free land pattern viewer.

Electronic Industries Alliance (EIA)

The EIA is a national trade organization comprising over 1000 U.S. manufacturers and high-tech associations and companies. Their primary focus is promoting the market development and competitiveness of the U.S. high-tech industry in the global economy through domestic and international policy efforts. They have influence on design standards set by contributing groups, which include the following:

- CEA—the Consumer Electronics Association
- ECA—the Electronic Components, Assemblies, and Materials Association
- GEIA—the Government Electronics and Information Technology Association
- JEDEC—the JEDEC Solid State Technology Association
- TIA—the Telecommunications Industry Association
- EIF—the Electronic Industries Foundation
- ISA—the Internet Security Alliance

Joint Electron Device Engineering Council (JEDEC)

The JEDEC (now also known as JEDEC Solid State Technology Association) is the semiconductor engineering standardization body of the EIA. It is an association of several hundred organizations that represents all areas of the electronics industry. Its primary focus with regard to PCB design is in standardizing discrete and integrated circuit semiconductor devices and packages. You need to know the package specifications in order to design footprints for your PCB. You can access many of the standards online at http://www.jedec.org. A list of package specifications is provided in Appendix C.

International Engineering Consortium (IEC)

The IEC is a nonprofit organization that works with business and educational communities. It conducts research and reports findings in publications and conferences to address industry opportunities and challenges to aid industry and academia. You can find out more about the IEC (including a free online educational program) at http://www.iec.org.

Military Standards

MIL-STD are maintained by Defense Supply Center Columbus (DSCC), which is a field activity of the Defense Logistics Agency, whose purpose is to provide logistics and contract management support to the U.S. armed forces. The Department of Defense develops and procures an incredible amount of material and engineering services through private contractors. MIL-STD set and communicate standards on how things are to be designed, built, and tested in a controlled, known, and acceptable manner so that everyone who bids on contracts knows exactly what is expected of them, so that they can be successful and competitive. In recent years specialized MIL-STD have been replaced by commercial standards such as IPC standards for PCB design and manufacturing and many other fields of engineering and manufacturing (ASME, etc.). Some of the MIL-STD are becoming obsolete, but new commercial standards are based on and update the old MIL-STD. For example, the newer IPC-2221A PCB standard originated from MIL-STD-275. You can obtain many of the old MIL-STD for free at the DSCC Web site, http://www.dscc.dla.mil/Programs/MilSpec/DocSearch.asp.

American National Standards Institute (ANSI)

The ANSI is a private, nonprofit organization that administers and coordinates voluntary consensus standardization and conformity assessment in the United States. Organizations may become accredited by ANSI, which signifies that their procedures meet ANSI's requirements for due process. There are a couple of PCB and electronic design standards produced through a joint effort between ANSI and other standards organizations (see IEEE below). You can find out more about ANSI at http://www.ansi.org.

Institute of Electrical and Electronics Engineers (IEEE)

The IEEE is a developer of technology standards that are designed to build consensus in an open-based process with input from interested parties. IEEE is a central source of standardization in fields such as telecommunications and power generation.

Examples of IEEE standards related to schematic design and PCB layout include IEEE/ANSI 315-1975, Graphic Symbols for Electrical and Electronics Diagrams, and IEEE-1445-1998, IEEE Standard for Digital Test Interchange Format, respectively. Visit IEEE at http://www.ieee.org.

Classes and Types of PCBs

The design approach for a PCB depends on many factors including its intended end use, design and fabrication complexity, acceptable fabrication allowances, and type of component and attachment technology. Standard classifications have been established to aid designers, fabricators, and consumers in communicating with each other on these issues. The classifications include performance class, producibility level, and type of construction.

Performance classes

PCBs can fall into any of three end-use performance classes. Throughout many of the IPC standards (IPC-7351, Section 1.3; IPC-D-330, Section 1.1.42.6; IPC-CM-770E, Section 1.2.1) material performance and tolerance levels are determined by the class rating. Performance classes are based on things like allowed variation in copper-plating thickness, feature location tolerance, and hole diameter tolerance (plated and unplated), to name a few. The three classes are as follows:

- Class 1, General Electronic Products, includes general consumer products like televisions, electronic games, and personal computers that are not expected to have extended service lives and are not likely to be subjected to extensive test or repairability requirements.
- Class 2, Dedicated-Service Electronic Products, includes commercial and military products that have specific functions such as communications, instrumentation, and sensor systems, from which high performance is expected over a longer period of time. Since these items usually have a higher cost they are usually repairable and must meet stricter testing requirements.
- Class 3, High-Reliability Electronic Products, includes commercial and military equipment that has to be highly reliable under a wide range of environmental conditions. Examples include critical medical equipment and weapons systems. They typically have more stringent test specifications and possess greater environmental robustness and reworkability.

Producibility levels

Producibility levels were introduced in Chap. 3 and are described in more detail here. The levels are not a set of explicit requirements but a way of describing how complex a design is and the precision required to produce the particular features of a PCB or PCB assembly. Smaller features (trace widths, etc.) require stricter tolerances, which increases the design complexity. The IPC standards (IPC-7351, Section 1.3.1; IPC-CM-770E, Section 1.2.2; IPC-D-330, Section 1.1.42.6) provide several tables that assist the designer in determining the complexity as it relates to SFAs. For example, issues such as tolerances for interconnecting lands and conductor width tolerances are described in the standards. The three producibility levels are:

- Level A, general design—preferred complexity
- Level B, moderate design—standard complexity
- Level C, high design—reduced producibility complexity

Fabrication types and assembly subclasses

PCB fabrication types (IPC-CM-770E, Section 1.2.3) are indicated by a number; the higher the number, the greater the sophistication required to make the board. Issues that are related to the fabrication type are the number of copper layers (e.g., single layer, two layer, or multilayer) and the types of vias used to connect the layers, etc. The six fabrication types defined by IPC are:

- Type 1, single-sided printed board
- Type 2, double-sided printed board
- Type 3, multilayer printed board without blind or buried vias
- Type 4, multilayer printed board with blind and/or buried vias
- Type 5, multilayer metal-core printed board without blind or buried vias
- Type 6, multilayer metal-core printed board with blind and/or buried vias

Each PCB type can be further defined by an assembly subclass, which describes how components will be attached to the board (IPC-CM-770E, Section 1.2.2). The subclasses are as follows:

- Subclass A, through-hole devices (THD) only
- Subclass B, surface-mounted devices (SMD) only
- Subclass C, mixed THD and SMD (simple)
- Subclass X, complex THD/SMD, fine pitch, BGA packages
- Subclass Y, complex THD/SMD, ultrafine pitch, chip-scale packaging
- Subclass Z, complex THD/SMD, fine pitch, flip-chip packaging

Typically more sophisticated types and subclasses require stricter tolerances (producibility levels). Higher performance class boards are made more reliable by using stricter producibility levels and lower (easier) fabrication types and assembly classes.

OrCAD Layout design complexity levels—IPC performance classes

Table 4-1 shows the basic PCB characteristics that we will be dealing with in this book. The relationship between IPC classes and Layout's complexity levels is given in Appendix A.

	Class A	**Class B**	**Class C**
Number of Layers	6	12	20
Conductor width			
Internal	12	8	4
External	16	10	4
Conductor spacing	12	8	4
Annular ring			
Internal	8	5	2
External	10	8	5

Table 4-1 Basic PCB characteristics by IPC class

IPC land pattern density levels

The density levels are used to gauge PCB footprint (land pattern) designs with regard to how densely a board can be populated and with regard to the difficulty of trace routing and fabrication. More will discussed in Chap. 5 as to how this relates to footprint design in Layout. The three IPC land pattern density levels (IPC-7351, Section 1.4) are:

- Density Level A, most land protrusion (largest courtyard and least density)
- Density Level B, nominal land protrusion (median courtyard and median density)
- Density Level C, least land protrusion (smallest courtyard and highest density)

Introduction to Standard Fabrication Allowances

No manufacturing process is perfect and they are therefore subject to tolerance limitations. PCB manufacturing is no exception. Design tolerances include drill-hole location and diameter, copper plating and etching, and soldermask resolution, to name a few. Manufacturing tolerance becomes increasingly important as the number of layers increases and line widths and spacing decrease. The tolerance errors can add up at each manufacturing step and result in a scrapped board.

It is important to be aware of manufacturing limitations so that you stay within the boundaries of the manufacturer's capabilities. Industry standards exist to set minimum performance and process guidelines. Individual manufacturer's also have their own capabilities, and you need to be aware of them as well. Just because your design meets certain minimum industry standards does not mean that every manufacturer has the ability to manufacture or assemble the PCB as designed. The following discussion covers the major design issues to look out for and references to the appropriate standards.

Registration tolerances

As described in Chap. 1 (see also Coombs 2001, 17.1.4), many steps and design files are required to fabricate a multilayer PCB. The design parameters in each step have to line up with the next, or misregistration can occur, which can result in manufacturing defects and a non-operational board. One of the PCB's most vulnerable spots is the plated through-hole because it requires accurate alignment of many layers performed over several manufacturing steps.

Breakout and annular ring control

Figure 4-1 shows how fabrication allowances result in a final hole tolerance. Figure 4-1(a) shows the ideal hole, which has a specified diameter and location. Figure 4-1(b) shows the uncertainty of the final hole diameter due to drilling tolerances. Figure 4-1(c) shows the uncertainty of the hole location. Figure 4-1(d) shows the desired hole compared to the possible hole after considering the combined uncertainties. Feature dimensions on each layer of a PCB have uncertainty, which, when combined, can result in a bad board if allowances are not designed into the board.

In addition to hole tolerances, there are also tolerances on trace/land location and size due to plating thickness and variation in etch rate and consistency. The combination of these

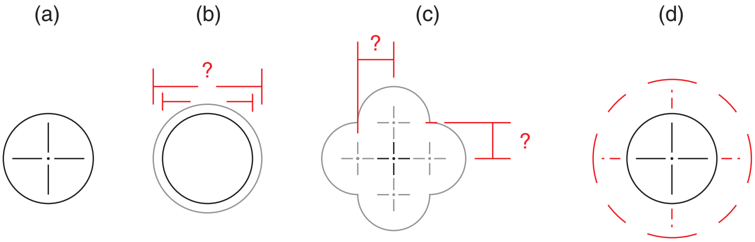


Figure 4-1 Example of fabrication tolerance and dimensional uncertainty.

uncertainties can result in problems such as loss of annular ring control and subsequent land breakout as shown in Fig. 4-2 (Coombs 2001, p. 42.2). Plated through-holes can often function with breakout, but reliability is greatly reduced. By knowing limitations of fabrication processes and following design guides you can greatly reduce the occurrence of defects and increase yield.

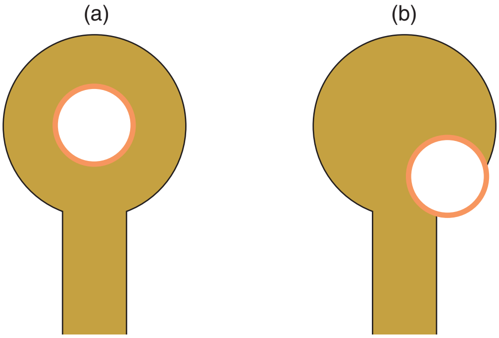


Figure 4-2 Breakout of plated through-hole due to misalignment. (a) Ideal PTH. (b) PTH breakout.

PCB Dimensions and Tolerances

The following sections briefly introduce design limitations that you should be aware of.

Standard panel sizes

There are 16 industry standard board panel sizes (per IPC-D-322 and IPC-2221A, Fig. 1, p. 28). The boards are identified by a letter and a number, which represent the x and y dimensions. Sizes range from A1 to D4 as shown in Table 4-2. An example of a size C2 panel is listed in the table, where C2 is 7.1 × 6.7 in.

Being aware of standard panel sizes may help reduce costs since smaller PCB designs can be panelized onto one large panel. If you have flexibility in specifying the size of your board you can do so in a way that will allow you to maximize the number of boards on one panel. This helps reduce cost by minimizing the number of parts being handled and the amount of waste generated. This is not always an option as PCB size is often driven by design constraints

Letter	Number			
	1	2	3	4
A	2.4 × 3.2	2.4 × 6.7	2.4 × 10.2	2.4 × 13.8
B	4.7 × 3.2	4.7 × 6.7	4.7 × 10.2	4.7 × 13.8
C	7.1 × 3.2	7.1 × 6.7	7.1 × 10.2	7.1 × 13.8
D	9.5 × 3.2	9.5 × 6.7	9.5 × 10.2	9.5 × 13.8

Sizes are given in inches.

Table 4-2 Standard copper clad panel sizes

that are out of your control. Small boards may have to be panelized, though, if they are to be assembled and soldered by automated processes since automated machinery has minimum size limitations (and maximums as well) on the size of PCBs that they can process. We will see in Chap. 11 how to panelize PCB designs using GerbTool.

Tooling area allowances and effective panel usage

When manufacturers make PCBs they need to have an area around the PCB outline to place tooling holes and certain manufacturing data marks. This area is called a tooling area. The required tooling area ranges from 0.375 to 1.5 in. (typically 1.0 in.) as measured from the edge of the board outline to the panel boundary (IPC-D-322). On panelized designs the distance between board outlines is typically 0.1 to 0.5 in. The goal is to utilize as much of a panel as possible without having to go to the next larger size (IPC-D-330 Section 2, Table 2-6, p. 9).

Most of the time these considerations are handled by the board manufacturer and are transparent to the board designer, but being aware of the issues may allow you to optimize the board layout and reduce production costs.

Standard finished PCB thickness

As described in Chap. 1, a PCB is an assembly of one or more cores joined together by sheets of partially cured epoxy (called prepreg). By stacking combinations of various core thicknesses and sheets of prepreg a wide variety of finished board thicknesses can be achieved. Table 4-3

Inches	Mils	Millimeters
0.020	20	0.51
0.030	30	0.76
0.040	40	1.02
0.062	62	1.6
0.093	93	2.4
0.125	125	3.2
0.250	250	6.4
0.500	500	12.7

Table 4-3 Typical finished board thicknesses

lists the typical board thicknesses in the industry. The following sections discuss standard core, prepreg and copper thickness, and tolerances. Unless you are designing controlled impedance PCBs you may not be immediately concerned about the discussion of each of the thicknesses described below. The information is presented here for completeness, and as a reference for the curious and those who are interested in designing controlled impedance PCBs, and can be used when working with Layout's Stackup Editor, which is discussed in Chap. 9.

Core thickness

Cores are made up of substrates (i.e., fully cured laminate epoxy), which are then plated with copper on one or both sides. Table 4-4 shows typical laminate epoxy thicknesses without copper cladding or foil (see also Coombs 2001, Table 5.5, p. 5.12 and IPC-4101, Table 3-7). Copper (foil and plated cladding) thicknesses are described below.

Mils		Millimeters	
Range	**Avg**	**Range**	**Avg**
0.98–4.69	2.8	0.025–0.119	0.072
4.72–6.46	5.6	0.120–0.164	0.142
6.50–11.8	9.1	0.165–0.299	0.232
11.8–19.6	15.7	0.300–0.499	0.400
19.7–30.9	25.3	0.500–0.785	0.643
30.9–40.9	35.9	0.786–1.039	0.913
40.9–65.9	53.4	1.040–1.674	1.357
65.9–101	83.4	1.675–2.564	2.120
101–141	121	2.565–3.579	3.072
141–250	195	3.580–6.350	4.965

Table 4-4 Typical laminate core thicknesses (without copper)

Prepreg thickness

The prepreg that is used to join the plated cores during PCB stack-up comes in sheets of various thicknesses. Table 4-5 shows the various prepreg types and their sheet thicknesses before curing (Coombs 2001, Table 6.3, p. 6.8 and Table 10.2, p. 10.4). Board manufacturers stack up combinations of sheets to obtain the desired board thickness. The actual thickness of a sheet once it is in a board and cured depends on whether it is between plane layers or signal layers, because signal layers tend to sink into the prepreg, which results in a thinner end thickness. The dielectric constant of the prepreg also varies by manufacturer and is discussed in Chap. 6.

Copper thickness for PTHs and vias

Electroless copper plating is used to plate holes to make PTHs and vias. While drilled holes are being plated some of the external surfaces are also plated. The thickness of the plating is

Prepreg type	Thickness range (mils)	(mm)
106	1.5–2.3	0.038–0.058
1080	2.3–3.0	0.058–0.076
2313	3.5–4.0	0.089–0.102
2116	4.5–5.3	0.114–0.135
2165	5.0–6.8	0.127–0.173
2157	5.8–6.5	0.147–0.165
7628	7.0–7.8	0.178–0.198

Table 4-5 Standard prepreg thicknesses

typically 20 to 100 microinches both in the holes and in the surfaces depending on the board manufacturer's processes (IPC-2221A, Table 4-3; Coombs 2001, p. 28.8).

Later in the fabrication process other plating processes are used to "finish" the board. After finishing processes are completed the external surfaces of a PCB can be much thicker, but the wall thickness of a PTH is usually 1 mil or less. Most of the time it does not enter into the drill size calculations unless the hole is very small (most finished hole sizes are 8 mils or larger), but the information is presented here for completeness. Table 4-6 shows the minimum PTH wall thickness as presented in the literature (IPC-2221A, Table 4-3).

	Classes 1 and 2		Class 3	
Minimum thickness	(mils)	(mm)	(mils)	(mm)
Average	0.79	0.020	0.98	0.025
Thin	0.71	0.018	0.79	0.020

Reference: IPC-2221A, Table 4-3 (partial data).

Table 4-6 Minimum electroless plating thicknesses (surfaces and holes)

Copper cladding/foil thickness

When you order your PCB the manufacturer will need to know how thick you want the copper. The thickness of the copper depends on how much current the trace will be required to carry and the required impedance of the traces (for controlled-impedance PCBs). The thickness also plays a role in how narrow the traces can be because thicker copper takes longer to etch and can result in variations in trace width and etchback effects as described below. As mentioned above, various finishing processes (etching and plating) alter the final cladding or foil thickness. The processes are described in detail in the IPC standards and Coombs and are not described here. Table 4-7 shows the copper thicknesses by weight and gauge as described in the literature (Coombs 2001, Table 5.4, ;. 5.11; IPC-D-330, Section 2, Table 2-16; IPC-4101A, Table 1-2, p. 3). The values listed here are for reference only.

Area wt	Nominal thickness		Internal minimum finished thickness		External minimum finished thickness	
(oz/ft^2)	(mils)	(mm)	(mils)	(mm)	(mils)	(mm)
0.148 ($^1/_8$)	0.20	0.005	0.12	0.0031	0.91	0.0231
0.25 ($^1/_4$)[b]	0.34	0.009	0.24	0.0062	1.03	0.0262
0.35 ($^3/_8$)[c]	0.47	0.012	0.37	0.0093	1.15	0.0293
0.50 ($^1/_2$)	0.68	0.017	0.45	0.0114	1.32	0.0334
0.75 ($^3/_4$)	1.01	0.026	0.76	0.0193	1.62	0.0410
1	1.35	0.034	0.98	0.0249	1.89	0.0479
2	2.70	0.069	2.19	0.0557	3.10	0.0787
3	4.05	0.103	3.41	0.0866	4.32	0.110
4	5.40	0.137	4.63	0.118	5.49	0.139
5	6.75	0.171	5.92	0.150	6.32	0.160
6	8.10	0.206	7.13	0.181	7.28	0.185
7	9.45	0.240	8.35	0.212	8.22	0.209
10	13.5	0.343	12.0	0.305	10.9	0.277
14	18.9	0.480	16.9	0.428	14.3	0.364

Table 4-7 Nominal and finished copper thickness by weight and gauge (±10%)

Copper Trace and Etching Tolerances

When copper is etched (instead of milled) the edge of the copper trace is neither a completely smooth nor a vertical wall. The roughness (called the edge definition) occurs because of mask resolution limitations, nonuniformity of the acid circulation, gas bubbles during etching, etc. The wall will have a slight angle to it because as the acid begins to work its way into the exposed copper a sidewall begins to form, which also is attacked by the acid. As Fig. 4-3 shows, the copper near the etch resist begins to be removed under the mask. This effect is called etchback or undercutting. If the etching process is stopped as soon as the last bit of copper cladding or foil is removed from the surface of the board, the trace width at the bottom will be the initial size of the mask width (which is defined by the Gerber files). For this reason the wider value (W, not w′, in the Fig. 4-3) is used for design calculations when trace width dimensions are required.

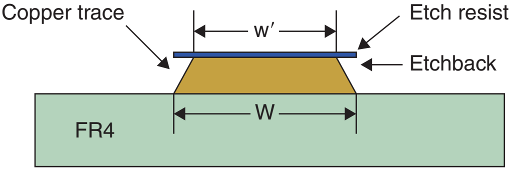


Figure 4-3 Result on finished trace width due to etchback.

Width tolerances are specified in Table 10-3 of IPC-2221A (p. 78) and range from ±4.0 mils to ±0.6 mil for 1½ oz copper depending on reducibility level and plating. The designer should be aware of the width variations when calculating trace widths for controlled impedances and for current handling ability. For general design considerations traces should be made as wide as practical. Per IPC-2221A the minimum trace width and spacing is 3.9 mils. Individual board manufacturers may have their own etching and spacing tolerances. Typical minimum trace widths are 4 to 8 mils. It is a good idea to call and ask what their capabilities are or check their Web sites.

Standard Hole Dimensions

Holes are drilled into PCBs by various techniques including twist bits, router bits, lasers, and plasmas. The capabilities with regard to placement and size accuracy and the speed can vary considerably. But the board designer needs to know what size of drill hole to specify in a padstack. Standard drill bit sizes are specified in ANSI standard B19.11M. However, not all board manufacturers carry every size bit. When you specify a particular hole size manufacturers have different ways of "adjusting" it to fit their capabilities. Some may round (up or down) to the nearest drill size available or they may always round up to the next largest drill bit to make sure that the hole is never too small. This affects annular ring width, which can lead to breakout as described earlier. IPC-D-330 (Section 2, Table 2-4) lists minimum plated through-hole sizes by board thickness and class.

When laminate materials are drilled they become soft due to frictional heating. The softened laminate then smears during the drilling process, which coats the surface of the copper and can prohibit good plating (Coombs, p. 10.7). To solve this problem the laminate inside the hole is etched back after being drilled to desmear the hole. Etchback enhances plating of PTHs (Coombs, p. 48.30), but excessive etchback can cause partial delamination and internal shorts when combined with misregistration and may make the hole larger than requested. This is one reason why adequate clearance is required between the plated through-hole and the ground plane is needed (Coombs, p. 17.9).

After the hole is drilled and desmeared, it is plated. Depending on the manufacturer's plating methods and processes the plating can add as much as 1 mil of thickness on all surfaces, which means that the diameter of the hole could be as much as 2 mils smaller than the specified drill diameter. The padstack drill size in Layout is the actual drill size, not the finished hole size. In most cases the variance in available drill bit size and plating is not a problem. But if your holes are very small and or the lead diameters are very close to the size of the drill hole, the hole variations can cause a lead to not fit into its through-hole. Padstack calculations that account for plating widths and tolerances are described in the next chapter. Another problem that can occur is that if the hole size is very small compared to the thickness of the board the plating process may not be satisfactory. The "proper" hole diameter to PCB width is called the aspect ratio.

Aspect ratio (AR) is the ratio of the plated hole diameter to the PCB thickness. It is recommended that the AR be between 3:1 and 5:1 for Level A boards (IPC-2221A Table 5-1, p. 27; also IPC-CM-770; and IPC-D-330, Table 6-30), with 3:1 being a good target (Coombs, p. 42.3).

The AR for Level B boards is 6:1 to 8:1, and Level C boards may be as high as 9:1 or higher. Check with your board manufacturer to know what their capabilities are because if the aspect ratio is too high, plating problems can occur inside the hole, which can lead to open circuits from incomplete plating and barrel cracking.

Padstack design, which includes all of the issues described above, is covered in detail in Chaps. 5 and 8.

Soldermask Tolerance

Due to photolithography misregistration and swell of the soldermasks, lands can be partially covered. Soldermasks that are patterned on solder-plated lands may be damaged when the solder reflows during soldering operations and can adversely affect solderability. This may be especially troublesome on very small parts (SOT23). To reduce these risks, the soldermask openings are often larger than the lands (oversized). There are two basic categories of soldermask materials: liquid screen printed and photoimageable masks. The recommended oversizing for liquid-screen-printed coatings is 16 to 20 mils, and the recommended oversize of photoimageable masks is 0 to 5 mils (IPC-2221A, 4.5.1.2, p. 24). Many of the Layout footprints have clearances of between 0 and 5 mils. Many fabricators will adjust the soldermask as necessary for their processes. However, some do not and expect (or assume) that you will do it. Check with your board house to find out if they require oversizing and, if so, how much and who they expect to do it.

End Note

Suggested reading

Highly suggested reading for new PCB designers is given below. A more thorough list is given in Appendix B.

1. IPC-2221A, Generic Standard on Printed Board Design (easy reading, ~100 pages, lots of pictures).
2. MIL-STD-275, Printed Wiring for Electronic Equipment (similar to and superceded by IPC-2221A) (*free download*).
3. IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard (easy reading, ~74 pages, lots of pictures).
4. IEEE/ANSI 315-1975, Graphic Symbols for Electrical and Electronics Diagrams.
5. MIL-HDBK-198, Selection and Use of Capacitors (*free download*).
6. MIL-HDBK-199, Selection and Use of Resistors (*free download*).

Other items of interest

1. ASME B18, Series Standards for Mounting Hardware (includes tables for standard screw sizes and recommended drill hole sizes, etc.).
2. MIL-HDBK-5961A, List of Standard Semiconductor Devices (*free download*).

3. ANSI/IPC-D-322, Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes.
4. MIL-HDBK-1861A, Selection and Use of Electrical and Electronic Assemblies, Boards, Cards, and Associated Hardware (*free download*).
5. 47CFR15, FCC Rules on Radio Frequency Devices (including unintentional radiators) (*free download*).

CHAPTER 5

Introduction to Design for Manufacturing

Introduction to PCB Assembly and Soldering Processes

For a PCB to be manufacturable the bare board has to be able to be fabricated within standard fabrication allowances (SFAs), and the board has to be able to be assembled given the different component technologies. As discussed in the previous chapters there are many steps to designing and fabricating a PCB. When a design is complete and submitted to a board house they must be able to perform the manufacturing steps that the design calls for. Whether a PCB is manufacturable or not really begins with and includes parts creation and schematic entry in Capture, padstack and footprint design, parts placement and trace routing, and finally postprocessing in Layout.

But it does not end there. Once the board has been fabricated it is of little use without the functional parts. Those parts need to be able to be attached to the board without them or the board being damaged. Parts attachment encompasses positioning the parts (which depends on proper parts placement and orientation) and making the reliable solder joints between the component's leads and the board's mounting pads (which depends on good padstack and footprint design). This chapter provides the information necessary for padstack and footprint design and component placement for the design of manufacturable PCBs.

Assembly Processes

Printed circuit boards may be manually assembled or assembled by automated machinery. Assembly processes depend on the class of component technology (Classes A through Z as described earlier) and the number of boards to be assembled at one time. Some companies may both fabricate and assemble boards under one roof, while some companies may specialize in PCB fabrication only and others in PCB assembly only. The method of assembly plays a role in how you lay out your PCB because of clearance and orientation issues and soldering processes. A brief summary of assembly processes is given here along with component placement, orientation, and spacing considerations.

Manual assembly processes

Manual assembly is typically used for prototype and low-volume work and in post-automated assembly for odd-form components. Both surface-mount technology (SMT) and through-hole technology (THT) components may be assembled manually. In low-volume work an assembly line of several assemblers may be used, in which each person is responsible for attaching specific components. The assembly processes may be interrupted several times to functionally test sections of the PCB as it is assembled. Manual assembly may involve both manual placement and soldering or a mixture of manual placement and automated soldering (described below).

Manual assembly can be tedious work. Consistent component placement and orientation can aid manual assemblers. For example, orienting polarized components (capacitors and diodes) in the same direction and orienting integrated circuits (ICs) so that pin 1 on all ICs is located in the same direction can significantly reduce assembly defects and increase yield.

Automated assembly processes (pick and place)

Automated insertion processes (pick and place) exist for both through-hole devices and surface-mounted devices, which includes both radial- and axial-leaded devices. Automated machines are programmed to extract parts from reels or bins and place the components on the PCB in the correct location and orientation. Through-hole devices can typically be populated at rates from 20,000 components per hour (CPH) to 40,000 CPH (Coombs 2001, Section 41.2.5, p. 41.10). Programming information for the automated placement machinery can be supplied by the Gerber files (*.AST and *.ASB) generated by Layout and other CAM programs.

Through-hole devices are usually packaged as roles or strips of components, which are taped together by their leads. Through-hole components are usually placed only on the top side of the board so that the leads can be wave soldered and the components themselves are not exposed to molten solder. Soldering processes are described below. The typical automated process steps for through-hole devices is insertion of dual inline packages first, then axial-leaded devices, then radial-leaded devices, and finally odd-form devices. After the components have been inserted, the board is most often wave soldered (wave soldering is described below), but can be reflow soldered (intrusive reflow; see Coombs, p. 43.10), also described below.

Surface-mounted devices are commonly packaged in tubes, matrix trays, tape and reel, and bulk. Surface-mounted devices may be mounted on one or both sides of a PCB. When attached to the top side only, solder paste is screen printed onto the PCB's solder pads. The parts are then placed onto the board by the pick-and-place equipment with the component lead terminations set into the paste, temporarily holding the parts in place. The board is then run through a reflow oven, which melts and then cools the solder, thereby attaching the part to the board. Surface-mounted devices can typically be populated at rates from 10,000 to 100,000 CPH (Coombs 2001, Section 41.3.2, p. 41.15).

When surface-mounted devices are placed on both sides of a PCB or when a board contains both surface and through-hole devices a sequential, reflow–wave soldering process is employed. First the top-side surface-mounted devices are attached to the board using the solder paste and reflow process described below. Next, through-hole devices are inserted from the top and held in place by clinching (bending) the leads on the bottom, by gluing the part to the top, or in some cases by friction between the lead and the hole. The board is flipped over and adhesive dots are applied to the bottom of the board by an automated dispenser. The bottom-mounted surface-mounted devices (SMDs) are then positioned manually or by pick-and-place machines onto the glue dots. The adhesive holds the bottom-side surface-mounted devices in place until the solder joint has been completed. The assembly is run through an oven to cure the adhesive. The board, with through-hole components on the top and SMDs on the top and bottom, is then run through a wave-soldering station, which solders the through-leads and the bottom-mounted SMDs. The previously soldered top-mounted SMDs remain soldered on the top.

When a PCB has only SMDs, but has them on both sides, a two-step reflow soldering process is sometimes used. The top-mounted SMDs are attached to the board first using a high-temperature solder paste, and then the board is run through a high temperature reflow oven. With the top-side components securely in place, the board is flipped over and the bottom-mounted SMDs are attached with the lower temperature paste and reflow process as described below.

Soldering Processes

Soldering is used both to attach components physically to the PCB and to provide electrical conductivity between the component's leads and the PCB traces. For the soldering process to be successful an intermetallic compound, or alloy, must be formed between the solder and the base material (the leads and traces). To protect the solder joint areas from oxidation, contact areas on new PCBs receive a surface finish by being dipped in a solder bath and hot-air solder leveled or are plated by some other plating process such as electroless nickel or palladium (Coombs, p. 32.1). Just prior to or during soldering the surfaces to be joined are cleaned (deoxidized) with flux so that the solder can flow over and wet the surfaces.

There are two general soldering methods: mass soldering (which includes wave, oven reflow, vapor phase reflow, and conduction reflow) and directed energy (which includes hot gas, hot bar, laser, iron, and pinpoint torch) (see Coombs, p. 43.10; IPC-CM-770, p. 34). Only manual, wave soldering, and oven-reflow soldering will be discussed here and only briefly.

Manual soldering

Manual soldering is used for a wide variety of applications from complete PCB assembly to simple repair work and touch-up. There are several types of manual soldering tools available, including but not limited to hot-air pencils, soldering irons, and induction coils. Other than slower soldering speed, the biggest drawbacks to manual soldering are the increased risk of electrostatic discharge during handling and thermal gradients caused by localized heating of the board and parts. Parts placed on the board that will be manually placed and soldered require no special layout consideration as far as spacing and orientation other than the basics described below. However, it is helpful to the assembler if parts placement affords room to work and similar parts are aligned and oriented in a consistent manner as described above.

Wave soldering

During wave soldering the board is held by its edges on a conveyor, fluxed, and preheated as shown in Figs. 5-1 and 5-2. The conveyor moves the board past a standing wave of molten solder so that only the bottom side of the board is exposed to the solder. Wave soldering can be used for both through-hole devices (THDs) and SMDs, but reflow is preferred for SMDs. The through-hole components are placed on the top with the leads protruding out the bottom of board, which is prefluxed. As the conveyer moves the PCB into the solder wave, solder wicks up the barrel and creates fillets on the top and the bottom. SMDs are glued to the board, fluxed, and run through the wave. Very small components or large tantalum caps can be

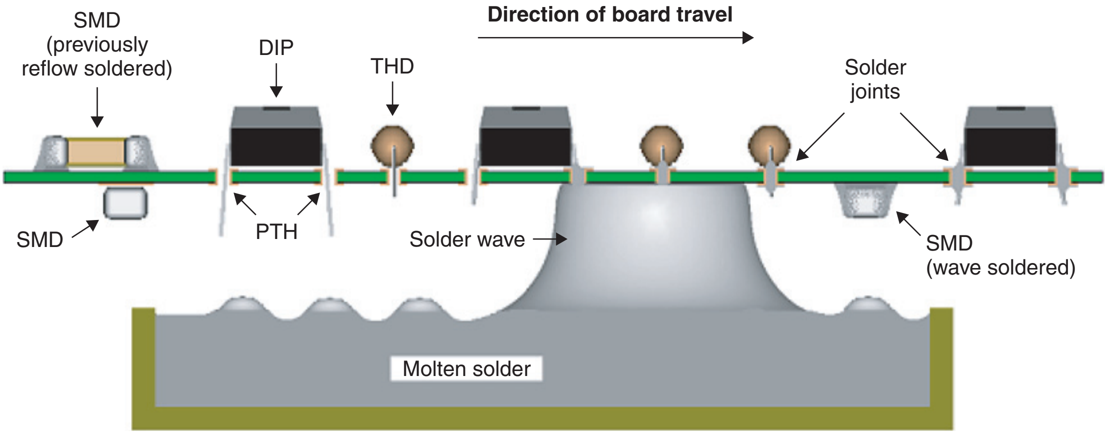

SMD
(previously
reflow soldered)
DIP
THD
Direction of board travel
Solder
joints
SMD
PTH
Solder wave
SMD
(wave soldered)
Molten solder

Figure 5-1 Wave soldering (side view). DIP, dual inline package; PTH, plated through-hole.

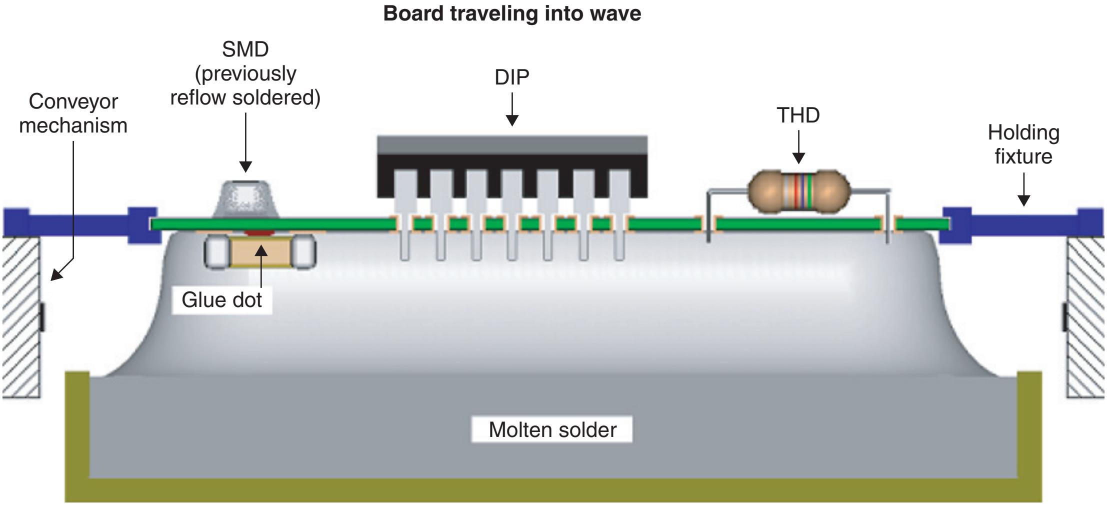

Board traveling into wave
SMD
(previously
reflow soldered)
Conveyor
mechanism
DIP
THD
Holding
fixture
Glue dot
Molten solder

Figure 5-2 Wave soldering (rear view).

problematic with wave soldering. The small parts cause problems during the gluing process because in some cases the glue dot is larger than the component and the glue can ooze over onto the solder pads. Large SMDs cause problems because of thermal stresses that can lead to component cracking.

When surface-mounted devices are wave soldered (i.e., mounted to the bottom side of the board) the designer needs to know (or specify) the direction the board will travel through the wave. The components should be placed on the board as shown in Fig. 5-3 so that smaller parts are not shadowed by larger parts, which can cause poor solder joints on the smaller parts, and so that solder bridging does not occur across the leads.

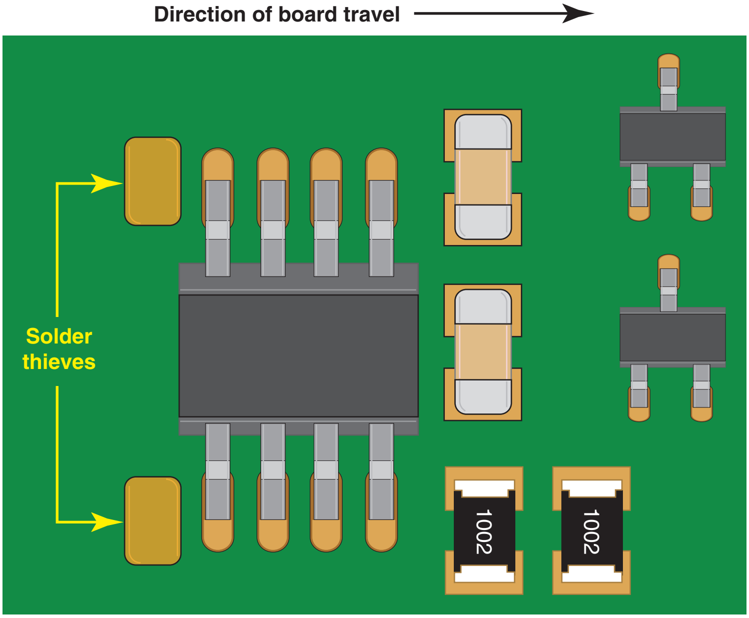


Figure 5-3 SMD component orientation for wave soldering.

Solder bridging can occur because of the fine lead pitch of some SMDs. As each pin leaves the solder wave it tends to draw some of the solder from the pin beside it as the molten solder attempts to reduce its surface tension (for the orientation shown in Fig. 5-3). This causes a problem at the last two rows of pins as there are no pins that follow to draw the excess solder away from them, which can result in the last two pins on a side being bridged by the excess solder. One method to minimize the bridge is to place solder thieves on the trailing edges of SMD ICs as shown in Fig. 5-3. The solder thieves are extra pads placed after the last pads that pull the excess solder away from the pads. Solder thieves can also be made by simply making the last pads a little larger and extending farther back than the typical pads on that device.

If SMD parts are on top of the board and are reflow soldered prior to wave soldering, fan-out vias need to be located away from lands to prevent solder migration away from the SMD lands and down into the via. This can occur as heat conducts from the solder wave up via barrels and re-reflows the solder, which then draws the solder down the via by capillary action. The suggested spacing is ⩾20 mils (IPC-7351, Section3.4.6.2) between the edge of the via and the edge of the pad. The default spacing in Layout is between 50 and 75 mils depending on the settings.

Some boards may be too large or too small to be wave soldered. Large boards sag as they are heated unless special holding fixtures are used. Very small boards may need to be panelized with breakaways (tab routes or V scores) so that they can be handled by automated equipment without having to make specialized board holders. Panelization is demonstrated in Chap. 11.

Reflow soldering

There are various types of reflow soldering, but the discussion here is limited to oven-type reflow soldering. Reflow soldering is most often used for surface-mount devices, but through-hole components can also be soldered this way (called pin-in-paste or intrusive reflow soldering). A schematic diagram of a reflow oven is shown in Fig. 5-4.

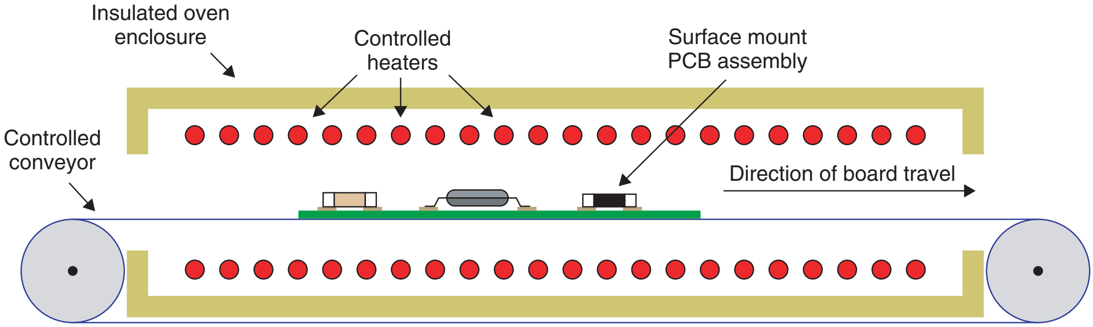


Figure 5-4 Reflow soldering oven (side view).

Solder paste (which contains solder and flux in a viscous paste) is applied to a bare board with a stencil. The components are placed into position (usually by pick-and-place machines) so that the leads sit in the solder paste. The assembly is placed on a conveyor and run through a temperature-controlled oven that heats the boards and parts evenly. As the assembly heats up the flux is activated and the solder reflows (melts). Surface tension of the molten solder tends to self-align the parts. However, if parts are not in proper alignment and thermal gradients do not melt the solder on all pads at the same time, the component may stand up on one end (called tombstoning). Once the assembly has reached the proper temperature and the solder has reflowed, the assembly exits the oven and is cooled to solidify the solder.

Solderable components need to be selected for both wave and reflow soldering. It is also important not to place all of the thermally massive parts in the same area of the board, as this can cause thermal gradients across the board and poor solder joint formation in the cooler areas (Coombs, p. 43.12; for board design see Coombs, p. 43.25).

Component Placement and Orientation Guide

A PCB assembly consists of the bare board, the attached components, and connectors. The board design can have a significant impact on how easily components can be placed on and attached to the board and how reliable the end product is.

The board topology (class and level), the component technology (SMD or through-hole), and the soldering method used to attach the parts (reflow vs wave soldering) play a significant role in how parts should be placed and spaced on the board.

Component placement and orientation depend on the type of component (THT or SMT), the assembly method (manual, wave soldered, or reflow), and the electrical performance requirements (electrical discussed below). These by themselves do not make the board function better but they do make it easier to assemble, inspect, test, and troubleshoot. General guidelines are:

1. Components should be placed so that they are neat and organized with uniform spacing and alignment.
2. Components should be oriented such that component edges are parallel to the board edges (with the exception noted below for wave soldering).
3. If a board is machine soldered, through-hole components should be mounted on a single side that is opposite the solder whenever possible.
4. When placing components on both sides of the board and when mixing through-hole and SMD technologies, keep in mind that multiple assembly phases may be required to place all of the components, which increases cost and potential failure points and makes rework more difficult.
5. Do not put plastic leaded chip carriers (PLCCs) or large tantalum capacitors on the bottom side of board (i.e., do not wave solder them), as they can easily crack due to thermal stresses.
6. A 100-mil (2.5-mm) grid should be used if possible, but a 20-mil (0.5-mm) grid or even 2-mil (0.05-mm) grid can be used if required for component leads that are not on standard grids (IPC-2221A, Section 5.4.2, p. 31 and Section 8.1.2 p. 56). When a metric grid is used, a grid of 2.54 mm (0.100 in.), 1.27 mm (0.05 in.), 0.64 mm (0.025 in.), or 0.50 mm (0.020 in.) should be used (IPC-7351, Section 3.4.1.4, p. 20).
7. A 0.100-in. (2.54-mm) grid should be used for boards that will undergo bed-of-nails testing.
8. Polarized capacitors and diodes should all be oriented consistently throughout the board for ease of inspection and testing.
9. When machine-vision-assisted assembly processes are used, add fiducials (global and local) to aid in component placement.
10. If the design allows, connectors should be placed on the short side of the board when using automated soldering processes.
11. Allow adequate space along board edges during component placement for handling the board and to accommodate mounting hardware.

12. Components that weigh more than 5. 0 g per lead should be mechanically supported if the board will experience vibration (IPC-2221A, Section 5.2.7, p. 29).
13. Thermal management during soldering processes and circuit operation should be considered throughout the design process.
14. Electrical considerations usually have priority over mechanical considerations when there is a conflict between the two, unless it will result in a mechanical failure of the board.
15. For mixed-signal (analog/digital) PCBs, components should be segregated to minimize the effect of switching noise on analog circuits. High-power circuits should also be segregated from low-power and low-noise circuits.

Component Spacing for Through-hole Devices

The following tables provide minimum recommended spacing guidelines for discrete and IC through-hole devices.

Discrete THDs

For discrete THDs, see Tables 5-1 and 5-2.

Integrated circuit through-hole devices

For integrated circuit THDs, see Table 5-3.

Mixed discrete and IC through-hole devices

For mixed discrete and IC THDs, see Table 5-4.

Holes and jumper wires

For holes and jumper wires, see Table 5-5.

Component Spacing for Surface-Mounted Devices

The following tables provide minimum recommended spacing guidelines for discrete and IC surface-mount devices.

Discrete SMDs

See Table 5-6 for discrete SMDs.

Integrated-circuit SMDs

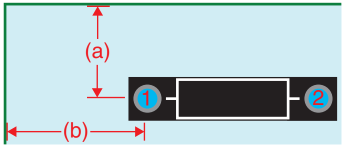
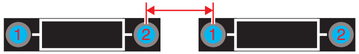
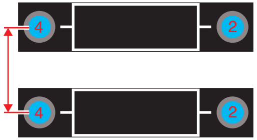
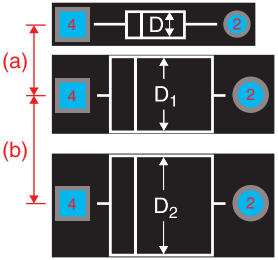
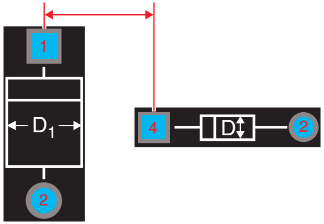
For IC SMDs see Table 5-7.

Mixed discrete and IC SMDs

Use the greater of any of the preceding spacing rules for the components involved.

Mixed THD and SMD Spacing Requirements

Use the greater of any of the preceding spacing rules for the components involved (usually the THT spacing).

Parameter		Mils	Millimeters	Layout default
Side to PCB edge		$a = 75$	$a = 1.9$	Depends on pad to track space setting. No DRC error occurs as long as place outline does not cross the center of the board outline.
End to PCB edge		$b = 90$	$b = 2.29$	
End to end		100	2.54	DRC error occurs if place outlines overlap.
Side to side When body diameters are <100 mils (2.54 mm)		100	2.54	DRC error occurs if place outlines overlap.
Side to side When $D_2 > D_1 > 100$ mils	 4 D 2 (a) 4 D_1 2 (b) 4 D_2 2	$a = 70 + \frac{1}{2}D_1$ $b = 10 + \frac{1}{2}D_1 + \frac{1}{2}D_2$ (*a* and *b* $\geqslant$100 mills minimum)	$a = 1.78 + \frac{1}{2}D_1$ $b = 0.25 + \frac{1}{2}D_1 + \frac{1}{2}D_2$ (*a* and *b* $\geqslant$2.54 mm minimum)	DRC error occurs if place outlines overlap.
Side to end When one or more body diameters are >100 mils		$95 + \frac{1}{2}D_1$	$2.41 + \frac{1}{2}D_1$	DRC error occurs if place outlines overlap.

Reference: IPC-2221A, Fig. 7-1, p. 51.

Table 5-1 Minimum recommended spacing for discrete, axial THDs

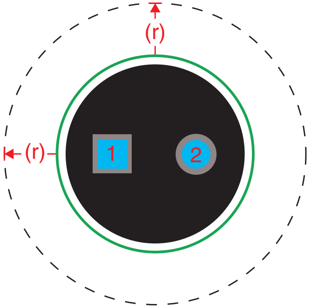
Parameter	Mils	Millimeters	Layout default
PCB edge  	$r = \frac{1}{2}$ the diameter of the device or $\frac{1}{2}$ the height, whichever is greater, AND $r \geqslant 60$ mills (1.52 mm).		No DRC error occurs as long as place outline does not cross the center of the board outline.
Others parts	$r = \frac{1}{2}$ the diameter of the device or $\frac{1}{2}$ the height, whichever is greater.		DRC error occurs if place outlines overlap.

Table 5-2 Minimum recommended spacing for discrete, radial THDs

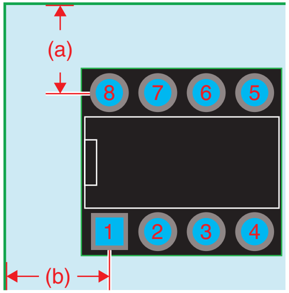
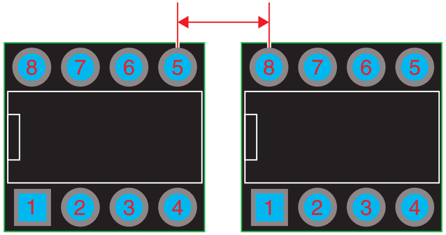
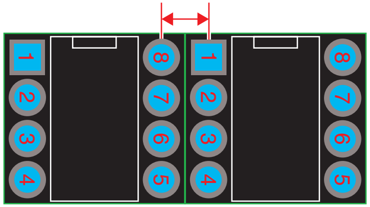
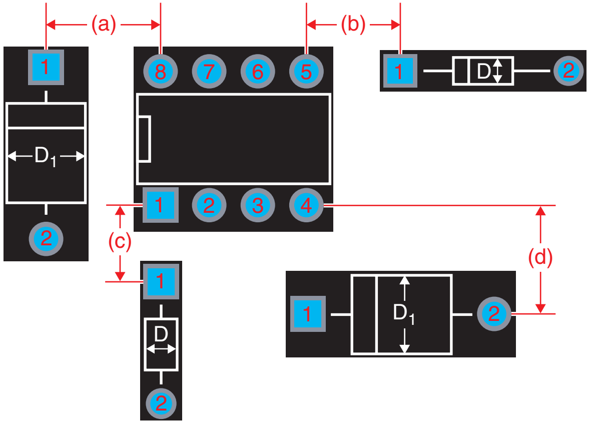
Parameter		Mils	Millimeters	Layout default
Side to PCB edge	 (a) (b) 8 7 6 5 1 2 3 4	$a = 100$	$a = 2.54$	Depends on pad to track spacing setting. No DRC error occurs as long as place outline does not cross the center of the board outline.
End to edge		$b = 75$	$b = 1.91$	
End to end	 8 7 6 5 1 2 3 4 8 7 6 5 1 2 3 4	200	5.08	No DRC error occurs as long as place outlines do not overlap. Could violate IPC standard and not cause DRC error.
Side to side	 1 2 3 4 8 7 6 5 1 2 3 4 8 7 6 5	100	2.54	

Table 5-3 Minimum recommended spacing for through-hole mounted ICs


(a)
(b)
(c)
(d)
D₁
D
D₁
D
1
2
8
7
6
5
1
2
3
4
1
2
1
2
1
2

Parameter	Mils	Millimeters	Layout default
a ($D_1 > 100$)	$115 + \frac{1}{2}D_1$	$2.91 + \frac{1}{2}D_1$	No set rule. DRC error occurs if place outlines overlap.
b ($D < 100$)	200	5.08	
c ($D < 100$)	100	2.54	
d ($D_1 > 100$)	$40 + \frac{1}{2}D_1$	$1.02 + \frac{1}{2}D_1$	

Table 5-4 Minimum recommended spacing between through-hole discretes and ICs

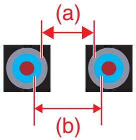
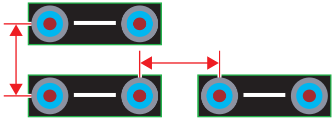
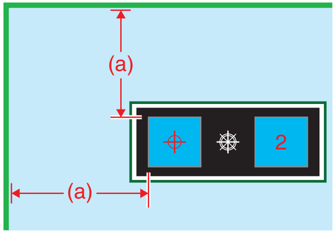
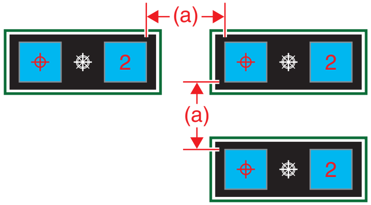
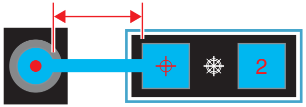
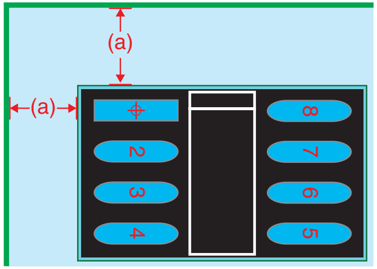
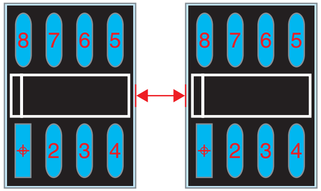
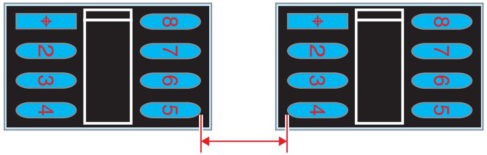
Parameter	Mils	Millimeters	Layout default
Hole to hole (Plated or nonplated) 	(*a*) So as not to violate pad spacing rules. (*b*) So that residual laminate is >20 mils (0. 5 mm) between holes.		DRC error occurs if pad-to-pad spacing rules are violated.
Jumper wires (any direction) 	100	2.54	DRC error occurs if pad-to-pad spacing rules are violated.

Table 5-5 Minimum recommended spacing for holes and jumper wires

Parameter		Mils	Millimeters	Layout DRC
Side to PCB edge and/or end to PCB edge		60	1.5	DRC error occurs if space from pad to edge of board outline is less than pad to track spacing rule or if place outline crosses center of board outline.
End to end and/ or side to side		Size 0603 or larger 20 Smaller than 0603 12	 0.50 0.30	Spacing determined by relationship of place outline to pads and body. DRC error occurs if place outlines overlap. Layout's default pad-to-pad spacing for many footprints is 30 mils (0.76 mm).
Pad to via		20	0.50	DRC error occurs if distance between edge of pads is less than pad-to-pad spacing rule.

References: IPC-2221A, p. 56; IPC-7351, Tables 3-3 to 3-9, Figs. 3-14 and 8-35.

Table 5-6 Minimum recommended spacing for discrete SMDs

Parameter		Mils	Millimeters	Layout default
Component side to PCB edge and/ or end to PCB edge		60	1.5	DRC error occurs if space from pad to edge of board outline is less that pad to track spacing rule or if place outline crosses center of board outline.
End to end (body)	 8 7 6 5 2 3 4 8 7 6 5 2 3 4	20	0.50	Spacing determined by relationship of place outline to pads and body. DRC error occurs if place outlines overlap. Layout's default pad-to-pad spacing for many footprints is 30 mils (0.76 mm).but end-to-end (body) spacing is 0.
Side to side (pad to pad)	 2 3 4 8 7 6 5 2 3 4 8 7 6 5			

References: IPC-2221A, p. 56; IPC-7351, Tables 3-3 to 3-9.

Table 5-7 Minimum recommended spacing for IC SMDs

Footprint and Padstack Design for PCB Manufacturability

Many footprints are included with the Layout software, but you will need to make your own at some point. Chapter 8 describes the Layout tools that are used to design the footprints, and the following describes the design considerations and industry standards related to designing footprints. Footprint design for SMDs and THDs are significantly different, but both require consideration of PCB manufacturability and assembly. A footprint (land pattern) in Layout consists of padstacks, silk-screen obstacles, and a place outline (see Chap. 8 for specifics).

There is no component spacing spreadsheet in Layout as there is a route spacing spreadsheet. The footprint design (the place outline) determines the spacing and therefore the maximum board density possible (without incurring DRC errors). Per the IPC standards there are several spacing recommendations, which are dependent on the board classification and package types. Layout's footprints generally fall within IPC design standards for Level A boards, but were not necessarily designed to a particular producibility level. So if you need to produce a Level C board you will need to modify or make new footprints that fall within the specific guidelines. Or if you want footprints that specifically meet Level A requirements to increase yield and reliability then you may also need to design special footprints or modify existing ones. The following discusses some of the design issues and provides references to the industry standards.

Land Patterns for Surface-Mounted Devices

When you are doing a board layout and need a part that is not in the Layout footprint library there are several things you can do to construct one. If Layout has a footprint that is similar to the one you need, but it has the wrong number of pins, you can save a copy of the existing part with a new name and use it as a pattern to add pins and resize the place outline and silk screen as necessary. If Layout has no footprint that you can use as a pattern, the next step is to check with the manufacturer's data sheet to see if it has a suggested land pattern. If they do not provide the necessary information then you may be able to find the design parameters from the IPC Land Pattern Viewer. If all else fails you will need to design one from scratch using the package information from the component's data sheet or one of the JEDEC package standards.

Component data sheets and the JEDEC package standards provide information about the package dimensions, but not the PCB land pattern, typically. The IPC standards provide guidance on the land pattern dimensions relative to the lead dimensions but does so in a way that requires additional calculations to construct the padstacks and footprints in Layout. When designing footprints in Layout you need to know the size of the padstack and the distances between the centers of the pads. The IPC standards tyically provide spacing information relative to the edges of the pads.

So for convenience, a way of translating the JEDEC package dimensions directly into Layout footprint dimensions while maintaining compliance with IPC standards is needed.

When you look up a part's data sheet the dimensions are usually with regard to the package. An example of an eight-pin small outline integrated circuit (SOIC) is shown in Fig. 5-5. They may also provide the JEDEC specification. Figure 5-6 illustrates an example of JEDEC standard MS-012 for an SOIC package. Fig. 5-6 reprinted with permission of JEDEC.

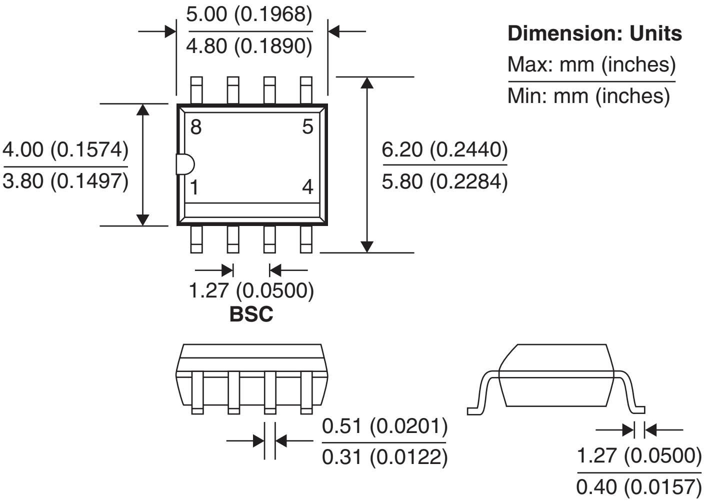
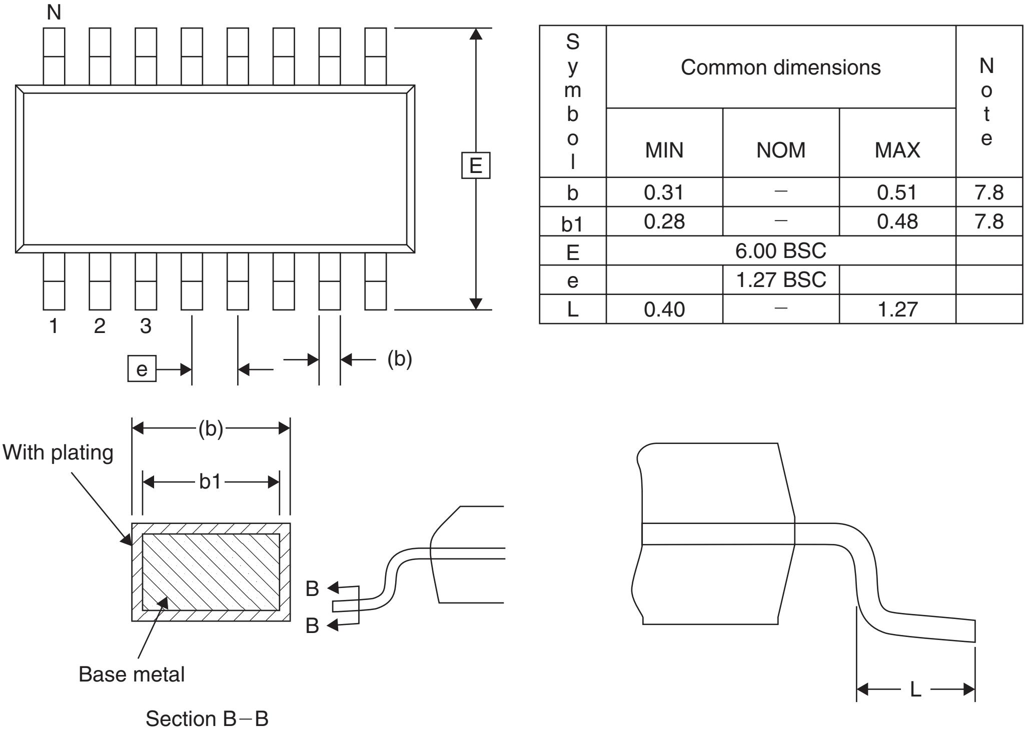

5.00 (0.1968)
4.80 (0.1890)
Dimension: Units
Max: mm (inches)
Min: mm (inches)
8
5
1
4
4.00 (0.1574)
3.80 (0.1497)
6.20 (0.2440)
5.80 (0.2284)
1.27 (0.0500)
BSC
0.51 (0.0201)
0.31 (0.0122)
1.27 (0.0500)
0.40 (0.0157)

Figure 5-5 Data sheet package dimensions (typical convention).


N
E
1
2
3
e
(b)
With plating
(b)
b1
Base metal
B
B
Section B–B
L

Symbol	Common dimensions			Note
	MIN	NOM	MAX	
b	0.31	–	0.51	7.8
b1	0.28	–	0.48	7.8
E	6.00 BSC			
e		1.27 BSC		
L	0.40	–	1.27	

Figure 5-6 JEDEC package dimensions (typical convention).

From the manufacturer's information and/or the standards we need to be able to determine the padstack width and height and the spacing between the pads in both the *x* and the *y* direction as shown in Fig. 5-7, in order to create a new footprint in Layout.

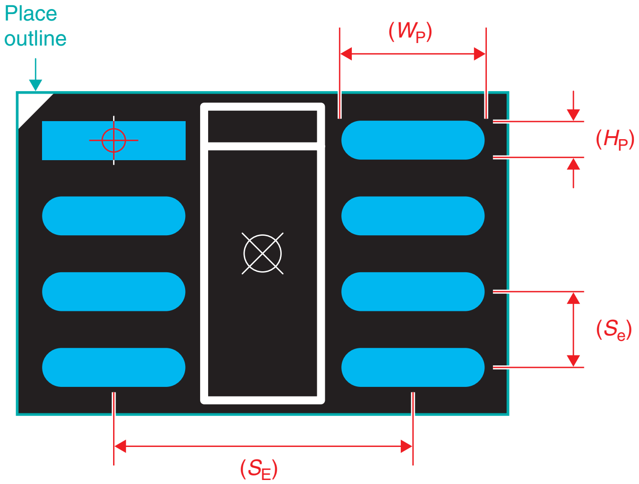


Figure 5-7 Footprint dimensions (typical convention).

We begin by looking at the design of the padstack followed by footprint design using the established padstacks.

SMD padstack design

A good padstack promotes the best possible solder joint between a component termination (lead) and the PCB. The padstack must allow for component dimensional variations, PCB fabrication tolerances, placement tolerances, and solder fillet specifications. Through-hole devices are relatively large and therefore more forgiving of these tolerances, but SMDs are typically much smaller and are therefore more sensitive to manufacturing and placement variations. IPC-7351 (which superceded IPC-SM-780/2) is the standard for surface-mount land pattern design for both padstack and footprint design.

As shown in Fig. 5-8 the solder pad (padstack) needs to be larger than the component lead to allow a proper solder joint. The required pad oversize is defined in IPC-7351 (pp. 8 to 14), where the term J_T defines the distance from the end of the pad to the toe of the lead, J_H defines the distance from the end of the pad to the heel of the lead, and J_S defines the distance from the sides of the pad to the sides of the lead.

The values for J_T, J_H, and J_S depend on the type of component and the desired density level (A through C); nominal values are provided in Tables 5-8, 5-9, and 5-10.

To design a padstack in Layout we need to know the width of the padstack, W_P, and the height of the padstack, H_P, to be able to fill in the required values in the padstack spreadsheet (Fig. 5-9).

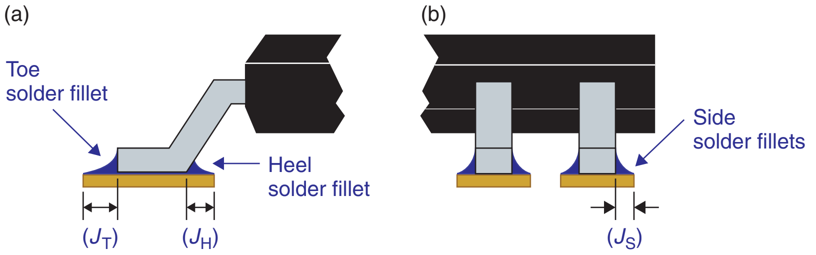


Figure 5-8 SMD padstack requirements. (a) Side view. (b) Toe view.

	Nominal density	
Package type	**Mils**	**Millimeters**
Gull wing (SOG)	14	0.35
J lead (SOJ)	14	0.35
Chip components (0603 and larger)	14	0.35
Chip components (smaller than 0603)	4	0.10
Small outline (SO)	12	0.30
Tantalum capacitors	6	0.15
Leadless chip carrier	22	0.55
MELF	16	0.40
Butt joints	31	0.80

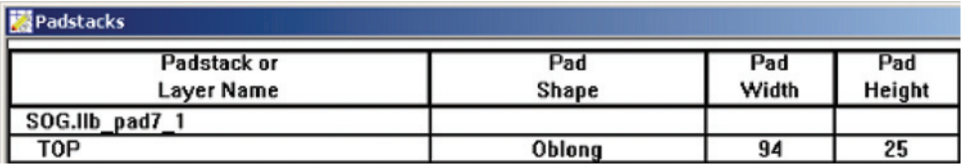
Table 5-8 Nominal toe solder fillet values (J_T) by package type

	Nominal density	
Package type	**Mils**	**Millimeters**
Gull wing (SOG)	14	0.35
J lead (SOJ)	−8	−0.20
Small outline (SO)	0	0.00
Chip components (all)	−2	−0.05
Tantalum capacitors	20	0.50
MELF	4	0.10
Leadless chip carrier	6	0.15
Butt joints	31	0.80

Table 5-9 Nominal heel solder fillet values (J_H) by package type

Package type	Nominal density Mils	 Millimeters
Gull wing (SOG) (pitch greater than 0.625 mm)	1	0.03
J lead (SOJ)	1	0.03
Gull wing (SOG) (pitch less than 0.625 mm)	−1	−0.02
Chip components (0603 and larger)	0	0.00
Chip components (smaller than 0603)	0	0.00
MELF	2	0.05
Small outline (SO)	−2	−0.04
Tantalum capacitors	−2	−0.05
Leadless chip carrier	−2	−0.05
Butt joints	8	0.20

Table 5-10 Nominal side solder fillet values (J_S) by package type



Padstacks

Padstack or Layer Name	Pad Shape	Pad Width	Pad Height
SOG.llb_pad7_1			
TOP	Oblong	94	25

Figure 5-9 Padstack spreadsheet for design

Using the parameters from the component data sheet or the JEDEC standard, Eqs. (1) and (2) can be used to determine maximum sizes for W_P and H_P:

$$W_{P(MAX)} = E_{MIN} - (E_{MAX} - 2L_{MIN}) + 2J_T + 2J_H + 2\sqrt{(E_{TOL(\Delta)})^2 + F^2 + P^2}, \qquad (1)$$

where $W_{P(MAX)}$ is the maximum pad width (see Figs. 5-7 and 5-9); E (MIN and MAX) is the distance between the ends of the leads per the JEDEC dimensions (Fig. 5-6); $E_{TOL(\delta)}$ is the tolerance of E per the JEDEC dimensions or calculated from $(E_{MAX} - E_{MIN})$ (Fig. 5-6); L is the length of the lead that will be soldered to the pad per the JEDEC dimensions (Fig. 5-6); J_T and J_H are solder fillet allowances as described in Tables 5-8 and 5-9, which are derived from IPC-7351; F is the PCB fabrication tolerance (IPC-2221A, Table 10-3, 0. 1 mm or 4 mils typically); and P is the placement tolerance of pick-and-place machines (depends on the machine, 0.15 mm or 6 mils is typical); and

$$H_{P(max)} = b_{MIN} + 2J_S + \sqrt{(b_{TOL(\Delta)})^2 + F^2 + P^2}, \qquad (2)$$

where $H_{P(MAX)}$ is the maximum pad height (see Figs. 5-7 and 5-9), b_{MIN} is the minimum lead width, J_S is the solder fillet allowances as described in Table 5-10, $b_{TOL(\delta)}$ is the tolerance of b

per the JEDEC dimensions or calculated from ($b_{\mathrm{MAX}} - b1_{\mathrm{MIN}}$) (Fig. 5-6), and F and P are as described for Eq. (1).

These equations were derived from various tables in IPC-7351, but the actual standard also includes rounding factors, which are not included in Eqs. (1) and (2). Tables 5-8, 5-9, and 5-10 were also derived from various tables in IPC-7351, but the source standard includes additional data for greater and lesser density levels, while only the nominal density levels are included here. Please see the source for full dimensional considerations or download the IPC land pattern viewer from the IPC Web site (a demo version is available for free).

Once the pad is designed (i.e., you have calculated the width and height), use the procedures given in Chap. 8 to create the pad with the Layout Library Manager.

SMD footprint design

Once the padstacks are designed, they need to be correctly located to complete the footprint design. An example of how IPC-7351 defines land pattern parameters is shown in Fig. 5-10 for an eight-pin SOIC. The component outline defines the outermost boundary of the IC including both the edge of the package and the end of the leads. Next a courtyard is defined around the part that includes the body and the basic land pattern. The courtyard is adjusted outward from the part outline to protrude into and consume PCB real estate. The amount of protrusion (called courtyard excess) determines the minimum separation between components during placement. The greater the courtyard excess the less densely the PCB can be populated. Density levels are categorized by Levels A through C, as listed in Table 5-11 for various SMD packages (from IPC-7351 Tables 3-2 through 3-14).

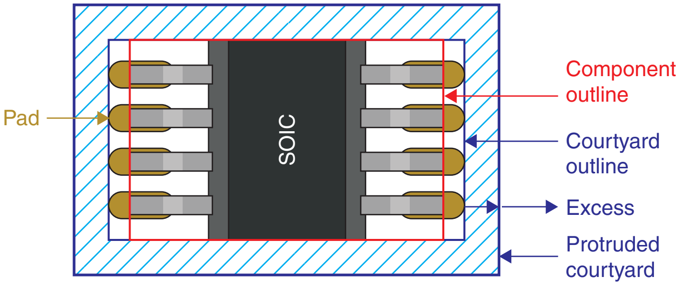


Figure 5-10 IPC-7351 land pattern description of an eight-pin SOIC

Layout uses a concept similar to but not exactly the same as the IPC-7351 land patterns for its SMD footprints. Figure 5-11(a) shows the eight-pin SOIC outlines in Layout overlaid onto the IPC land pattern, and Fig. 5-11(b) shows the actual Layout footprint as seen in the Library Manager. Notice that the Layout place outline does not include the excess at the ends of the body, and the excess beyond the leads may not be the same as the IPC excess.

For most of the Layout footprints included with the software the courtyard excess is 15 mils past the lead ends, which is between Density Levels A and B (see Table 5-11). Presumably

	Density Level A		Density Level B		Density Level C	
Package type	**Mils**	**Millimeters**	**Mils**	**Millimeters**	**Mils**	**Millimeters**
Gull wing (SOG)	20	0.50	10	0.25	4	0.10
J lead (SOJ)	20	0.50	10	0.25	4	0.10
Small outline (SO)	20	0.50	10	0.25	4	0.10
Chip components (0603 and larger)	20	0.50	10	0.25	4	0.10
Tantalum capacitors	20	0.50	10	0.25	4	0.10
MELF	20	0.50	10	0.25	4	0.10
Leadless chip carrier	20	0.50	10	0.25	4	0.10
Chip components (smaller than 0603)	8	0.20	6	0.15	4	0.10
Butt joints	59	1.50	31	0.80	8	0.20

Table 5-11 Courtyard excess (protrusion) by density level for various SMDs

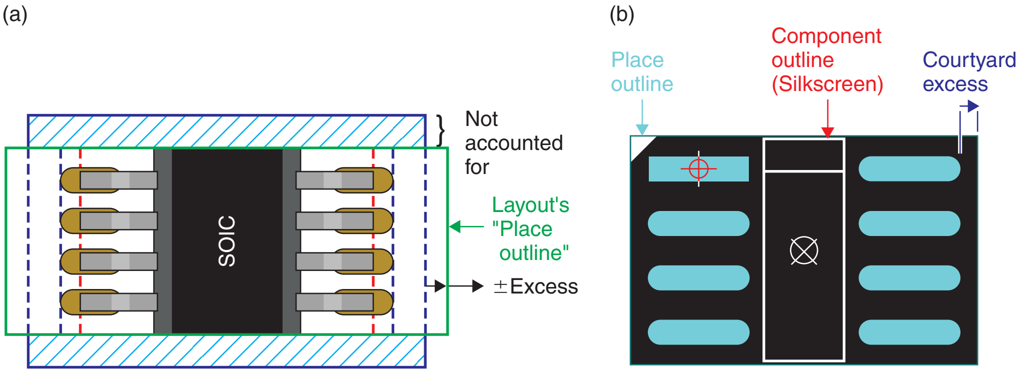


Figure 5-11 Comparison of Layout footprint to IPC land pattern. (a) Layout to IPC outline. (b) Layout's SOIC footprint

this is an artifact of following the earlier IPC standard (IPC-SM-780), which used a general 30 mil spacing rule for surface-mount devices. To make Layout's DRC utility catch spacing violations many of the footprints are made with a 15-mil courtyard excess (15 mils for each component results in 30 mils total spacing). But the DRC will not ensure end-to-end spacing requirements since the Layout footprints do not add an excess past the body boundary (see the component placement discussion below). Additionally, some of the native Layout footprints may not meet Density Level A specifications. But if Level B is acceptable then you can pack them as tight as possible (relative to the place outline) and still have room to spare. If you want to pack the components tighter still (Level C density), then you will have to modify the footprint (the place outline obstacle) to prevent getting DRC errors.

Since there is no component spacing spreadsheet in Layout as there is a route spacing spreadsheet you will have to rely on the footprint design (the place outline obstacle) and the DRC to meet design standards. If the footprint's place outline is not designed to meet design constraints then it is up to the PCB designer to consider component spacing while placing parts on the board. You can use Tables 5-6 and 5-7 as a guide.

Land Patterns for Through-hole Devices

Standardized footprint design for through-hole devices is perhaps not as widely known as the SMD standards. This may be partly because of the greater variety of package styles of the through-hole devices and partly because their typically larger size makes them less sensitive to many of the design and manufacturing issues related to SMDs. As a result land pattern standards or guides for through-hole devices are harder to come by for many devices and may not exist for others. In this section we look at how to design footprints and padstacks for through-hole devices.

Footprint design for through-hole devices

Through-hole devices fall generally into one of two categories: axial-leaded and radial-leaded. An example of a radial-leaded capacitor is shown in Fig. 5-12. The footprint design for this type

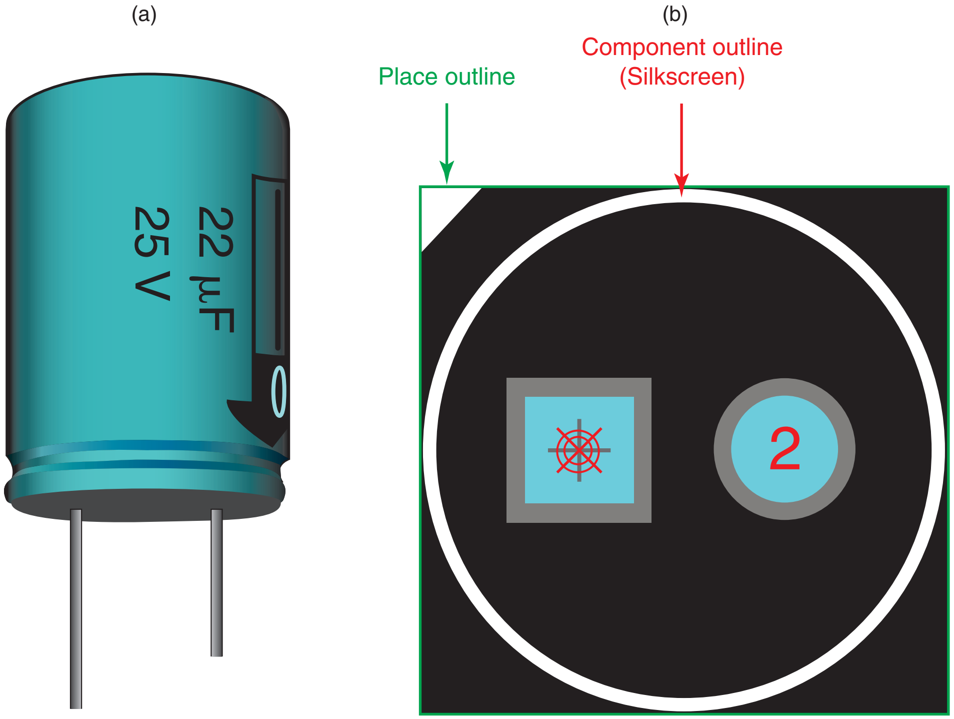


Figure 5-12 Radial-leaded through-hole device. (a) Axial-leaded capacitor. (b) Layout axial footprint

of device is determined strictly by the construction of the device. Clearly the padstacks have to be located where the leads extend from the body. Radial-leaded devices include pin grid arrays and many discrete transistor devices such as TO220 and TO92 packages. The only variable is the padstack design with regard to the lead diameters. Padstack design is described below.

Footprint designs for components with axial leads are highly variable compared to the radial-leaded devices, but the IPC standards (IPC-CM-770, Section 11.1.8, p. 67) and other sources in literature provide general guidance on footprint design. Figure 5-13 illustrates the design parameters for an axial-leaded component (in this case carbon resistor). The location of the padstacks depends on the length of the body and the location of the lead bends (lead form). The minimum required distance between the padstacks is calculated using Eq. (3),

$$L_P = L_B + n \times D_L + 2L_{LE}, \tag{3}$$

where L_P is the pad spacing (center to center), L_B is the length of the body, D_L is the diameter of the leads, L_{LE} is the length of the lead extension from body to bend, and n is an integer allowance for bend radius based on lead diameter per Table 5-12. Padstack calculations are described in the next section. Once this minimum padstack spacing is calculated the padstacks should be placed on the closest standard grid location. Standard grid spacing is described under Component Placement and Orientation Guide. In most cases a 100-mil grid

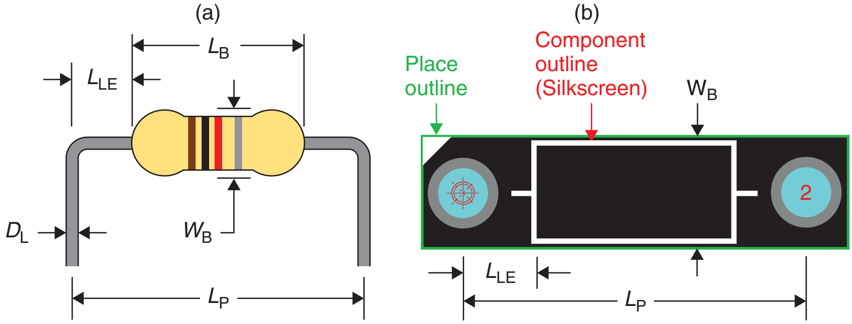


Figure 5-13 Generic footprint design parameters for axial-leaded components. (a) Radial-leaded resistor. (b) Layout radial footprint

Lead diameter	n
$D_L \lesssim 31$ (mils)	3
$D_L \lesssim (0.8\,\text{mm})$	
$31 < D_L \leqslant 47$ (mils)	4
$0.8 < D_L \leqslant 1.2$ (mm)	
$47 < D_L$ (mils)	5
$1.2 < D_L$ (mm)	

Table 5-12 Bend radius factor

is used. The total length of both leads should not exceed 1 in. (25 mm) unless the component is mechanically supported.

Padstack design for through-hole devices

The biggest vulnerability of PCB fabrication is the plated through-hole (PTH) because of registration errors, aspect ratio, plating, etc. The likely failure points are breakout (annular ring control) due to misalignment and opens due to thermal stress and cycling during soldering processes (assembly and rework). But if we follow the standards and fabricator's design guides then we will usually have little trouble.

In designing the PTHs for through-hole components we need to consider the lead-diameter-to-drill-hole relationship, the PCB-thickness-to-drill-hole relationship (aspect ratio), the width of the copper ring around the hole (annular ring), the clearance of plane layers from the PTH, and the capabilities of the board manufacturer (see Figs. 4-1 and 4-2). Both Coombs and the IPC standards are consulted here to define a process for designing PTHs in Layout.

Hole-to-lead ratio

The size of the plated through-hole should be large enough so that the lead can easily slip into the hole, but it should not be so large that it prevents capillary action during soldering operations. There are two methods for determining the required hole size relative to the diameter of the lead that will be soldered into it. The first method is derived from a combination of IPC-2221A (Section 9.1.3, p. 74) and Coombs (Section 42.2.1, p. 42.3). This method takes into account the plating thickness (either assumed or known) and allows the designer to define a tolerance factor. This method produces a clearance between the lead and the PTH that varies with the diameter of the lead. The drill diameter is calculated using Eq. (4),

$$D_H = (D_L + 2T_P) \times k, \tag{4}$$

where D_H is the diameter of the drill hole in Layout, D_L is the diameter of the lead (per the component's data sheet or by measurement), T_P is the thickness of the plating inside the hole (if not known use $T_P = 1$ mil), and k is a user-defined tolerance factor, for which $1.05 < k \leqslant 3.0$ (1.5 is recommended).

As an example, if the diameter of a component lead, D_L, is 32 mils, then the drill hole should be $D_H = (32 + 2 \times 1) \times 1.5 = 51$ mils. With the exception of the variable k, this method is explicit and easy to use. However, as lead diameters become larger the clearance between the lead and the hole becomes wider, and at some point the clearance may become too large for proper capillary action to take place. The point at which this occurs is not well documented in the literature.

The second method is to use a lookup table in which the drill-hole size is dependent on the lead diameter and the desired producibility level (A–C) as shown in Table 5-13 (derived from IPC-2222, Table 9-3, p. 20). So as an example using this method, if we use the same 32-mil lead diameter and the data sheet specifies a 10% tolerance on the lead diameter, then the maximum lead diameter is 35.2 mils and the minimum is 28.8 mils. And if we want a producibility level of A, then the hole diameter would be between 36.2 (35.2 + 10) and 56.8 mils (28.8 + 28).

	Level A		Level B		Level C	
Hole size	**Mils**	**Millimeters**	**Mils**	**Millimeters**	**Mils**	**Millimeters**
Minimum = max lead diameter +	10	0.25	8	0.20	6	0.15
Maximum = min lead diameter +	28	0.70	28	0.70	24	0.60

Table 5-13 Hole-to-lead size relationship by producibility level

If you search the Internet, you can find other algorithms for calculating the "proper" hole-to-lead ratio. Which method you choose is up to you. The two methods here were derived from the IPC standards and other sources, but they are not hard and fast requirements.

PTH land dimension (annular ring width)

Once the size of the drill hole has been determined the next step is to determine the diameter of the pad (also called the land). The difference between the pad diameter and the drill-hole diameter is called the annular ring. This is the copper area where the solder joint is made with the component lead. The larger the pad diameter is, the larger the solder joint will be—to a point. Too large a pad does not necessarily make a better solder joint and only increases the amount of heat required to make the solder joint. Too small a pad can cause a weak solder joint and the pad can be easily damaged by heat or mechanical stress and lift off from the board. The pad diameter recommended by IPC (IPC-2221A, p. 73) is calculated using Eq. (5),

$$D_P = a + 2b + c, \tag{5}$$

where D_P is the pad diameter (see Fig. 5-14), a is the finished hole size ($a = D_H - 2T_P$ from Fig. 5-14), b is the minimum annular ring requirements from Table 5-14 (IPC-2221A, Table 9-2), and c is the standard fabrications allowances from Table 5-15 (IPC-2221A, Table 9-1).

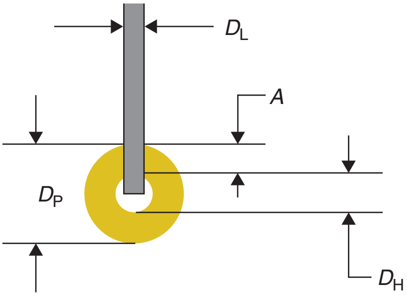


Figure 5-14 PTH design parameters

	Internal	External
Mils	1	2
Millimeters	0.025	0.05

Table 5-14 Annular ring requirements for internal and external rings

	Level A	Level B	Level C
Mils	16	10	8
Millimeters	0.40	0.25	0.20

Table 5-15 SFAs for PTH design

As an example, if we use the 32-mil lead from the example above (using a hole size of 50 mils) and we are calculating the size of an external pad (TOP or BOTTOM in Layout) and we want a Level A producibility level, then the pad size would be $(50 - 2 \times 1) + (2 \times 2) + 16 = 68$ mils.

Clearance between plane layers and PTHs

Plated through-holes and vias typically have lands on all layers even when there is no connection to it on that layer; these are called nonfunctional lands. IPC-2222 (p. 18, section 9.1.4) states that nonfunctional lands should be used on internal layers when possible, but nonfunctional lands are not required on every layer if the board is over 10 layers thick, and they are not required on plane layers. When a via or plated through-hole passes through a plane layer, a minimum amount of space is required between the plane and the plated hole or its nonfunctional land to allow for fabrication allowances, to minimize wicking of plating solution into the laminate from the through-hole (resulting in internal shorts to internal plane layer), and to meet voltage withstanding (insulation) requirements.

IPC-2221A (Section 6.3.1, p. 42) states that the trace-to-trace spacing requirements (see also Table 6-8 in Chap. 6 of this text) apply to the clearance between the plane edge and the PTH or its land. Furthermore, per IPC-2222 (p. 17, Fig. 9-1), the minimum clearance between the plane edge and the edge of internal nonfunctional lands or plated holes is to be a minimum of 10 mils (0.25 mm), that is, the clearance diameter is to be 20 mils (0.51 mm) larger than the drill diameter.

The padstacks in Layout do not contain nonfunctional lands on plane layers, so the clearance diameter should be 20 mils (0.51 mm) larger than the drill diameter (i.e., the edge of the plane should be 10 mils from the edge of the plated through-hole barrel). Most (but not all) of the padstacks in the footprints included with the Layout libraries meet the recommended clearance. Padstacks that are not designed this way may not cause a problem during fabrication or operation of the board. If you find a padstack that does not meet these recommendations, check your board manufacturer's specifications to determine if changes are required.

If the land (pad) is designed per Eq. (5) above and the minimum clearance between the hole and the plane is used, the clearance diameter will typically be several mils larger than the lands. If the lands are larger than the clearance diameter, however, there will be an overlap of the lands and the plane layers as shown in Fig. 5-15, even if the clearance (dimension *d*) meets IPC standards. This should be avoided as there will be capacitive coupling between the

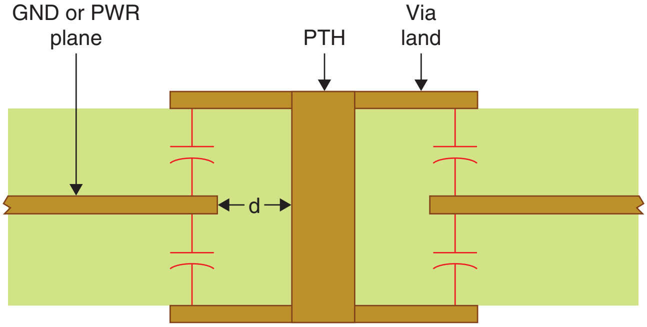


Figure 5-15 PTH or via with oversized lands overlapping plane.

pad and the plane, which can alter the characteristic impedance of the trace and could cause cross-talk problems at high frequencies. Characteristic impedance is described in greater detail in Chap. 6.

Another thing to pay attention to is that the clearance diameter should be no larger than necessary as large slots in the ground (return) plane can result if several pins are close together (as in a board or socket connector), which can cause problems with high-speed digital and high-frequency analog circuits when signal lines pass between the pins. This forces return signals on the ground planes to go around the open slot in the ground plane and increase the loop inductance of the circuit. We will look at loop inductance and ground planes in Chap. 6.

Soldermask and solder paste dimensions

The soldermask opening is typically the same size as the pad (land) diameter in Layout. Board manufacturers sometimes require a particular oversized opening (5 mils is not uncommon). If they do not automatically adjust the size for you then you will need to modify the soldermask opening before you postprocess the PCB design. You can do this at the footprint level or on the PCB itself.

The solder paste dimensions are usually the same size as the external lands (TOP and BOTTOM layers). This is the case with many of the Layout footprints, but some of the footprints do not have a solder paste defined. If you will need the solder paste definitions make sure that they are properly specified for your specific assembly needs.

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CHAPTER 6

PCB Design for Signal Integrity

Desirable electrical characteristics of a circuit and its PCB include low noise, low distortion, low cross talk, and low radiated emissions, to name a few. The purpose of this chapter is to introduce the issues that cause PCB performance problems and how to route the PCB to minimize them and maximize signal integrity.

Circuit Design Issues Not Related to PCB Layout

Circuit design constraints are primarily the responsibility of the circuit design engineer and will not be covered in detail here, but some of the issues will be mentioned briefly since the symptoms of poor circuit design can be confused with PCB design problems.

Noise

Noise generally refers to any signal that interferes with or degrades a signal of interest. It is often used with an adjective for problems, such as phase noise, switching noise, cross-talk noise, and reflection noise. In this text we will limit the term “noise” to mean random or pseudo-random, natural signals, which are generally not a result of the PCB design. Functional problems such as cross talk or ringing (which are PCB-related problems) will be named as such. From this perspective there are two basic categories of noise: background noise and intrinsic component noise. These noise problems are generally addressed by the circuit designer, not the PCB designer, but are discussed here briefly for completeness.

Background noise

Background noise is an uncontrolled signal that originates from the system or environment your board is working in. For example, if your circuit is an audio amplifier that is supposed to amplify a speaker’s voice as he or she speaks into a microphone, but a crowd of people is talking around the speaker or a jet plane flies overhead, both the speaker’s voice and the background sounds will be amplified and the signal would be considered noisy or said to suffer from a low signal-to-noise ratio. There is nothing you can do about it from the PCB design perspective. Sensors may also be noisy because of their sensitivity, but that is also a circuit design issue and needs to be handled long before the PCB is laid out.

Intrinsic noise

There are four basic types of intrinsic noise: thermal noise, shot noise, contact noise, and popcorn noise. Thermal noise (a.k.a. Johnson noise) is due to the motion of electrons in a conducting material. It is present in any material that exhibits a resistance to current flow and is a function of temperature. It is white noise (is constant over frequency) and is prominent in resistors and semiconductor devices. Shot noise is also white noise and is due to potential barriers and is also prevalent in semiconductor devices.

Contact noise (also called excess noise in resistors and $1/f$ noise) is due to imperfect connections at contact junctions or interfaces. It is not constant over frequency and can be fairly large at low frequencies. Your best defense against this type of noise is good quality connectors and good solder joints.

Popcorn noise (also called burst noise) is typically proportional to $1/f^2$ and is worse in high-impedance circuits. It is caused by manufacturing defects in semiconductors and ICs.

Distortion

Distortion is an issue more related to analog circuitry because of the nature of continuous signals. In analog circuitry all voltages between the power supply rails may be of significance. Digital signals are not continuous; they are either HI or LO and usually nothing in between matters. As long as voltage levels meet threshold specifications there is no ambiguity and therefore no quality issues. Ringing on the rising and falling edges of a square wave might be considered distortion, but that is handled differently, as described below. Distortion of a sinusoidal signal (which normally has a single spike on a frequency spectrum) begins to occur in amplifiers as the sine waves either are clipped or experience a phase reversal. Op-amps have amplitude limits imposed by the power supplies, their drive capabilities, and their frequency response. If the amplitude of a sinusoidal output signal (as determined by the input signal times the gain) exceeds the output capability of the op-amp, then the output signal will be clipped off and begin to resemble a square wave. Square waves are composed of many sine waves, which are primarily odd harmonics of the fundamental frequency of the square wave. The dominant harmonic is typically the third one, so as a sine wave begins to clip the onset of third harmonic distortion is observed.

If the input signal exceeds the op-amp's input limits (as imposed by the power supply rails) the output signal will also be distorted. Some amplifiers simply clip the signal (causing third harmonic distortion), while other op-amps experience phase inversion, which also causes harmonic distortion.

These problems are caused by the circuit design and component selection and are not the fault of the PCB design. These effects are mentioned because if you are not used to them or do not know about them they can be confused with PCB layout problems. Along with harmonic distortion ringing will produce unwanted frequency components, which can be seen with a spectrum analyzer and may be confused with other forms of distortion or noise. Ringing is is caused by reflections, which in turn are caused by impedance mismatches on PCB traces which *is* a function of the PCB design.

Frequency response

Both analog and digital circuits have frequency limits. In digital circuitry, if frequency limits are exceeded the signal level may rise and fall before a gate has a chance to switch states. This may give the appearance that the signal is attenuated or that the receiving gate is “not seeing” the signal. This too is a circuit design problem and not a PCB problem. In circuit design we need to make sure that the components selected are within design constraints.

When signals exceed the frequency limits of analog circuitry the output signal will also be attenuated, and distortion will result if the sine wave begins to look like a triangle wave at the output of the frequency-limited component. This is a function of the amplifier’s slew rate, −3 dB BW, and gain bandwidth product. Again these issues need to be handled at the circuit design level, well before the PCB design stage.

Issues Related to PCB Layout

Electromagnetic Interference and Cross Talk

There are three goals in designing PCBs for electrical performance and signal integrity: (1) the PCB should be immune from interference from other systems, (2) it should not produce emissions that cause problems for other systems, and (3) it should demonstrate the desired signal quality. A common factor relating these three issues is electromagnetic waves. As Fig. 6-1 shows, “noise” can be introduced into your PCB from outside sources, and it can produce noise that is radiated to other systems and to itself.

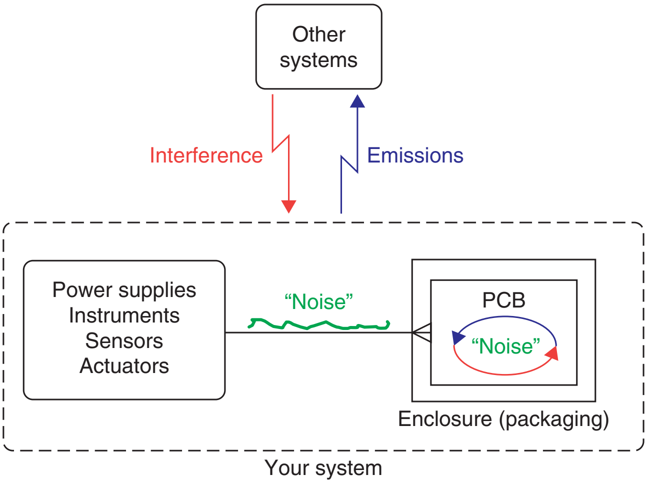


Figure 6-1 The enemy—electromagnetic interference.

When electromagnetic waves get into your system this is referred to as electromagnetic interference (EMI). On the flip side, your PCB can be the source of EMI and cause problems for other systems. The ability for systems to “play nice together” is referred to as electromagnetic compatibility (EMC). The FCC has established rules for many types of systems regarding

EMI and EMC, which, depending on your application, your PCB may have to abide by. Properly laying out your PCB can greatly reduce EMI and improve EMC. In this section we take a look at how to minimize EMI and its effects. There are many good books available that address these issues in greater detail. The material in this chapter is not intended to duplicate those works, but to provide an overview of the issues and provide insight on how to design PCBs with Layout with regard to signal integrity issues.

The method by which systems and circuits can "reach out and touch" another circuit is inductive and capacitive coupling of electromagnetic fields.

In the 1820s Faraday and Henry showed that an electric current could be produced in a conductor by changing the current in another, nearby conductor (Serway, p. 806). And years later Maxwell showed that changing electric fields also produce magnetic fields. These fields are the source of many woes in PCB design. We begin by looking at magnetic fields and inductive coupling.

Magnetic fields and inductive coupling

As shown in Fig. 6-2 a magnetic field vector, **B**, is developed around a conductor when current flows through the conductor, into the "X" end and out of the "Dot" end of the conductor. The right-hand rule (from Ampere's Law) is used to determine the direction of the field: if the thumb of the right hand points in the direction of conventional current flow (movement of positive charges), then the magnetic field curls in the direction of the fingers. This is defined mathematically by a cross product called the Biot-Savart law. By applying some calculus, which will not be shown here, an equation can be derived for the scalar (non-vector) magnitude, *B*, of the magnetic field vector, **B**, near the conductor.

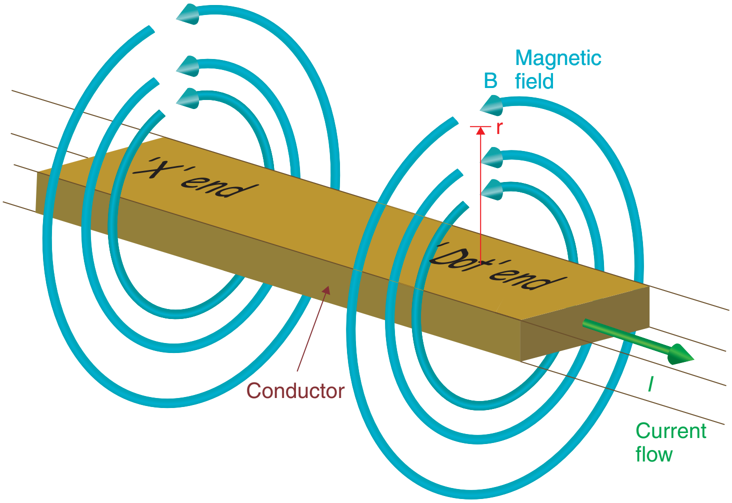


Figure 6-2 Magnetic field caused by a current-carrying conductor.

The magnitude of the magnetic field a distance "r" from a long straight conductor (Serway, p. 838) is given by Eq. (1),

$$B = \frac{\mu_0 I}{2\pi r}, \tag{1}$$

where B is the magnitude of the magnetic field in Wb/m^2, μ_0 is the permeability of free space ($\mu_0 = 4\pi \times 10^{-7}$ Wb/A · m), I is the current in amps (A), and r is the distance from the conductor.

The total magnetic field within or through an area is called magnetic flux, Φ, which has units of Wb and is described by Eq. (2) (Serway, p. 849; Wb/m^2 $\times$ m^2 = Wb),

$$\Phi = BA\cos(\theta), \tag{2}$$

where B is the magnetic field magnitude per unit area (Wb/m^2), A is the area intersected by the magnetic field (m^2), and θ is the angle between B and A.

Magnetic flux expands or contracts in proportion to changes in current flow. As the flux expands or contracts around the conductor, we see from Faraday's Law of Induction, given in Eq. (3) (Serway, p. 877), that a voltage is induced into the conductor. This is known as self-induced electromotive force (emf).

$$E = -\frac{d\Phi}{dt}. \tag{3}$$

The minus sign in Eq. (3) is a result of Lenz's Law, which states that the emf induced into the conductor produces a current in the conductor that creates a magnetic flux that will oppose the changing magnetic flux. This effect is called **self-inductance**. The self-inductance tends to limit how fast the current can change in a conductor. This is what makes an inductor have inductance and oppose AC currents in analog circuits and fast rise times in digital circuits. The magnitude of the inductance, L, is shown in Eq. (4):

$$L = \frac{N\Phi_m}{I}. \tag{4}$$

The inductance is directly proportional to N, the number of turns on a coil ($N = 1$ for a PCB trace and its return path) and the magnetic flux and is inversely proportional to the current, I.

If a secondary conductor is near a primary conductor, which is carrying current as shown in Fig. 6-3, some of the flux will be felt by the secondary conductor. If the current through the primary conductor changes with respect to time (as in the case of a rising edge of a digital signal or an AC signal) the magnetic field (and therefore the magnetic flux) also changes with respect to time as it increases in strength and expands outward (or decreases in strength and contracts inward) from (or toward) the primary conductor.

When the flux that is impinging on the secondary conductor changes with respect to time, as it expands or contracts, we see again from Faraday's Law of Induction, in Eq. (3) that a voltage, E_g, is induced into the secondary conductor. Using the right-hand rule for electric generators the direction of the induced current can be determined. To use the right hand rule point the thumb in the direction of the motion of the conductor (relative to the expanding/shrinking flux—v_C), point the first finger in the direction of the B field, and the middle finger will point in the direction of the force applied to the positive charges ($\mathbf{F}_C^+$) and therefore the positive current flow. The resultant voltage and current are shown in Fig. 6-3. Notice that the current in the secondary conductor flows in the direction opposite that of the current in the primary conductor as a result of the induced voltage. This produces a secondary magnetic field which opposes and partially cancels the primary magnetic field (by Lenz's Law).

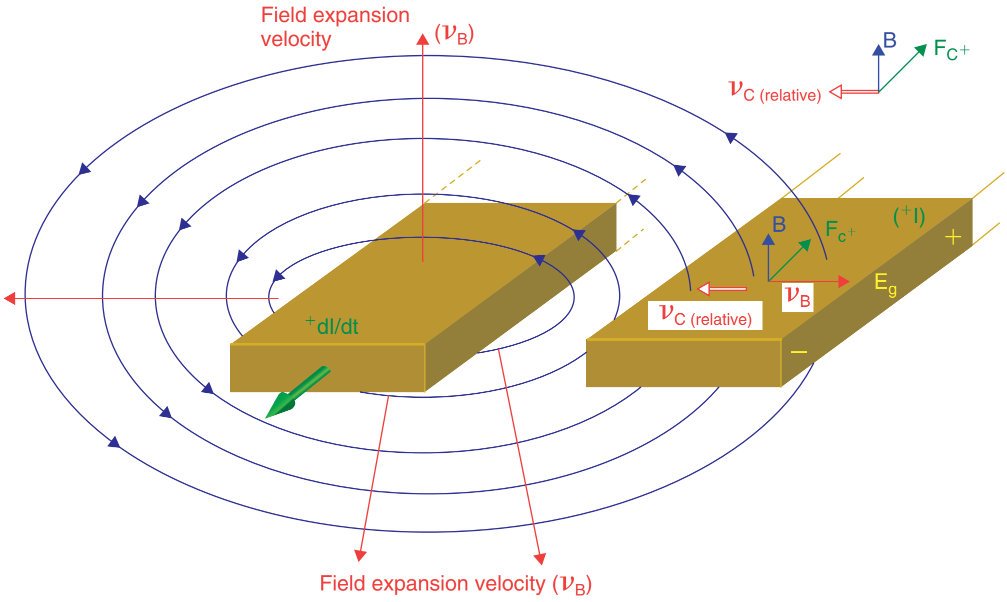


Figure 6-3 Voltage induced into adjacent trace by varying magnetic fields.

If the induced current flow in the secondary conductor is changing with respect to time (which it is because the primary conductor is causing it to) and it is in close proximity to the first conductor (which it is), then the secondary conductor will also induce an emf back into the primary conductor. The magnetic flux that goes back and forth between the two conductors is called **mutual inductance.**

The emf (voltage) generated into the primary conductor (by the secondary conductor) will be in a direction that aids the original current flow in the primary conductor as the secondary flux tries to oppose the primary flux. If the original flux is partially canceled then the self-inductance is also partially canceled and the changing current in the primary conductor is not as limited (i.e., it sees less inductance).

It would seem that unlimited current could flow in the primary inductor since the secondary conductor aids it, but the secondary inductor also experiences its own self-inductance and is therefore limited. Also the amount of mutual inductance between the two conductors is limited by how much of the flux couples the two conductors. This is similar to the coupling coefficient in transformers and in both circumstances is never 100%.

When a trace on a PCB induces a voltage into an adjacent signal trace we call that cross talk, which is bad because it generates noise in the adjacent signal trace. But if the second conductor is the PCB’s ground plane, that is good because it reduces the trace’s inductance and therefore the overall **loop inductance** of the circuit. For the time being we will stick with using the term “return plane,” rather than “ground plane,” for reasons described later.

Loop inductance

In Fig. 6-3 only segments of the traces were shown. Of course for current to flow through the circuit a closed path must exist, as shown in Fig. 6-4. Any conductor in the circuit that carries current will produce a magnetic field as indicated by the circular arrows.

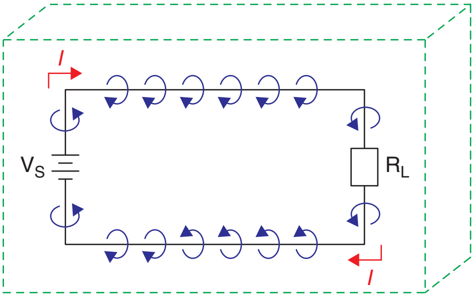


Figure 6-4 Loop inductance of a closed circuit.

An equation for inductance is given in Eq. (5) (Serway, p. 905),

$$L = \mu_0 n^2 A\ell, \tag{5}$$

where n is the number of turns (1), $A\ell$ is the volume that the circuit occupies, and μ_0 is the relative permeability of the material in which the circuit exists. For most materials used in PCBs, $\mu_0 = 1$. So the inductance is a function of the volume of the inductor and the number of turns of the conductor around the space. Therefore, inductance is dependent on the circuit geometry, by which a smaller volume results in a smaller circuit or loop inductance.

If we look at the closed loop circuit shown in Fig. 6-4 with respect to its volume, we can see that if the circuit is physically large and makes a large loop, it will have what is referred to as high loop inductance.

If on the other hand we arrange the circuit as shown in Fig. 6-5, we can see from Eq. (5) that the loop inductance will be less since there is less volume. If you notice the direction of the arrows (the magnetic fields) you can see that the source current and the return current magnetic fields oppose each other, thereby reducing the flux and inductance.

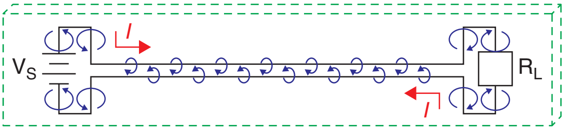


Figure 6-5 Closed loop circuit with low loop inductance.

Figure 6-6(a) shows the resultant magnetic field of two conductors in close proximity where the currents are in the same direction. As indicated the magnetic fields circulate in the same direction and aid each other. This is the case for an inductor in which the turns are wound in the same direction and build up an overall strong magnetic field.

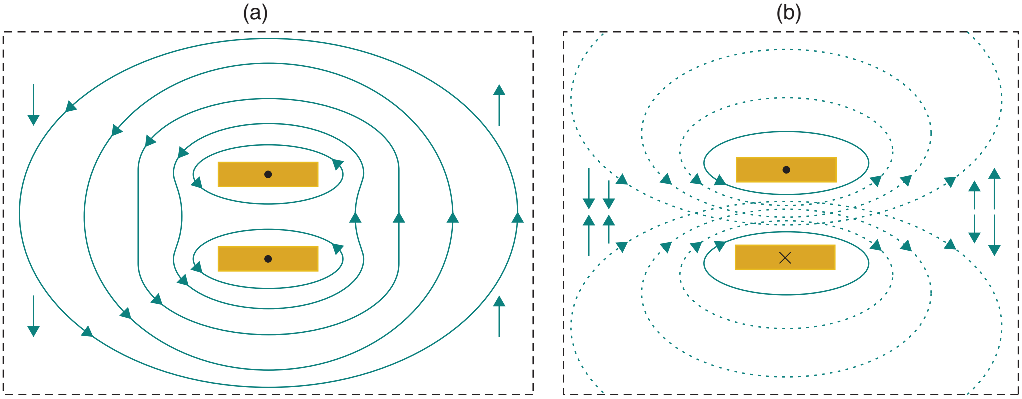


Figure 6-6 Aiding and opposing magnetic fields. (a) Aiding fields. (b) Opposing fields.

Figure 6-6(b) shows the resultant magnetic field when the currents of the two conductors are in opposite directions. The magnetic fields oppose each other and result in partial flux cancellation. The amount of cancellation depends on the amount of mutual inductance, which in turn depends in part on the distance between the conductors.

The situations in Figs. 6-4, 6-5, 6-6(a), and 6-6(b) are steady-state DC circuits, but if we apply the concept in Fig. 6-3 and Eq. (3) for time-varying currents then we can see that, if the return trace on a circuit board is in close proximity to the signal trace, then the inductance of the traces is reduced, that is, the loop inductance of the closed-loop circuit is reduced. If the loop inductance is reduced in an AC circuit, then by Eq. (6) it can be seen that there will be less inductive reactance (X_L), less voltage drop, and less cross talk (fewer EMI problems):

$$X_L = 2\pi f L. \tag{6}$$

To maintain a small X_L (and low loop inductance), we need to have the return path as wide as possible (low self-inductance) and as close as possible to the signal path wherever possible (maximum coupling and small cross-sectional areas). The easiest way to do this is by using a plane layer as the return path. The return plane has historically (and most often inappropriately) been called the ground plane, but it is being referred to more often as an image plane or a return plane. In PCB design a return plane has low inductance (and therefore low self-inductance) and it is everywhere the signal trace is and therefore allows for maximum coupling between the signal trace and the plane for any and all widths of the signal trace.

From this discussion then we can say that one of the most important functions of the return (image) plane is to reduce loop inductance. Reducing loop inductance (and the magnetic fields related to it) provides a low-impedance return path for power and signal lines and reduces unwanted cross talk to nearby conductors. It should also be stated that cross talk between unrelated conductors is also reduced by keeping them farther apart (i.e., r is large).

Electric fields and capacitive coupling

We saw in the previous paragraphs that keeping signal and power lines close to their return paths provides flux cancellation and reduces loop inductance, which is beneficial in all respects. But what happens with the electric fields under these circumstances and what is the effect on the circuit? Figure 6-7(a) shows electric field lines for a single charged conductor, which can represent a signal trace that is a long way away from its return path. Figure 6-7(b) shows electric field lines between two oppositely charged conductors, which can represent a

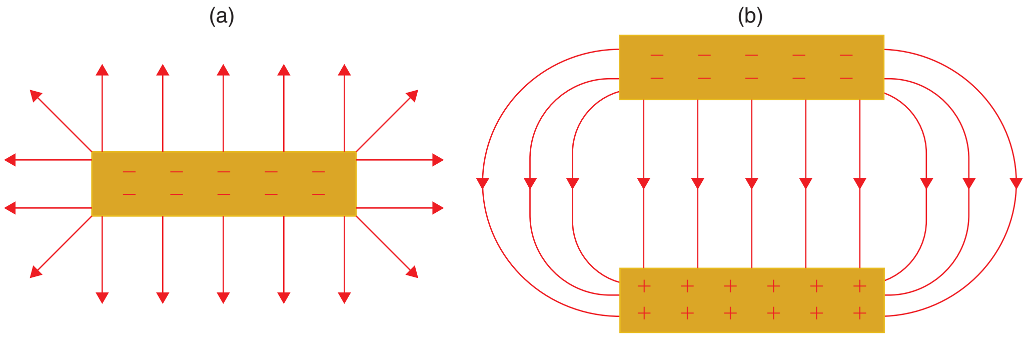


Figure 6-7 Electric fields on conductors. (a) A single charged conductor. (b) A field between oppositely charged conductors.

signal or power line close to its return path. As shown, the solitary conductor radiates electric field lines in all directions, while the coupled conductors contain (or at least concentrate) the electric field between them.

The Ampere–Maxwell Law (Serway, p. 851) states that “magnetic fields are produced both by conduction currents and by changing electric fields.” So, to minimize cross talk, it would seem to be in our best interest not to allow traces to radiate electric fields in an uncontrolled manner but to keep the signal (and power) traces close to their return paths. This is true for both magnetic and electric fields.

But what happens to the capacitance of the traces relative to the return plane when we do this? The equation of a parallel plate capacitor (in farads) in air is given in Eq. (7) (Serway, p. 712),

$$C = \frac{\varepsilon_0 A}{d}, \tag{7}$$

where C is capacitance (in farads), ε_0 is permittivity of free space, A is the area common to the parallel plates, and d is the distance between the plates. As indicated, as the plates become closer together or as the area becomes larger the capacitance increases. This is also holds for the capacitance between a trace and the return plane, although as we will see later the equation is slightly different and the units are in F/in. to make it easier to calculate capacitance for various trace lengths.

From Eq. (8) we can see that as the capacitance, C, increases the capacitive reactance decreases:

$$X_C = \frac{1}{2\pi fC}. \tag{8}$$

By combining Eqs. (7) and (8) as shown in Eq. (9), we can see that by keeping traces and power planes close to their return planes (small d) the capacitive reactance between the trace and the return plane is reduced (coupling is increased):

$$X_C = \frac{d}{2\pi f\varepsilon_0 A}. \tag{9}$$

And by keeping unrelated signal traces farther apart (large d) the reactance between the traces is higher and the coupling (cross talk) is reduced. With both magnetic and electric fields, the wider the return path (the areas of the conductor), the better the coupling, and the closer the signal or power conductor is to the return plane, the better the coupling.

Ground Planes and Ground Bounce

What ground is and what it is not

In the previous discussion, the term "return plane" was used instead of the term "ground plane." Unless the return plane is physically connected to the earth by some means, it really has nothing to do with "ground." The ground symbol, ⏚ has long been used on schematics (in academia and in practice) to indicate a connection to the point to which all closed-circuit currents must return. An example is shown in Fig. 6-8. This gives the impression that ground, somehow, is an omnipresent, unfaltering current sink and equipotential reference. Equipotential means that the voltage is the same everywhere, regardless of how much current is flowing through it. This is a myth.

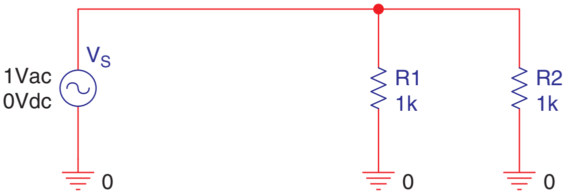


Figure 6-8 Typical depiction of "ground."

Although the depiction of the ground connection shown in Fig. 6-8 is convenient to use on the schematic, in reality there has to be a physical, real-world connection. And, just so you know, the official ground symbols per IEEE Std 315-1975 (ANSI Y32.2-1975) are given in Table 6-1. Symbols and definitions in Table 6-1 reprinted with permission from IEEE Std. 315-1975, Copyright 2003, by IEEE. All rights reserved. The IEEE disclaims any responsibility

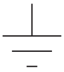
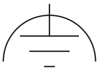
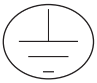
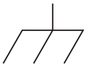
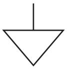
Symbol	Name	Purpose/usage
	Earth GND	A direct connection to the earth. A direct connection to a vehicle's or an airplane's frame that serves the same function as earth ground.
	Noiseless GND	Used to indicate a low or noiseless earth ground.
	Safety GND	Used to indicate a ground connection that serves a safety function against electric shock.
	Chassis GND	A connection to a chassis, or frame, or similar connection of a **printed circuit board** and may be completely different from earth ground.
	Return	Used to indicate common return connections.

Table 6-1 IEEE/ANSI Standard Ground Symbols

or liability resulting from the placement and use in the described manner. However, it is quite common that the ground and return symbols are used otherwise. Since the ground concept has been around a long time it is unlikely that its use will change overnight. The important thing is that it is clear what the symbol means. The standard states that the symbols can be given supplementary information (such as names) on the schematic to specifically annotate the symbol's purpose or function.

There are two basic ground and power connection schemes, parallel and series connections, as shown in Fig. 6-9. A parallel ground system is shown in Fig. 6-9(a). A parallel ground system is also called a separate ground system, since the current flow in each branch is supplied by and returns to the source through completely separate paths. A series connected ground system is shown in Fig. 6-9(b). The series connected ground system is also referred to as a common ground system or daisy chain, since the current flows in the two branches share a common path.

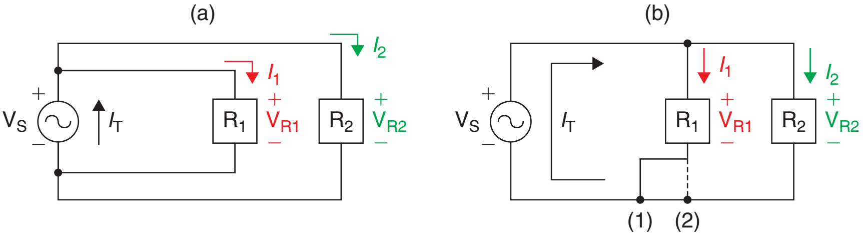


Figure 6-9 Typical signal and return connection schemes. (a) Parallel connected. (b) Series connected.

At the schematic level the circuits in Fig. 6-9 are identical; mathematically the circuits are also identical, that is, $I_T = I_1 + I_2$ and $V_{R1} = V_{R2} = V_S$. Furthermore, as indicated in Fig. 6-9(b), you could connect R_1 to the common return path at either point (1) or point (2) without changing the meaning of the circuit description in any way. However, on the PCB, the two circuits shown in Fig. 6-9 can be significantly different. There may even be significant differences between points (1) and (2) in Fig. 6-9(b).

It was said earlier that any conductor that carries current will produce a magnetic field. Even if there is very tight coupling between the signal conductor and its return conductor, some inductance will always exist because the coupling is not 100.0% complete; that is, there is less than perfect mutual inductance from the primary trace to the secondary trace (the return plane) and from the secondary trace back to the primary trace.

With this understanding we can see from Fig. 6-10 that there is an "unseen" schematic within the PCB. As a result, although the relationship $I_T = I_1 + I_2$ is still true, it should be realized that $V_{R1} = V_{R2} = V_S$ is no longer true, because there are voltage drops along the shared and individual impedances between the source and each of the loads. Furthermore points (1) and (2) and any other points along the return path are not equipotential. The ideal, equipotential ground plane does not exist in practice.

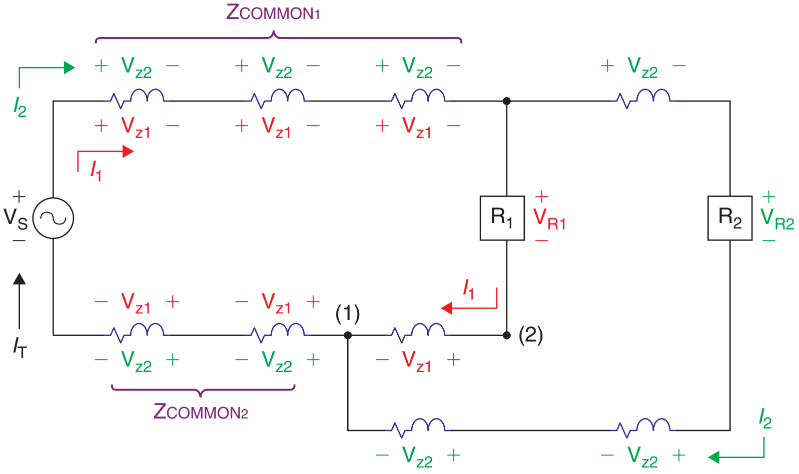

ZCOMMON1
+ Vz2 −
+ Vz1 −
I2
I1
+
VS
−
IT
R1
+
VR1
−
R2
+
VR2
−
− Vz1 +
− Vz2 +
(1)
(2)
ZCOMMON2
I2

Figure 6-10 The actual circuit—the hidden schematic.

Common impedance is particularly troublesome when high-power or noisy signals share common return paths ($Z_{COMMON1}$ and $Z_{COMMON2}$) with low-power signals. High-speed digital signals operating near low-level analog signals are an example.

Clearly then, it would seem that the best return system is the parallel system shown in Fig. 6-9(a). However, a potential problem rises when we try to implement this approach on the PCB. Figure 6-11 shows the routing scenarios in which Fig. 6-11(a) is the parallel connection and Fig. 6-11(b) is the series connection. As described above and shown in Fig. 6-11(a) the current paths do not interfere with each other in the parallel connection since their paths are completely separate, and since each signal path is directly above its return path, there is tight

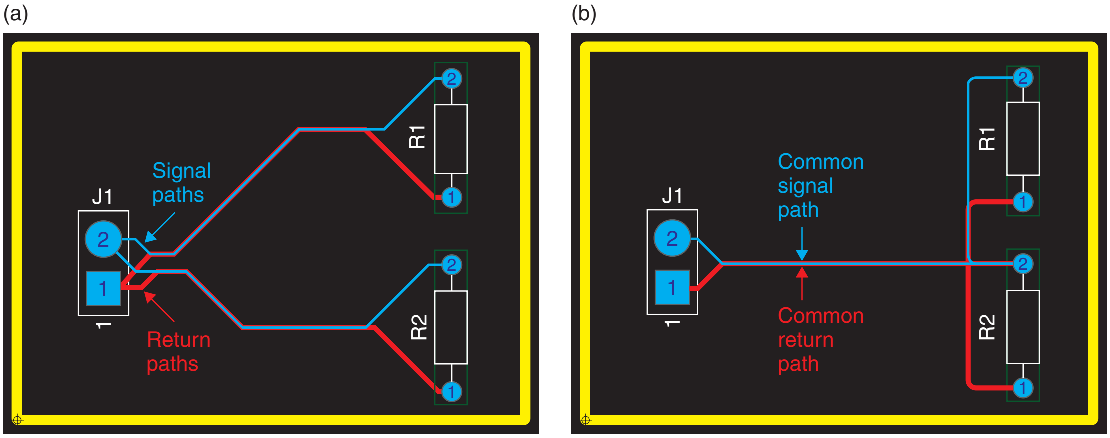

(a)
J1
2
1
Signal paths
Return paths
R1
R2
(b)
Common signal path
Common return path

Figure 6-11 Signal and return connection schemes in Layout. (a) Parallel (separate) connected. (b) Series (common) connected.

coupling between the signal and the return and therefore the inductance is minimized. The problem is that it would become incredibly cumbersome to route a PCB using this approach with even a few additional components and worse on a high-density, multilayer PCB. If components are moved, movement of the signal and return paths would have to be carefully coordinated, resulting in many opportunities for routing "errors" that could be difficult to detect with an automatic design rule check.

The series connection in Fig. 6-11(b) is obviously much easier to route, but it loses the benefit of the separate signal and return paths. Even with the signal and return paths tightly coupled, the common paths (impedances) could be problematic for circuits operating at high frequency or with fast rise times.

Ground (return) planes

Above, we said that we want the return path to be as wide as possible and as "everywhere" as possible, which, when taken to the extreme, causes the return path to become a plane. But since (at first glance) it appears that a plane is potentially a common return path (a common impedance), the question arises as to if this is really the best solution to overcome the inconvenience of the routing problem. If we reroute the circuit of Fig. 6-8 as shown in Fig. 6-12, in which the return path is the GND plane in Layout (where the thermal reliefs indicate a connection to the GND plane), we can analyze the situation. If the signal path is relatively close to the return path, the return signal will automatically flow through the GND plane directly below the signal trace. The reason this happens is that by doing so the loop inductance of the circuit is minimized. As is commonly known in DC circuits, current follows the path of least resistance. Perhaps not as commonly known, AC currents will follow the path of least impedance and, particularly on PCBs, the path of least inductance. The only way for that to happen is if the return current travels directly under the signal trace on its way back to

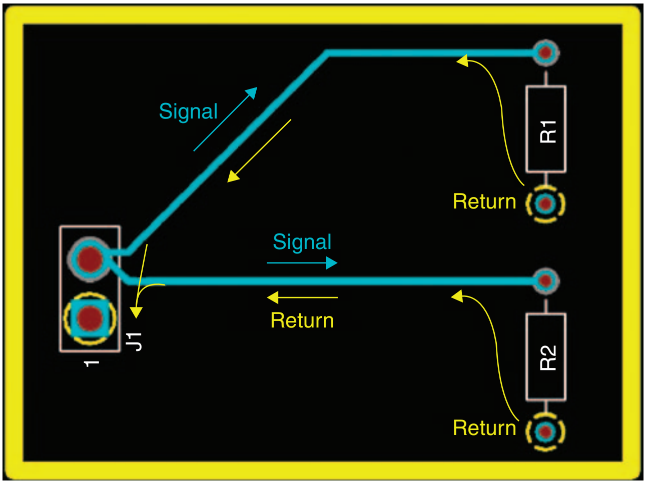


Figure 6-12 Pseudo-common return path using a "ground" plane.

the source. This is true no matter what kind of crazy path the signal trace makes, as long as no discontinuities exist in the return plane.

So (in Fig. 6-12) even if R_2 was directly between R_1 and the PCB connector the return paths would not be common as long as the signal traces to R_1 and R_2 did not overlap (which can happen if the signal traces were routed on different layers) or become "too" close. We will look at the appropriate trace separation (what "too close" means) in the routing section discussed later.

Ground bounce and rail collapse

In a typical PCB the power distribution system contains one or more power and ground planes. The power and ground planes are like very wide traces (have little inductance) and are usually adjacent to each other (high capacitance). This is exactly what we want for the power distribution system. However, despite these advantages, a problem occurs in high-speed digital systems when gates switch from one state to another. The problem in general is known as switching noise.

Figure 6-13 shows a representative CMOS logic gate. The capacitor, C_L, represents all of the capacitances related to construction of the CMOS transistors Q1 and Q2. When the gate switches from one state to another, C_L has to charge (or discharge) before the gate can reach its steady-state value. For example, at a logic state of 0, Q1 is off and Q2 is on, the output (and VC_L) is at V_{SS} (0 V). When the gate tries to switch to a high state, logic level 1, Q1 turns on, Q2 turns off, and C_L begins to charge to V_{DD}. During this transition the gate consumes significant power because for a brief moment Q1 and Q2 are both partially on. A short circuit exists from V_{DD} to V_{SS} through Q1 and Q2 and through C_L (which has low impedance while it

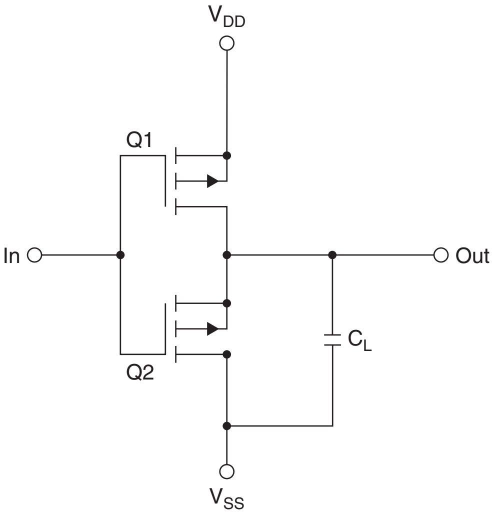


Figure 6-13 A CMOS logic gate.

charges). Because a high current results (even if only briefly) the voltage at the V_{DD} pin tends to drop until the switching is complete and C_L is fully charged. A similar thing happens when the gate tries to change from a logic 1 to a logic 0 state except that as C_L tries to discharge through Q2 (which is turning on as Q1 turns off) the voltage at the V_{SS} pin tends to rise until the switching is complete and C_L is fully discharged.

Because the power and ground planes are not superconductors there is a drop in voltage between the supply pins of the gate and where power is connected to the PCB (same for the return plane). Remember that there is always some amount of resistance and inductance—even on the so-called ground plane. This is shown in Fig. 6-14, in which we see the supply voltages across the PCB while the gate is switching. The drop in the positive rail is called rail collapse and the rise in ground potential is called ground bounce. Note that, since there is really nothing magical about the so-called ground plane, the term "rail collapse" can refer to the ground rail rising as well as the supply rail dropping.

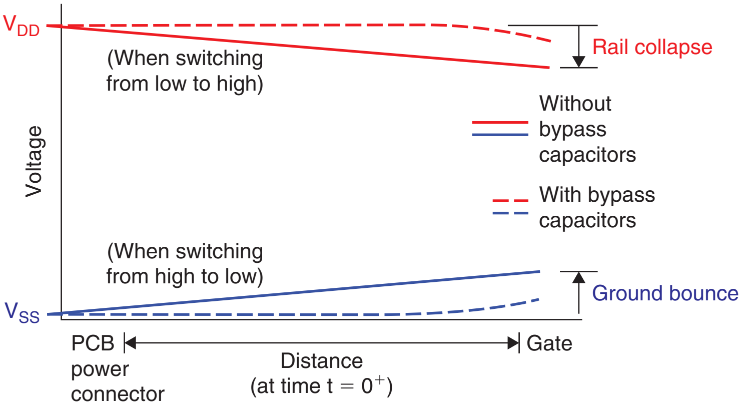


Figure 6-14 Illustration of ground bounce and rail collapse.

The solid line in Fig. 6-14 shows that a relatively linear drop in positive rail voltage (or rise in ground potential) occurs along the distance from the connector to the switching gate when none of the ICs on the PCB have bypass capacitors. The worst voltage drop occurs at the gate itself, but any gates located between the switching gate and the connector will "feel" the voltage drop as well.

The dashed lines in Fig. 6-14 indicate the voltage drop (or rise in ground potential) when all of the ICs have bypass capacitors. The capacitors act as current reservoirs and help hold up the positive rail voltage and keep down the return (ground) rail voltage except at close proximity to the gate that is switching (although it is minimized there as well).

The primary purpose of bypass capacitors in digital circuits is to promote a stable PCB power distribution system and prevent rail collapse and ground bounce—that is, to keep switching noise off from the rails. Conversely, the purpose of analog bypass capacitors is to keep any power supply noise that does exist from getting to the analog circuitry; that is, the bypass capacitors act as lowpass filters and short out power supply transients (noise) before they get to the amplifiers.

Since analog circuits (particularly amplifiers) are usually designed to operate strictly between (and a safe distance from) the rails, they rarely cause rail collapse but are usually the victims of it. The purpose of amplifier circuits is to amplify small signals, which are often in the millivolt or microvolt range; thus a very quiet circuit environment is highly desirable. Since digital switching noise can be as much as 100 mV or more, making analog and digital systems work together on the same PCB can be a significant challenge.

Even when a PCB's power distribution system is well designed (low inductance planes and lots of bypass caps) switching noise can be a significant problem for analog circuits (and other digital circuits for that matter) as the switching currents surge across the PCB planes. This is particularly true if the analog circuitry is between the PCB connector and the noise digital circuitry. Any voltage drops along the path will be seen as noise by the analog system.

It was said earlier (see Fig. 6-12) that as long as traces did not overlap or if they were not too close the return currents would tend to stay directly under the signal traces and cross talk would be minimized. However, in very high frequency analog or high-speed digital systems, return currents (whether signal or power return) may deviate from the ideal path because of imperfections in the PCB's copper plating and variations in the laminate materials. As a result, high-frequency analog and high-speed digital return currents may actually spread across a return plane "looking" for the path of least inductance. This occurs particularly when a signal leaves one layer and goes to another through a via and the return currents do not have an easy path from the one return plane to another that is closer to the new signal layer.

Split power and ground planes

The solution to the problem of digital noise being injected into analog circuitry through the supply planes is to segregate the analog components from the digital ones and eliminate common return paths. Segregating the components is straightforward; the components are physically placed in different places on the board. Eliminating common return paths can be accomplished by splitting the ground and power planes into separate areas. The various planes are shown in Fig. 6-15. A typical plane is one continuous sheet (an entire layer dedicated to a single power or ground connection) as shown in Fig. 6-15(a). But it is possible and advantageous to break up the plane into sections or to create completely separate planes for the digital and analog areas. Figure 6-15(b) shows a split plane that provides isolated areas on a single layer while providing an electrically common reference point. This configuration is common where power electronics are placed over the plane area that is close to the board connectors, and analog and digital electronics are placed over their respective return planes. This allows all circuits on the board to be referenced to a common ground but forces the specific return currents to stay within their own areas. This is demonstrated in the design examples in Chap. 9.

Return planes can also be completely separate areas by using moats as in Fig. 6-15(c) or distinct continuous planes as shown in Fig. 6-15(d). Moated planes are sometimes used as

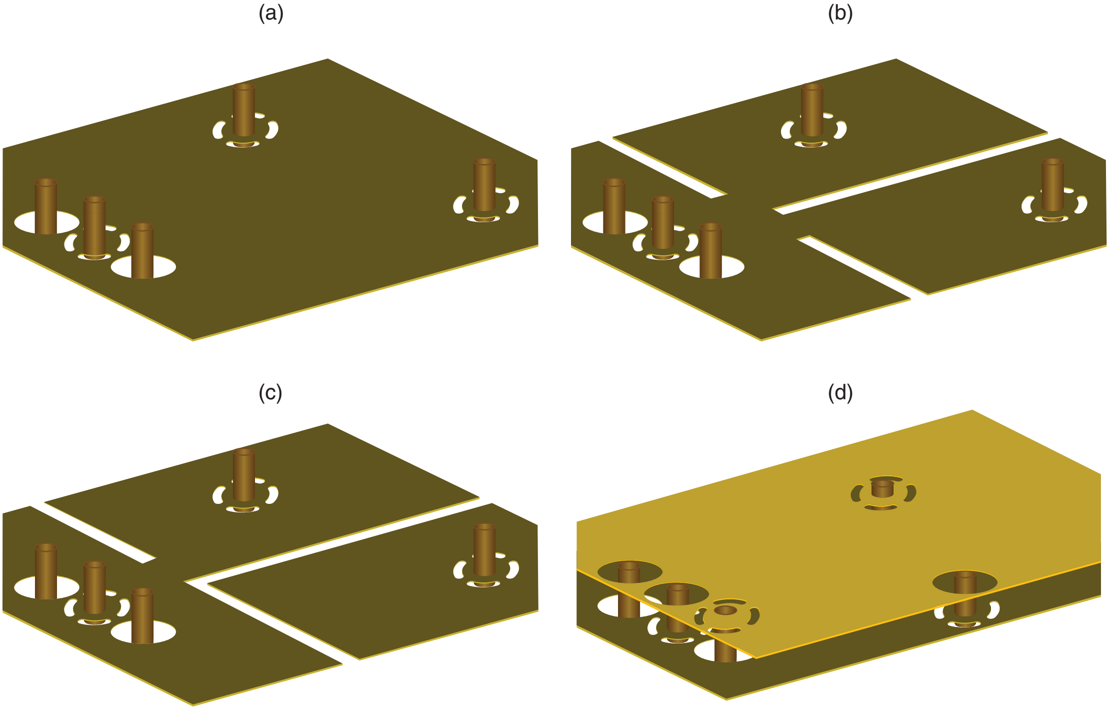


Figure 6-15 Different types of power/ground planes. (a) Continuous plane. (b) Split plane. (c) Moated plane. (d) Isolated, continuous planes.

local ground or reference planes for high speed clocks or small sections of a circuit that require their own regulated supply or ground potential, and isolated planes are used where parts of the system do not share a common ground reference or power supply system.

Care must be exercised when using split or multiple isolated ground and power planes. Even if the planes are separated physically noise can be capacitively coupled from one plane to the next as shown in Figs. 6-16(a) and 6-16(b). To minimize noise coupling between analog and digital planes, split planes on different layers should be prevented from overlapping each other, as shown in Fig. 6-16(c), or should be separated with a shield plane, as shown in Fig. 6-16(d). This is demonstrated in Example 3 in Chap. 9.

On rare occasions the analog and digital return or reference planes of a PCB may be on different layers (and not overlapping or separated by a shield plane) but must be referenced to a common point (for example, when working with analog-to-digital and digital-to-analog converters). So the question becomes how to keep them physically separated but electrically connected. The easiest way is by using the isolated planes (Fig. 6-15(c)) and then connecting the planes at a point using a plated through-hole as shown in Fig. 6-17(a) or a shorting bar (search for "copper strip" in the *Layout User's Guide*). Moated planes (Fig. 6-15(c)) can also

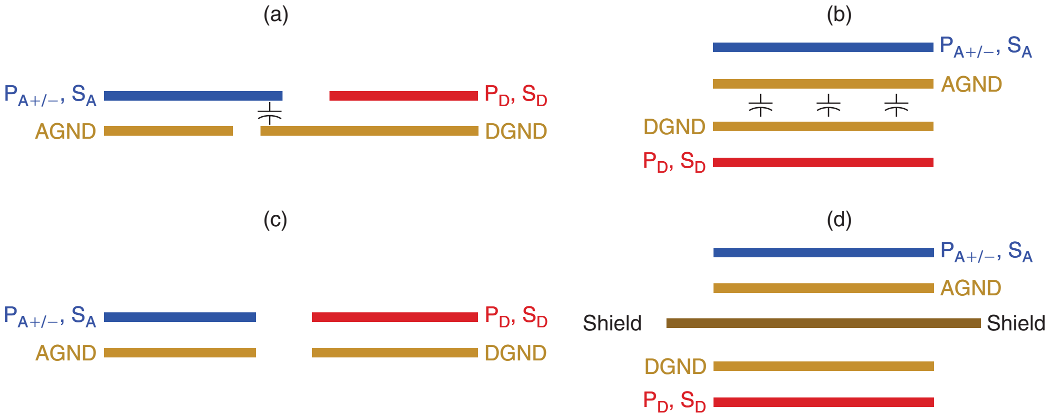

(a)
$P_{A+/-}$, S_A
AGND
P_D, S_D
DGND
(b)
$P_{A+/-}$, S_A
AGND
DGND
P_D, S_D
(c)
$P_{A+/-}$, S_A
AGND
P_D, S_D
DGND
(d)
$P_{A+/-}$, S_A
AGND
Shield
Shield
DGND
P_D, S_D

Figure 6-16 Power and ground plane stack-up scenarios. (a) Coupling between overlapped planes. (b) Coupling between parallel planes. (c) Nonoverlapping split planes. (d) Shielded isolated planes. Key: P, power; S, signal; A, analog; D, digital.

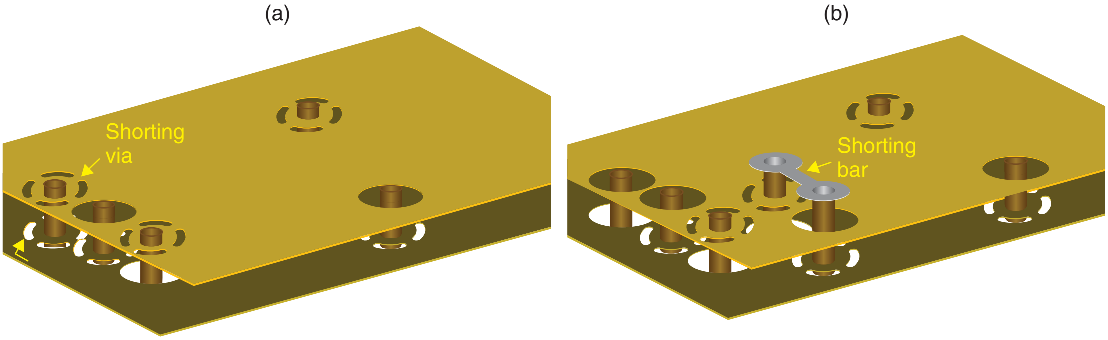

(a)
Shorting
via
(b)
Shorting
bar

Figure 6-17 Methods of shorting separate plane layers together. (a) A via as a short. (b) A copper trace (strip) as a short.

be connected using the shorting bar. Both of these methods can be used in Layout and are demonstrated in the design examples.

PCB Electrical Characteristics

Characteristic impedance

It was stated earlier that to minimize cross talk we want to minimize trace (loop) inductance and maximize the capacitance to the return plane. What does this do to the characteristic impedance, Z_0, of a trace?

Perhaps the first thing to do is to look at what characteristic impedance really is. For example RG58 is a coaxial cable that is often used as a shielded transmission line in 50-Ω systems. Actually, RG58 is about 52 Ω, not 50 Ω. But even so, what does that mean? If you use an ohmmeter to measure the resistance from the center conductor to the shield you will see that it is neither 52 nor 50 Ω. So how is its characteristic impedance 52 Ω?

Figure 6-18 shows a model of a transmission line, which consists of series inductors and parallel capacitors. This is called the lumped-element model, which assumes that the series resistance is negligibly small and that the transmission line is infinitely long (or at least long enough to watch what happens). Each LC "lump" represents a finite section of the transmission line, and the sum total of the elements is representative of the total inductance and capacitance of the transmission line.

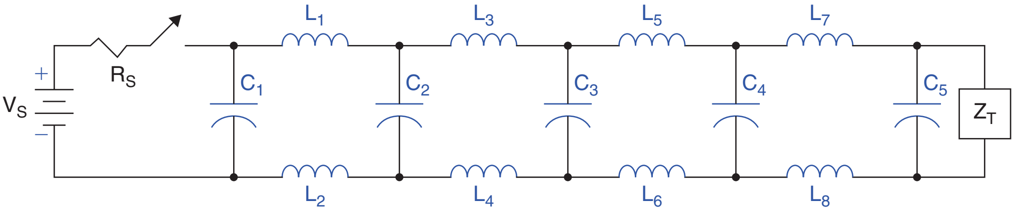


Figure 6-18 A lumped-element transmission line model.

We begin the analysis with all of the capacitors discharged and all currents at zero. At time $t = 0$ s the switch is shut, which applies the source voltage, V_S, to the transmission line through the source resistance R_S as shown in Fig. 6-19. Initially C_1 acts as a short circuit so $I = V_S/R_S$. Current, I, begins to charge capacitor C_1, and a return current will also flow out of the bottom of C_1 back to the source (note that this is a *displacement* current as postulated by Maxwell rather than a *conduction* current as defined by Ampere). The instantaneous impedance is $Z_{C1} = V_{Line}/I$.

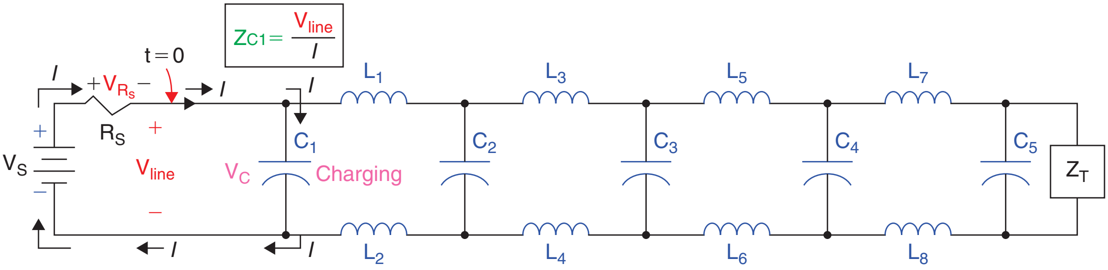


Figure 6-19 A signal applied to the transmission line.

As C_1 charges (no longer acting like a short) current begins to flow into L_1. Each inductor pair (L_1 and L_2, L_3 and L_4, etc.) is mutually coupled, so the magnetic field of L_1 induces the return current in L_2.

As current flows past L_1, C_2 begins charging positively on the top side; and as L_2 forces return current to flow back to the source (due to mutual inductance), C_2 begins charging negatively on the bottom side (relative to its top lead).

At some point C_1 becomes fully charged to a value of $V_{C1} = V_{Line} = V_S - I \cdot R_S$ and then the displacement current no longer flows through C_1, so the instantaneous impedance at C_1 is $Z_{C1} = \infty$ and $Z_{C2} = V_{Line}/I$. Current continues down the line, charging up each capacitor in turn to a value of $V_{Cn} = V_{Line}$.

As each capacitor along the way is charging, the instantaneous impedance across the line is $Z_{Cn} = V_{Line}/I_{Cn}$ as shown in Fig. 6-20. As each capacitor becomes fully charged its impedance goes to infinity because the displacement current through it goes to zero. As seen from the source (V_S) the impedance of the line is $Z_{Line} = V_{Line}/I = V_{Line}/I_{Cn}$ and is dynamic since it travels along the line. Furthermore, the impedance farther down the line is unknown.

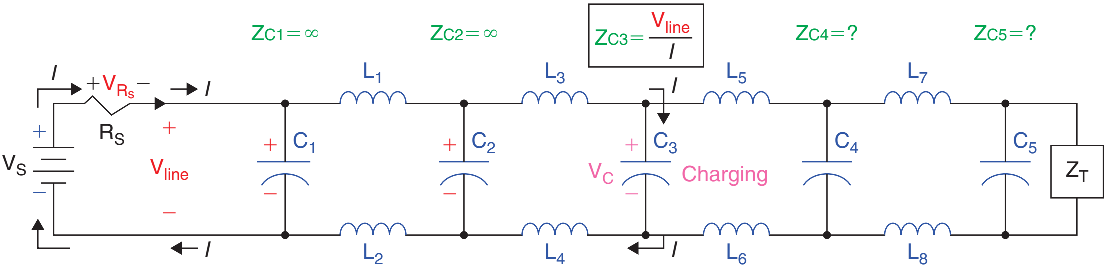


Figure 6-20 The instantaneous impedance propagates along the transmission line.

The speed at which the instantaneous impedance travels along the line is dependent on the inductance and the capacitance of each section. It was said above it is desirable to have as little loop inductance as possible (which will never be zero) and as much capacitance as possible (which will never be infinite). Thus there will always be finite inductive reactance (X_L) and capacitive reactance (X_C) during any transient. However, the capacitors that are charged have nothing to do with the impedance (since they look like open circuits) and the inductors that have steady-state current flowing through them have nothing to do with the impedance (since they look like shorts). The capacitors and inductors farther down the line have nothing to do with the impedance either, since they do not see any action until the capacitors and inductors before them have approached a steady-state condition. Until the voltage (V_{Line}) reaches the load, Z_T, the source actually has no idea the load, Z_T, even exists; neither does it know how many sections of L and C there are until all of the previous sections have reached steady state. If the impedance of each section is the same all along the line, then we call the instantaneous impedance the characteristic impedance of the transmission line and give it the special symbol Z_0.

Before we consider what happens to the current flow and line voltage in Fig. 6-20 once all of the capacitors are charged, and the line voltage and current reach Z_T, we need to take a closer look at the behavior of the transmission line. From the above discussion we see that it takes a finite amount of time for the applied voltage (minus the voltage drop, V_{Rs}) to propagate down the line, and, as the applied voltage propagates, it essentially behaves as a wave. In fact the effects described here are due to wave properties and not directly due to electrons flowing (at least not like we normally think of them). The key to understanding Z_0 (and reflections and ringing as we will see shortly) is in understanding how and at what speed the waves travel.

If you ask an average person how fast electricity travels you will usually get the answer that it travels at the speed of light. Except in one particular case, that answer is not correct. If we think of electricity as flowing electrons, then electricity actually travels at only about 1 cm/s (Bogatin, 211), pretty slow really. This seems counterintuitive since when we turn on a light switch the lights come on seemingly immediately, as if the "electricity" traveled at the speed of light from the switch to the light bulb. But what does travel at (almost) the speed of light is the electromagnetic wave that is launched into the wiring by the switch closing.

Figure 6-21 can be used to explain the difference between the speed of electrons and the electromagnetic wave velocity. The figure shows a copper tube, which contains marbles that are separated by small springs. If an additional marble (No. 5) is shoved into the tube, marble 4 is shoved further into the tube, compressing the spring between it and marble 3. Note that in this early stage marbles 2 and 1 have no idea what is going on yet. As No. 5 is shoved into No. 4's place the rest of the marbles must "do the wave" to make room for it. Eventually all of the marbles have slid over by one marble space and marble 1 pops out the other end.

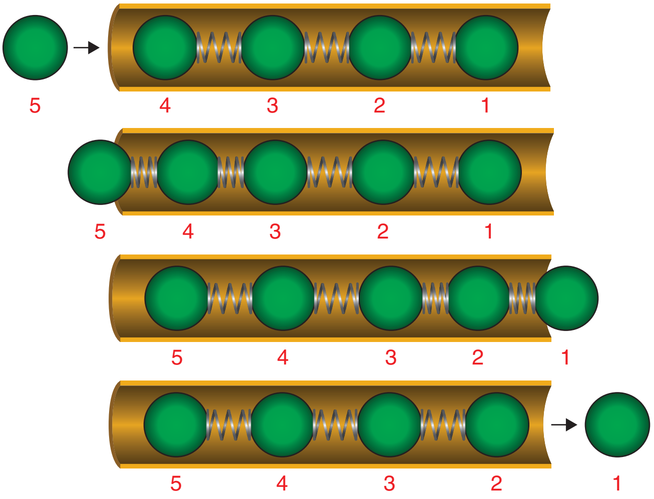


Figure 6-21 Wave velocity vs particle velocity.

Notice now that all of the marbles have moved a distance of only one marble space, but the effect of this movement (a wave) is felt at the end of the tube in about the same amount of time. The speed of the wave is determined for the most part by the value of the spring constants and partly by the momentum of the marbles.

So in a transmission line the electrons travel slowly, but the electromagnetic (EM) waves travel fast. The speed of the EM wave is determined by how quickly the magnetic fields in the inductors and the electric fields in the capacitors can be built up or dissipated, which is influenced by the material properties and geometry of the PCB through which the wave travels.

The velocity of an EM wave through a medium is described by Eq. (10),

$$v_{\mathrm{EM}} = \frac{1}{\sqrt{\varepsilon_0 \varepsilon_r \mu_0 \mu_r}}, \tag{10}$$

where v_{EM} is the velocity of the EM wave in a given material, ε_0 is the permittivity of free space (8.89×10^{-12} F/m), ε_r is the relative permittivity (dielectric constant) of the material (a unitless constant relative to ε_0), μ_0 is the permeability of free space ($4\pi \times 10^{-7}$ H/m), and μ_r is the relative permeability of the material (a unitless constant relative to μ_0).

You may recall that the speed of light, c (a special EM wave), in free space is

$$c = \frac{1}{\sqrt{\varepsilon_0 \mu_0}}. \tag{11}$$

So we can rewrite Eq. (10) as

$$v_{\mathrm{EM}} = c \cdot \frac{1}{\sqrt{\varepsilon_r \mu_r}}. \tag{12}$$

As stated, the terms ε_r (relative permittivity) and μ_r (relative permeability) are unitless. Furthermore μ_r is equal to 1 in free space and in most polymers (including FR4 laminate), so we can further simplify Eq. (12) as shown in Eq. (13):

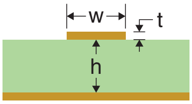
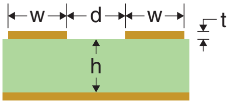
$$v_{\mathrm{EM}} = c \cdot \frac{1}{\sqrt{\varepsilon_r}}. \tag{13}$$

From Eq. (13) we see that the velocity of an EM wave (which comprises both electric and magnetic fields) in a PCB varies inversely with the relative permittivity, ε_r.

Relating this observation with Eq. (7) we can state (without rigorous proof) that the capacitance of a transmission line is determined by the geometry of the transmission line and the relative dielectric constant (ε_r) within the transmission line. And the inductance of a transmission line (specifically the loop inductance) is determined by the geometry, but μ_r falls out since it is equal to 1 (see Eq. (5) and Figs. 6-4 and 6-5).

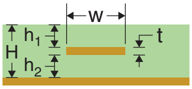
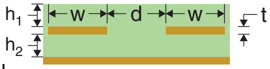
In practice, calculating the characteristic impedance, capacitance, and inductance can be fairly complex, depending on the geometry of the circuit, but fortunately that has been done for us for the most common transmission line configurations. The equations are shown in

Tables 6-2, 6-3, 6-4, and 6-5. The PCB designer has full control over the trace width (*w*) and partial control over the trace thickness (*t*) by selecting the ounces per square foot, but may have little or no control over the thickness of the laminate (*h*). These equations are solved for *w* and presented later in this chapter (see Tables 6-6 and 6-7).

Microstrip transmission lines	**Z_0 (Ω)**	**C_0 (pF/in.)**
Surface 	$Z_0 = \frac{k}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w+t}\right)$	$C_0 = \frac{0.67(\varepsilon_r + 1.41)}{\ln\left(\frac{5.98h}{0.8w+t}\right)}$
Surface differential 	$Z_{\text{diff}} = 2Z_0\left(1 - 0.48 \cdot e^{\left(-0.964\frac{d}{h}\right)}\right)$ Z_0 same as surface microstrip	

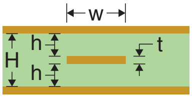
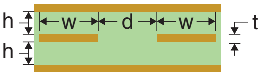
$L_0 = \frac{Z_0^{\,2} \cdot C_0}{12}$ in nH/in., where ***k*** = 87 for 15 < ***w*** < 25 mils and ***k*** = 79 for 5 < ***w*** < 15 mils. Restrictions: 0.1 < ***w/h*** < 3.0 and 1 < ε_r < 15 (typically 4.0 to 4.5 for FR4).

Table 6-2 Surface microstrip transmission lines

Microstrip transmission lines	**Z_0 (Ω)**	**C_0 (pF/in.)**
Embedded 	$Z_0 = \frac{k}{\varepsilon_r + 1.41} \ln\left(\frac{5.98h_2}{0.8w+t}\right)\left(1 - \frac{h_1}{0.1}\right)$ OR $Z_0 = \frac{k}{\varepsilon_{r.\text{eff}} + 1.41} \ln\left(\frac{5.98h_2}{0.8w+t}\right)$ $\varepsilon_{r.\text{eff}} = \varepsilon_r\left(1 - e^{\frac{-1.55H}{h_2}}\right)$	$C_0 = \frac{1.41\varepsilon_{r.\text{eff}}}{\ln\left(\frac{5.98h}{0.8w+t}\right)}$
Embedded edge coupled differential 	$Z_{\text{diff}} = 2Z_0\left(1 - 0.48 \cdot e^{\frac{-0.964}{2h+t}}\right)$ $h = h_1 = h_2$ Z_0 same as embedded microstrip	

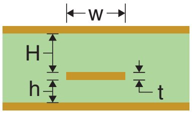
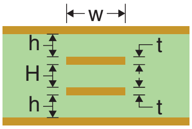
k = 87. Restrictions: 0.1 ***w/h*** < 3.0, 1 ε_r < 15, and $Z_0 < Z_{\text{diff}} < 2Z_0$.

Table 6-3 Embedded microstrip transmission lines

Stripline transmission lines	**Z_0 (Ω)**	**C_0 (pF/in.)**
Balanced (symmetric) 	$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9H}{0.8w+t}\right)$ OR $Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9(2h+t)}{0.8w+t}\right)$	$C_0 = \frac{1.41\varepsilon_r}{\ln\left(\frac{3.81h}{0.8w+t}\right)}$
Differential (edge coupled) 	$Z_0 = 2Z_0\left(1 - 0.347 \cdot e^{\frac{-298}{2h+t}}\right)$ Z_0 same as symmetric stripline	

Restrictions: $w/(h-t) < 0.35$ and $w/h < 2.0$, $t/h < 0.25$, and $0.005 < w < 0.015$ in.

Table 6-4 Balanced stripline

Stripline transmission lines	**Z_0 (Ω)**	**C_0 (pF/in.)**
Unbalanced (asymmetric) 	$Z_0 = \frac{80}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9(H+h+t)}{0.8w+t}\right)$ $\left(1\frac{h}{4(H+h+t)}\right)$	$C_0 = \frac{2.82\varepsilon_r}{\ln\left(\frac{2(h-t)}{0.268w+0.335t}\right)}$
Differential (broadside compled) 	$Z_{\text{diff}} = \frac{82.2}{\sqrt{\varepsilon_r}} \ln\left(\frac{5.98H}{0.8w+t}\right)$ $(1 - e^{-0.64})$ Z_0 same as unbalanced stripline	

References: IPC-2141, p. 12; IPC-2221A, p. 44; IPC-D-330, Section 2, Table 2-1 2; Brooks, p. 203; Montrose (1999), p. 171–177.

Table 6-5 Unbalanced stripline

Note

- *Unless otherwise noted,* $L_0 = \frac{Z_0^{\,2} \cdot C_0}{1000}$ *in nH/in.*

Reflections

So the next question is, what happens when the voltage "wave front," V_{Line}, reaches the termination impedance, Z_T? The answer is that it depends on what Z_T is.

Let's assume for a minute that Z_T is an open circuit. When the last capacitor, C_5, in Fig. 6-18 is charged and V_{Line} reaches Z_T (which equals infinity), then all capacitors are charged along the line (and their impedance equals infinity), so all current stops—or at least it would like to. But it cannot, because all of the inductors have current, I_{Line}, through them and they will not allow I_{Line} to stop instantly. As the magnetic fields of L_7 and L_8 begin to collapse to try to maintain their current (remember that they are mutually coupled and influence each other) they continue to shove current into C_5, raising its voltage a bit more (we will see later what "a bit more" means).

The magnetic fields of each inductor pair (L_3 and L_4, L_1 and L_2, etc.) will collapse, one after the next, back toward the source and raise the voltage of its nearest capacitor, all the way down the line. This new voltage front (V_{Line} + a bit more) propagates back from Z_T toward the source with the collapsing magnetic fields until all of the magnetic fields have collapsed and all of the capacitors have this new charge on them. An analogy of a reflection from a high impedance termination is shown in Fig. 6-22, which shows a person launching a wave into a rope. If the rope experiences little or no friction, the wave will propagate down the rope unattenuated. If the end of the rope is loose (a high impedance) the wave will be reflected back toward the person, who will feel an identical wave returned.

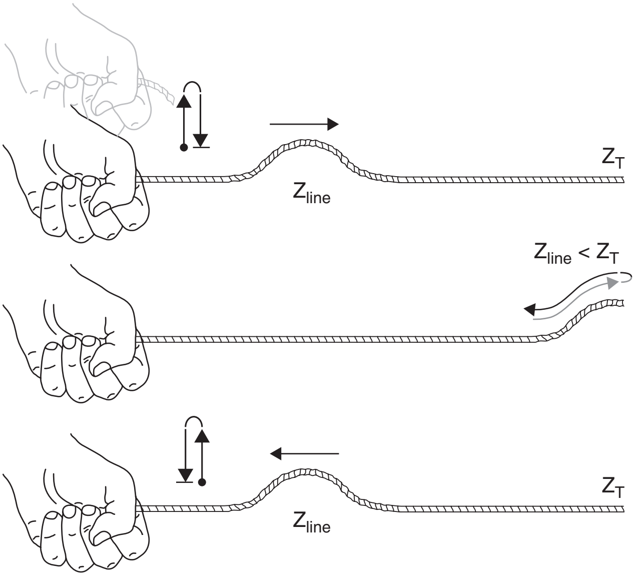


Figure 6-22 Positively reflected wave (Z_T is an open circuit).

In the example above the reflected wave has the same polarity and amplitude of the transmitted (incident) wave. In reality the rope would not be in a frictionless environment (and Z_T would not be infinitely high). In that case the reflected wave would still have the same polarity as the incident wave but the amplitude would be less.

The magnitude and polarity of the reflected wave are described by the reflection coefficient, ρ (Greek letter "r"), as shown in Eq. (14):

$$\rho = \frac{Z_T - Z_{\text{Line}}}{Z_T + Z_{\text{Line}}}. \tag{14}$$

The reflection coefficient can have values between -1 and $+1$. If $Z_T > Z_{\text{Line}}$ (i.e., as Z_T approaches ∞, as in the example above), then

$$\rho \cong \frac{Z_T}{Z_T} = 1,$$

which means that the reflected wave will be exactly the same amplitude and have the same polarity as the incident wave.

Next we consider what happens if Z_T (in Fig. 6-18) is a short circuit instead of an open circuit. At first the exact same thing occurs as described above when the switch is shut. That is (assuming the same initial conditions as above, all caps are discharged, etc.), the capacitors and inductors take their turn charging up and building up magnetic fields, V_{Line} is applied to the line, current I_{Line} flows, and $Z_{Cn} = V_{\text{Line}}/I_{Cn}$, so the instantaneous line impedance is equivalent to Z_{Cn}. A different result occurs at the end of the transmission line. Since $Z_T = 0\ \Omega$ and inductors L_7 and L_8 again want to maintain their current flow, I_{Line} flows straight through the short, Z_T.

Since the current through L_7 and L_8 is maintained (even for just an instant) and since the voltage drop across an inductor with a constant current flow is zero, capacitor C_4 sees the short and begins to discharge through L_7 and L_8 (helping to maintain their current flow) and on through the short, Z_T. A short moment later C_4 is at the same potential as C_5 and Z_T (0 V), while L_7 and L_8 have managed to maintain their current. The capacitors continue to discharge one after the other (C_3, then C_2, etc.) and each inductor pair maintains its current until finally all capacitors are shorted (and all the inductors look like a short if they have the same constant current). In the final analysis, $V_{\text{Line}} = V_{ZT} = 0\,\text{V}$ and therefore $Z_{\text{Line}} = 0/I_{\text{Line}} = 0\ \Omega$ and $I_{\text{Line}} = V_S/R_S$.

A mechanical analogy of a wave reflected negatively from a "dead short" is shown in Fig. 6-23. If a positive wave is launched into a rope that is rigidly fixed at the end the wave will be negatively reflected. In a perfectly loss-less environment the reflected wave will be of the same magnitude but opposite polarity as the incident wave.

In the electrical example above, the negatively reflected wave has the same magnitude as but opposite polarity to the voltage stored on the capacitors. As the negative wave hits each capacitor it is forced to give up its charge (as current), which helps maintain the current flow through the nearest inductors and all the way down the line through the short at the end of the line. This negatively reflected wave is again represented mathematically by the reflection

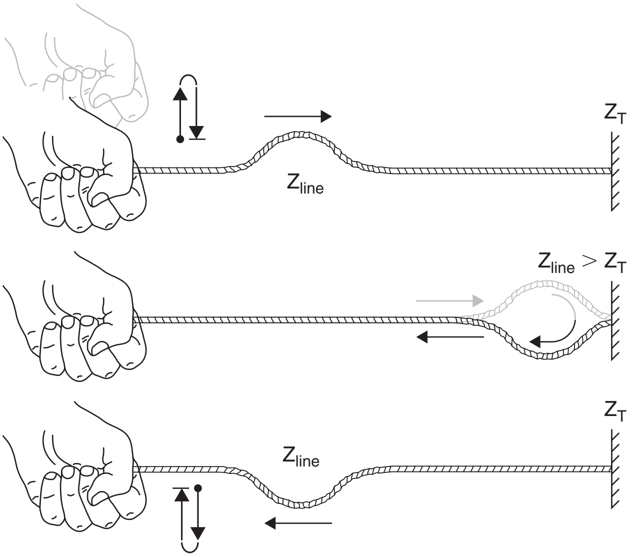


*Figure 6-23 Negatively reflected wave (**Z_T** is a short circuit).*

coefficient (Eq. (14)), but in this case since $Z_T < Z_{Line}$ (i.e., as Z_T approaches 0), $\rho = -1$, as shown in Eq. (15):

$$\rho = \frac{-Z_{Line}}{Z_{Line}} = -1. \tag{15}$$

Now let's say for argument that the characteristics of our transmission line are such that when we calculate $Z_{Cn} = V_{Line}/I_{Cn}$ at each capacitor/inductor section, $Z_{Cn} = 50\ \Omega$. Let us also set $R_S =$ to $50\ \Omega$. Now what happens when $Z_T = 50\ \Omega$? As you can suppose by this time, at the moment the switch is shut the capacitors take their turn getting charged (and the inductors are building their fields). Since each $Z_{Cn} = 50\ \Omega$ then Z_{Line} is also $50\ \Omega$. Since R_S and Z_{Line} are equal (and act as a voltage divider), $V_{Line} = ½V_S$. Once the wave front has propagated down the line and reaches Z_T, which is also $50\ \Omega$, I_{Line} continues to flow into Z_T as if nothing different has occurred and $V_{ZT} = V_{Line} = ½V_S$. As long as Z_T is purely resistive, then everything is at steady state and $Z_{Line} = Z_T = 50\ \Omega$. Also no voltage is reflected back toward the source because no change in voltage occurred on the capacitors and no current change occurred in the inductors.

In this case, since $Z_T = Z_{Line}$ the reflection coefficient is 0 ($\rho = 0$) as shown in Eq. (16):

$$\rho = \frac{0}{Z_T + Z_{Line}} = 0. \tag{16}$$

The mechanical analogy is shown in Fig. 6-24, in which none of the wave energy is reflected but is perfectly absorbed into the load at the end of the line.

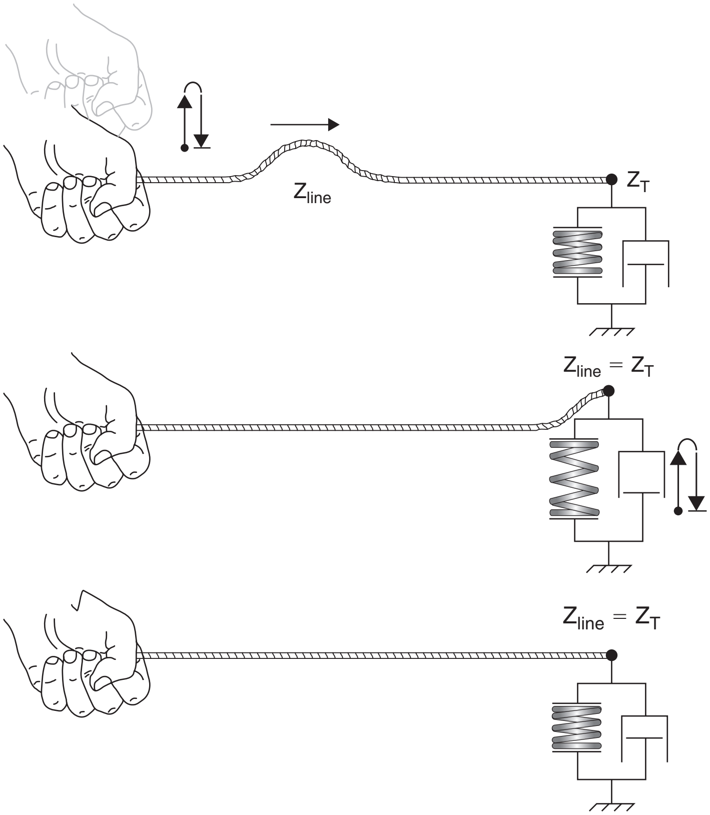


Figure 6-24 No reflection (Z_T absorbs wave energy).

From these examples we can conclude that Z_{Line} is in effect only during voltage transitions and is the result of the voltage transient and the current that flows to charge the line capacitance to the new voltage and to build the magnetic fields in the inductors. We can also see that if the impedance Z_T is not the same as Z_0 then a reflection will occur, but if the impedance Z_T is the same as Z_0 then no reflection will occur. Furthermore it takes a finite amount of time for a wave front to propagate from one end of a transmission line to the other, and if a reflection does occur it takes another finite amount of time for the reflection to propagate back to the source. What happens at the source is the next topic.

Ringing

When $\rho \neq 0$ between any adjacent impedances, reflections will occur. This is true both from driver to transmission line and from transmission line to load (and back). If there is little or no loss along the transmission line the reflected waves will bounce back and forth between the driver and the load if they are not matched to the transmission line (or if the transmission line is not matched to them). When viewing a particular point along the path, for example at the output pin of a gate or amplifier, the repeated reflections will be evident as ringing. Ringing is a direct result of reflections, which in turn are due to impedance mismatches.

One of the problems with ringing is that the voltage at any point along the line is effectively out of control since ringing causes voltage overshoots and undershoots (see Fig. 6-26). Overshoots can actually damage active devices that have input voltage limitations and will radiate greater EMI than normal signals. Overshoots and undershoots can cause digital circuits to be falsely triggered if the reflected voltage swings across switching thresholds. In analog circuits the interactions between a continuous wave signal and its reflections creates standing and/or traveling waves that can degrade the signal of interest.

The magnitude and frequency of the ringing depend on the speed of the wave through the transmission line, the length of the line, and the reflection coefficient at each impedance discontinuity. We take a detailed look at ringing using the circuit shown in Fig. 6-25.

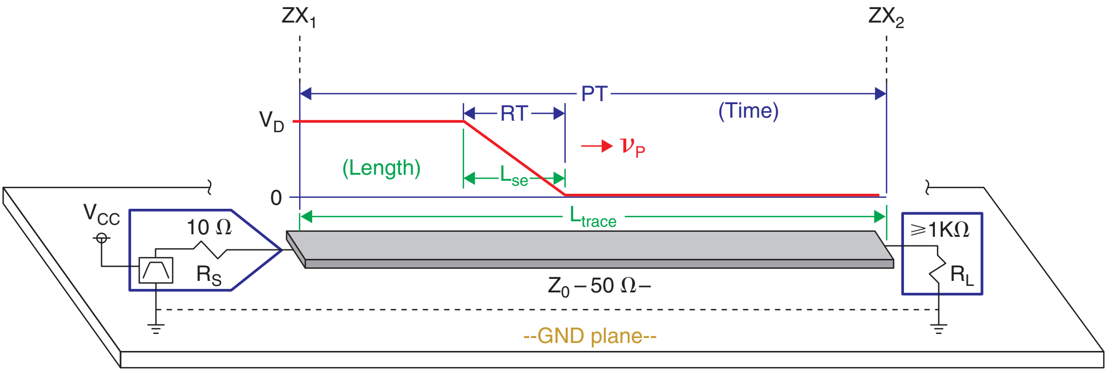


Figure 6-25 Representation of signal propagation on a PCB trace.

The circuit consists of a driver that is powered by V_{CC} and has a low output impedance, R_S (10 Ω); a transmission line with a characteristic impedance, Z_0 (50 Ω); and a receiver with a high input impedance, R_L (usually 1 kΩ or higher). The dashed lines indicate the interfaces of the mismatched impedances and are labeled as ZX_1 and ZX_2. The dimensions in green represent length, and the dimensions in blue represent time. The circuit in the figure can be used to represent an analog or digital circuit, but we will consider the digital application.

Consider the following:

- RT is the rise time, the time it takes for the output of a driver to transition from a minimum value to a maximum value. RT is specific to individual devices and is given in the data sheets.
- L_{trace} is the length of a trace (transmission line) on the PCB.
- v_p is the propagation velocity of a wave and is determined by Z_0, which is determined by ε_r and the transmission line dimensions (trace width and distance to the ground plane).
- PT is the propagation time, the time it takes for the transition to propagate from one end of the transmission line to the other.

- L_{SE} is the effective length of the rising edge (also called transition distance or the spatial extent of the transition (Bogatin, 215) or edge length (Johnson and Graham, 7)).
- Length and time are related by the propagation velocity of the wave, v_{p} (units of distance/time), where $\mathrm{PT} = \frac{L_{\mathrm{trace}}}{v_{\mathrm{p}}}$ (units of time) and $L_{\mathrm{SE}} = v_{\mathrm{p}} \times \mathrm{RT}$ (units in distance).

If length of the trace, L_{trace}, is longer than the spatial extent of the rising edge, L_{SE}, then the rising edge will fit entirely within the length of the trace and the reflection voltage will be an amplitude-scaled copy of the entire rising edge, for which the scaling is determined by the reflection coefficient, ρ. Another way of looking at the same thing is if the RT (rise time) is faster than the PT (propagation time); then the rising edge will have time to be fully reflected.

Electrically long traces

The goal is to design PCB traces such that they do not allow conditions to exist under which propagation times are too slow (compared to signal RTs) or a trace's length is too long (compared to a signal's spatial extent). When these conditions cannot be met, the trace is considered to be "electrically long" and must be treated as a transmission line. Proper treatment of a transmission line means controlling the impedance of the line over the entire length of the line and matching the impedance of the line with the source and load impedances so that reflections do not occur.

The obvious question is, when is a trace too long (or when is the RT too fast)? The magnitude of reflections and the ringing frequency are governed by the down and back (round trip) time of the reflections. Much of the literature states that the propagation time, PT, should be less than one-half of the rise time (i.e., $\mathrm{PT} < ½\mathrm{RT}$) or that the length of the trace should be less than one-half of the special extent of a rising edge (i.e., $L_{\mathrm{trace}} < ½L_{\mathrm{SE}}$). These relationships define the limits, not the goal. The shorter trace lengths are or the slower the RT is, the better off you will be. The examples below illustrate this in greater detail. After the examples general design recommendations are provided.

Figure 6-26 shows what happens when PT is too long compared to RT. The data in the figure were generated using the transmission line model found in PSpice and the PT was set four times longer than the RT (instead of being $< ½\mathrm{RT}$). Simulating transmission lines with Capture and PSpice is covered in Chap. 11. Refer to Fig. 6-25 and 6-26 during the discussion.

(0) At time $t = 0\,\mathrm{ns}$ the logic gate output ($\mathrm{V_{source}}$) switches to $V_{\mathrm{CC}} = 5\,\mathrm{V_{DC}}$ and begins to increase in voltage at the output ($\mathrm{V_{drive}}$) (start of rising edge). The first capacitor in the transmission line is uncharged and acts like a short to GND.

(1) At $t = 10\,\mathrm{ns}$ the gate has finished switching and the voltage at the output of the driver, V_{D}, is $V_{\mathrm{D}} = V_{\mathrm{CC}} \frac{Z_0}{Z_0 + R_{\mathrm{S}}} = 5\left(\frac{50}{50+10}\right) = 4.17V$ because of the voltage divider established by $\mathrm{R_S}$ and Z_0. At this point the beginning of the rising edge is halfway to the load, and the tail end of the rising edge is just leaving the load side of $\mathrm{R_S}$.

(2) At $t = 20\,\mathrm{ns}$ the beginning of the rising edge reaches the load resistor, $\mathrm{R_L}$. Since there is an impedance mismatch between Z_0 (50 Ω) and R_{L} (1 kΩ) there is a positive reflection that

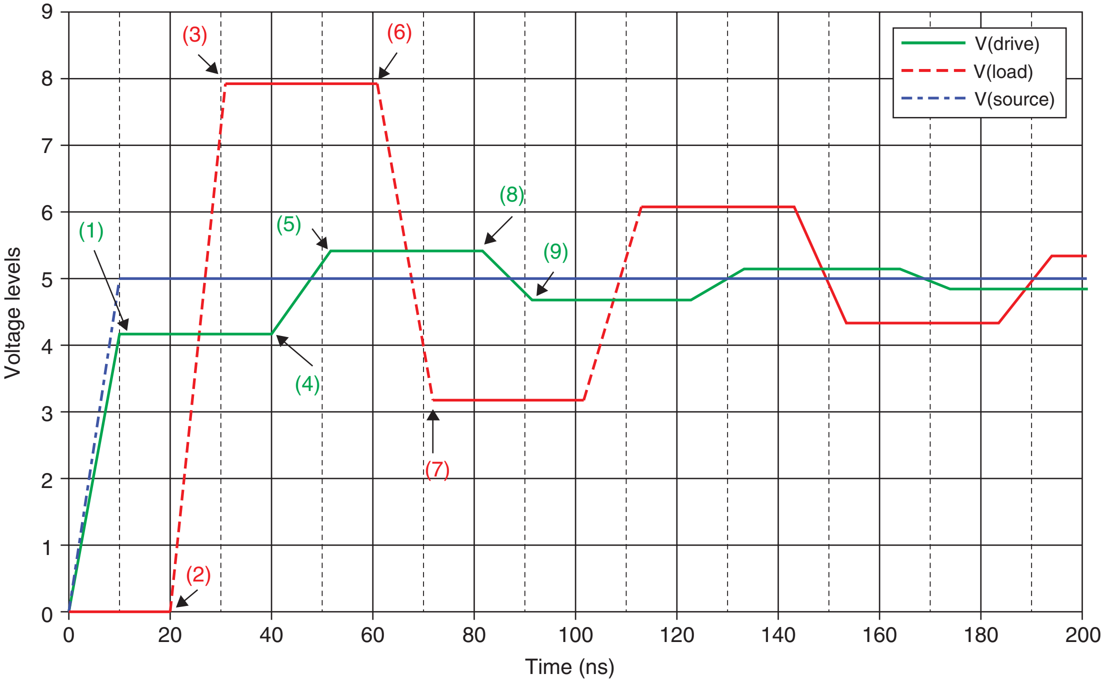


Figure 6-26 Ringing on an electrically long transmission line.

begins immediately to head back to R_S. The reflected voltage is added to the rest of the rising edge as it continues to arrive at R_L. The reflection coefficient looking into the load from the transmission line is $\rho = \frac{1000-50}{1000+50} = 0.90$.

(3) By $t = 30$ ns the trailing end of the rising edge reaches the load. The voltage at the load (V_{load}) is now the sum of its previous voltage (0 V) plus the value of the incoming voltage (4.17 V) plus the reflected voltage ($4.17 \times 0.90 = 3.75$ V) for a total of $4.17 + 3.75 = 7.92$ V. The reflected voltage (3.75 V) is well on its way back toward the source.

(4) At $t = 40$ ns the rising edge that was positively reflected from the load begins to arrive at the source, R_S. The voltage at the source begins to rise (pts 4 to 5). However, since the impedance of the transmission line is greater than that of the source resistor, a negative reflection immediately begins to head back to the load. The reflection coefficient from the transmission line looking into R_S is $\rho = \frac{1000-50}{1000+50} = 0.90$.

(5) At $t = 50$ ns the 3.75 V reflected off from the load has completely reached R_S. The voltage at the load side of R_S is the sum of its original value (4.17 V) and the incoming reflected voltage (3.75 V) plus the voltage being re-reflected back to the load ($-0.667 \times 3.75\,V = -2.50\,V$) for a total of $4.17 + 3.75 + -2.5 = 5.42$ V. And the -2.50 V is on its way to the load.

(6) At $t = 60$ ns the -2.50 V reaches the load and begins to lower the load voltage from its previous value of 7.92 V. Because of the impedance mismatch between the transmission line

and the load, a reflection is immediately launched again. The reflection coefficient is still +0.90, so the reflection will have the same polarity as the incident wave. Since the incident wave is the −2.50 V reflected off from R_S, the load will reflect back a negative voltage. As the incoming −2.50 V runs into a positively reflected negative voltage, the overall voltage at the load (pts 6 to 7) drops significantly since ρ is high (0.90).

(7) At $t = 70$ ns the −2.50 V reflected off from the source has completely reached R_L where the voltage is the sum of its original value (7.92 V) and the incoming reflected voltage (−2.50 V) plus the voltage being re-reflected back to the load ($-2.50\,\text{V} \times 0.90 = -2.25\,\text{V}$) for a total of $7.92 + -2.50 + -2.25 = 3.16\,\text{V}$). And of course the −2.25 V is on its way to the source.

(8) At $t = 80$ ns the negative voltage that was reflected (positively, i.e., leaving the sign intact) from the load begins to arrive at R_S. Since the incoming voltage is negative, the voltage at R_S begins to fall. But since there is still a negative reflection coefficient (−0.667) from the transmission line looking into R_S, the wave that immediately begins to bounce off from R_S is now positive and heads back to the load.

(9) At $t = 90$ ns the −2.25 V reflected off from the load has completely reached R_S. Again the voltage at R_S is the sum of its previous value (5.42 V) and the incoming reflected voltage (−2.25 V) plus the voltage being re-reflected back to the load ($-0.667 \times -2.25\,\text{V} = +1.50\,\text{V}$) for a total of $5.42 + -2.25 + 1.50 = 4.67\,\text{V}$). And of course the +1.50 V is on its way to the load.

The reflections continue back and forth but decrease in value each trip. The losses occur because the energy that is not reflected at each impedance interface is absorbed into the source and load resistors. Eventually, the reflections become too small to notice and we say that it has reached steady state. The time to reach steady state is called the settling time and the shorter the settling time the better.

If the length of the trace, L_{trace}, is much shorter than the special extent of L_{SE} (as represented in Fig. 6-27), then the rising edge will not fit within the length of the trace and will reach the driver before the driver has even completely reached is steady-state value. If the trace is very short the reflection voltage will be reflected many times and repeatedly fold back onto itself as the driver output climbs to its steady-state value. Since the voltage at an interface is the

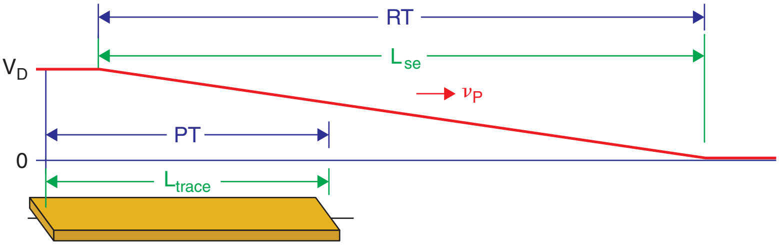


Figure 6-27 Representation of an electrically short trace.

sum of its existing voltage, the incoming reflection, and the reflected reflection, the effects of the reflections become "smeared" into each other. By the time the driver has fully reached its final value most of the reflections have come and gone and only the last, smaller overshoots and undershoots are evident.

Figure 6-28 shows what happens when PT is much shorter than RT on an electrically short trace. The reflections occur as previously described, but as shown in the graph many of the reflections have occurred by the time the driver reaches its full output level. Recall that the voltage at each impedance interface is the sum of its previous voltage plus the incoming voltage plus the reflected voltage, but since the reflections happen fast (relative to the rise time), each reflection never has a chance to reach its full voltage level (only a fraction of the rising edge at that time), so the reflections are much smaller and therefore the peaks (overshoots) and valleys (undershoots) are also much smaller (hardly noticeable), while the driver output is still rising. Also the ring frequency is higher with the shorter trace.

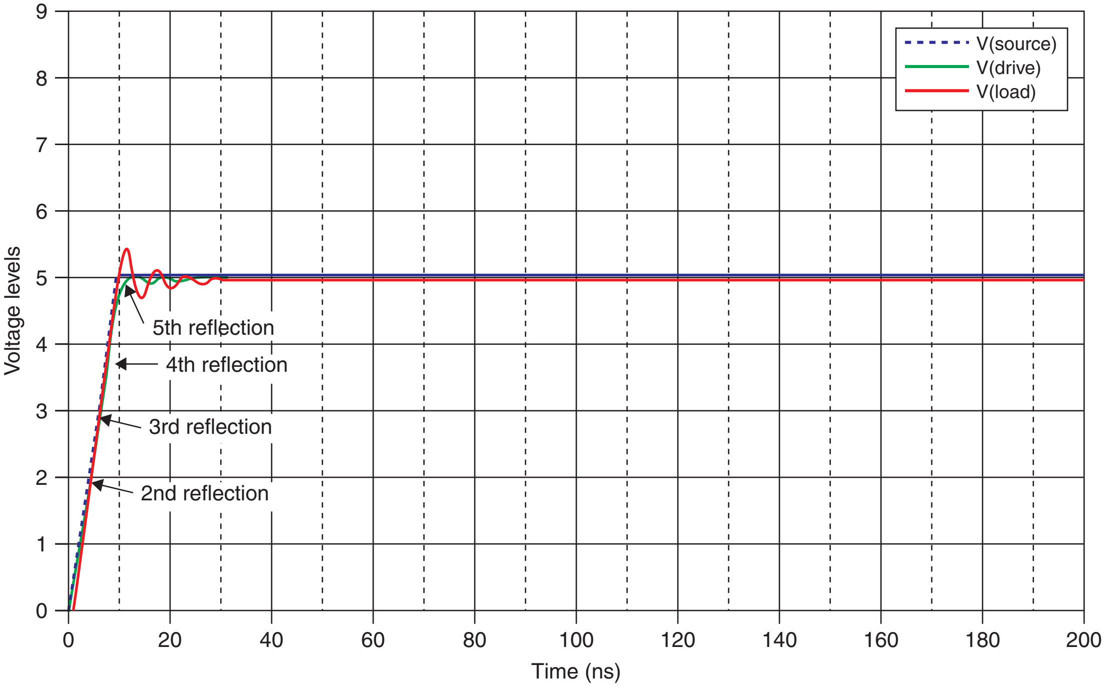


Figure 6-28 Negligible ringing on electrically short traces.

Critical length

As mentioned above an electrically short trace is one for which the propagation time is less than one-half of the rise time (i.e., PT $<$ ½RT) or the length of the trace is less than one-half of the special extent of a rising edge (i.e., $L_{\text{trace}} < ½L_{\text{SE}}$). The length of a trace or transmission line for which these conditions are just barely met is called the critical length. Figure 6-29

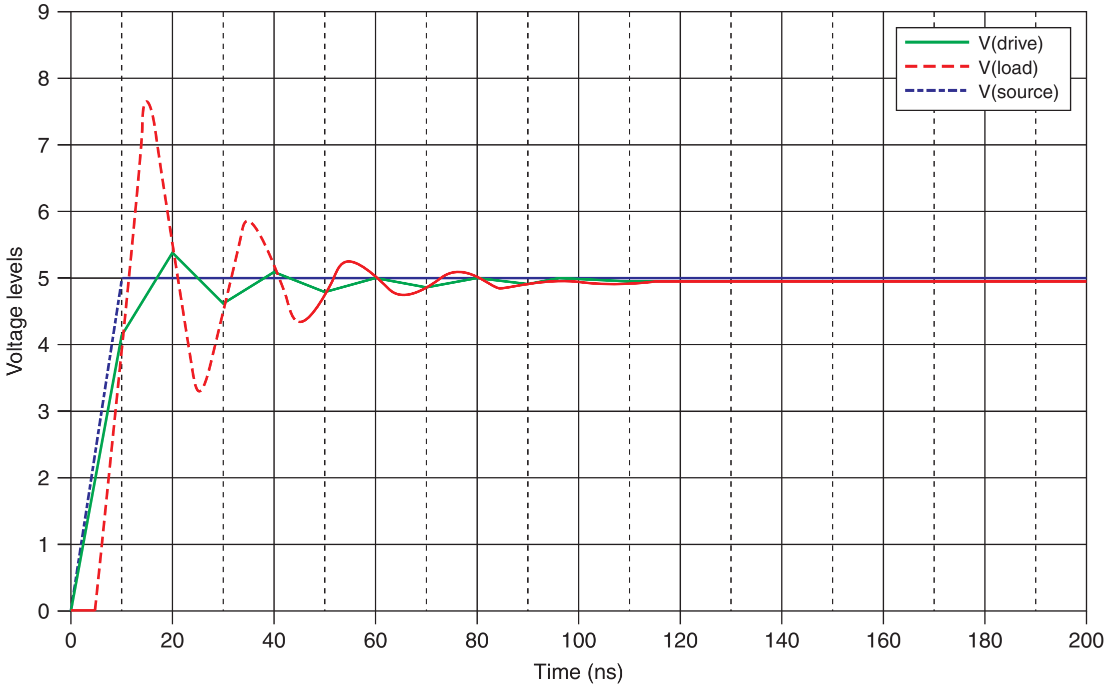


Figure 6-29 Reflections when PT = ½RT.

shows the voltage levels at critical length. Ringing still occurs, but the peaks never level off and the reflections settle sooner. But again the one-half rule is a limit and not a goal. Examples of determining critical length and designing transmission lines are given in the design section below and in Example 4 in Chap. 9.

Transmission line terminations

If we cannot make the rise time slower and/or the length of the trace shorter, then we will have noticeable reflections and ringing. The only other way to stop the reflections and ringing is to eliminate the impedance mismatches that are causing them by properly terminating the ends of the transmission line with the proper source and/or load resistors.

We can make $R_S = Z_0 = R_L$ by using a resistor in series with the source and a resistor in parallel with the load.

If the impedances are all matched then there will be no reflections, as shown in Fig. 6-30. However, only half the voltage will reach the load because a voltage divider results with R_S equal to R_L so $V_{Load} = ½V_{Source}$. This lower voltage at the load may not reach required logic thresholds, preventing affected digital circuits from functioning.

An alternative is to put a resistor in series with the driver such that the impedance that the transmission line sees looking at the driver and series resistor is equal to Z_0. So if Z_0 is

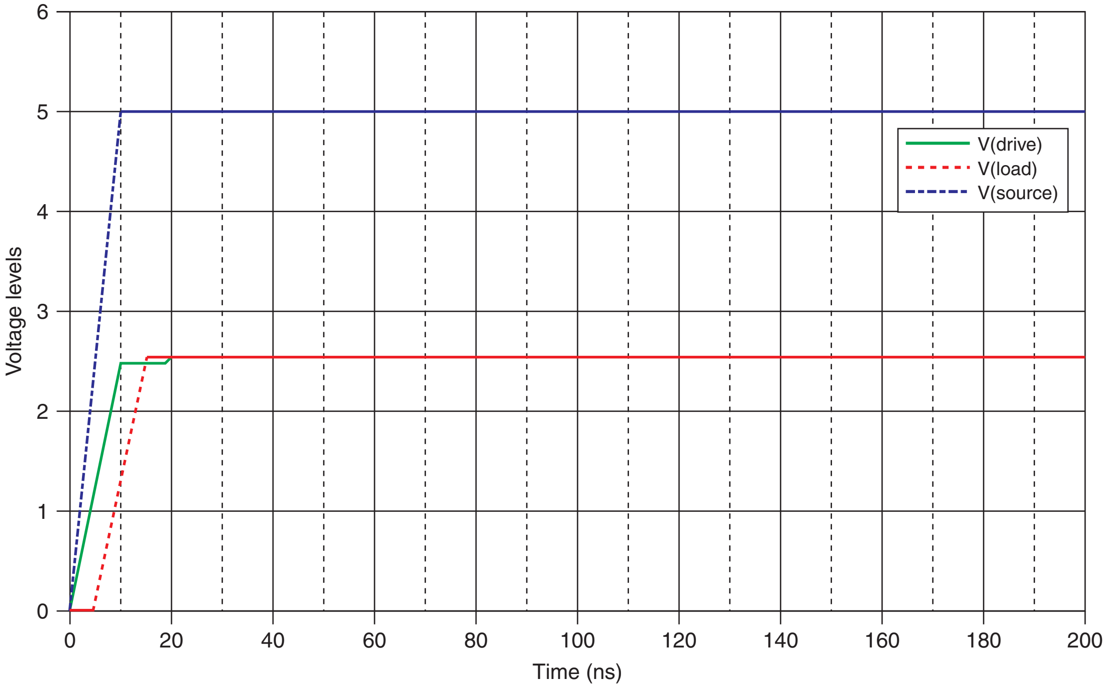


Figure 6-30 No reflections when all impedances are matched.

50 Ω and the driver output resistance is 10 Ω, then the transmission line will be matched to the driver by putting a 40-Ω resistor in series with R_S. An example of the result is shown in Fig. 6-31. Even when PT is > ½RT only one reflection occurs (the flat section on V_{Drive} between 10 and 20 ns) and it is absorbed into the 40-Ω resistor and R_S so the reflection dies there. An advantage of this type of termination technique is that the voltage at the load is also much closer to the ideal voltage. The momentary hold on V_{Drive} is usually not a problem, but it can be a problem in high-speed clock circuits for which the steady-state on (off) time is about the same duration as the rise time.

To match impedances between the source and the transmission line, place a resistor in series with the driver such that $R_{Series} = Z_0 - R_S$.

To match impedances between the transmission line and the load, place a resistor in parallel with the load such that $R_{Parallel} = (R_L Z_0)/(R_L - Z_0)$.

PCB Routing Topics

There are four areas for electrical considerations when routing your PCB: placing parts, PCB layer stack-up, bypass capacitors, and trace width and spacing width.

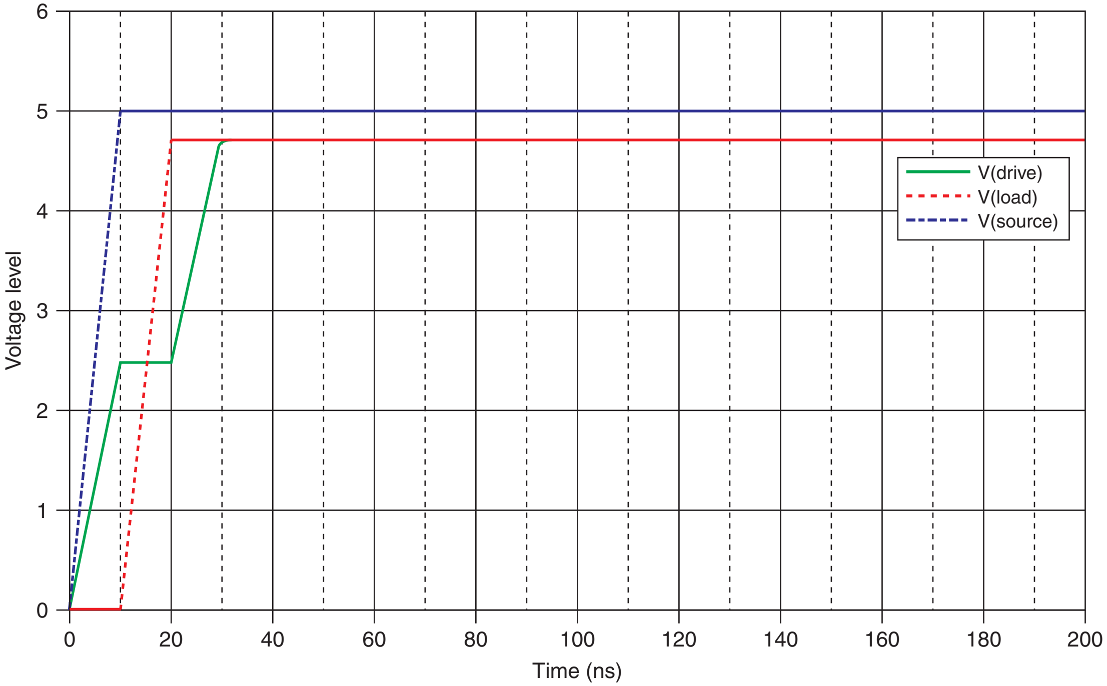


Figure 6-31 Reducing reflections by using a resistor in series with the source.

Parts placement for electrical considerations

Chapter 5 addressed parts placement with manufacturability in mind. Here we consider parts placement with electrical performance in mind. Usually the two goals complement each other, but occasionally they conflict. When conflicts do occur an attempt should be made to resolve the conflict in a way that is mutually beneficial. If that is not possible, electrical considerations usually have priority over mechanical considerations unless doing so will result in a mechanical failure of the board. For example, it may be necessary to manipulate the assembly or soldering processes or place parts on both sides of the board in order to meet manufacturability requirements and meet electrical performance requirements. Whatever solution is chosen the PCB needs to be manufacturable and operational.

Aside from manufacturability goals the first approach to placing parts for electrical considerations is usually determined by the function of the circuit. This is especially true for analog circuits where a signal enters the PCB, flows through the circuitry in more or less a single path (including feedback networks), and then leaves the board. Since analog circuits are susceptible to noise the goal is usually to place the parts to minimize the possibility of degrading the signals. This usually means keeping the parts as close together as possible so that the traces can be as short as possible and keeping the signal path as straight as possible (not zigzagging back and forth or from one side of the board to the other). This approach may increase the size of the board, however, and is not always possible.

With digital circuits it is also desirable to keep related parts close together and lines short, but because digital circuits often contain many parallel paths and branches and may contain wide data busses it may be nearly impossible to do so. Sometimes the best that can be accomplished is to keep parts that are functionally related closer together or place parts together that have the highest speed clocks and rising edges in order to minimize the length of related signal lines.

Mixed signal boards are even more challenging in that both analog and digital circuits and high-power circuits (such as switching regulators) exist on the same board. In these cases the PCB should be segregated into different areas as shown in Fig. 6-32. The topology may vary but the idea is to keep the higher power and other noisy circuitry closer to the connector if possible. This limits the amount of return plane that is utilized by these circuits and therefore minimizes the amount of return plane that is common between them and the rest of the circuitry. Digital and analog circuits should also be kept apart from each other to minimize the effects of switching noise on analog circuitry. When dividing the PCB in this way it is usually necessary (and beneficial) to set up split and isolated plane layers as shown in Fig. 6-15.

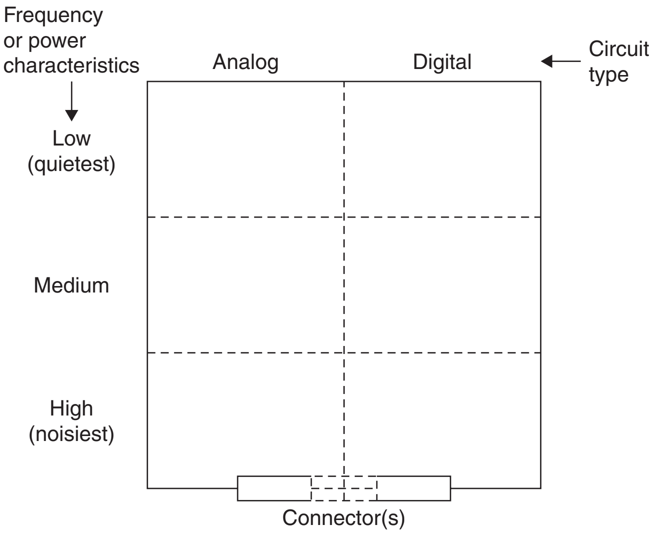


Figure 6-32 Board layout recommendations for noisy circuits.

PCB layer stack-up

The PCB layer stack-up and thickness are assigned to the manufacturer when the board is ordered and not during the routing process in Layout. But the PCB layer stack-up and thickness need to be defined early in the design stage before working in Layout, since the stack-up will determine how many layers to enable and how many power and ground planes to establish. The strategy for stacking up a PCB depends on a number of things such as the capabilities of your board manufacturer, the circuit density (both routing and parts), the frequency (analog) and rise/fall times (digital) of the signals, and the acceptable cost of the board.

As circuits become more dense, additional routing and plane layers are required. Digital circuits commonly require more layers than analog circuits because digital circuits typically consist of parts with greater numbers of pins per chip and because they have a higher number of parallel interconnections. High-speed circuits (whether analog or digital) may require a greater number of layers even if they are not very dense. This is because multilayer boards can provide better impedance control and shielding since they can have additional ground planes. The more layers a board has the more it costs, but once a PCB stack-up exceeds four layers the cost increase per layer usually becomes less for additional layers (to a point). Additionally the benefits of shielding and impedance control can considerably outweigh the increased cost of extra layers.

There are many possible ways to design the stack-up. If the board will be operated at low speeds and in an isolated environment almost anything you can dream up will work. However, as signal speeds increase the layer stack-up and trace routing become increasingly important because a poorly designed stack-up can lead to reflections and excessive EMI radiation (affecting external circuits as well as causing self-inflicted cross talk). A well-designed layer stack-up (and proper routing) not only minimizes the energy it radiates, but also can make your circuit relatively immune from external sources of radiation. In designing a layer stack-up there are only a few guidelines to follow, but they are important. The following few paragraphs and the examples demonstrate the guidelines.

Since PCBs are constructed of double-sided cores bonded together with prepreg, multilayer PCBs usually contain an even number of layers. Odd-layered boards can be made, but in most cases there is no cost benefit to adding only one layer instead of a layer pair (e.g., if you need five layers you may as well go with six). The extra layer can be an extra return/ground plane and the symmetry of an even number of layers helps minimize board warpage.

A signal layer should always be adjacent (and close) to a plane layer (preferably a return/GND plane) to minimize loop inductance, which minimizes electromagnetic radiation and cross talk. Power planes should also be adjacent (and close) to a return plane as this adds interplane capacitance, which helps minimize power supply noise and radiation. If you have to choose between a signal layer being adjacent to the return plane and a power plane being adjacent to the return plane, choose the signal layer. You can add more bypass and bulk capacitors between the power planes to make up for the loss in interplane capacitance.

The following stack-up examples are offered as a reference only. There are many more combinations possible, but only a few are shown here (please see the references for additional examples and details). The final board thickness in the examples is 0.093 in. and the copper is 1 oz (1.35 mils) thick. The availability of certain dimensions will depend on the manufacturer's capabilities and specific processes.

The thicknesses listed in the figures are given to provide perspective. You can use Tables 4-3, 4-4, and 4-5 to get an idea of the different combinations of cores and prepreg types used to make up different layer thicknesses, but remember that the thicknesses from the tables are preassembly thicknesses, and finished thicknesses may vary since traces sink into the soft prepreg, while plane layers do not (see Advanced Circuits Web site for examples of layer thicknesses).

A signal's return current will be on the ground or power plane that is closest to the signal line (if possible), and the relative dimensions determine the trace/plane routing pairs. Ideally all return currents will need to end up at the ground/return pin on the PCB's power connector. It may be beneficial to stack up and route your PCB to *try* to make it easier for the return currents of critical high-speed traces to be paired up with certain ground planes (so that they are not forced to go through capacitor leads or vias to get back to the ultimate return point), but there is no guarantee they will follow it. But remember that to an AC signal there is no real difference between the power plane and the ground plane because they are shorted together with bulk and bypass capacitors. So when signal traces transition from one layer to another the return currents may not have an easy path from one ground plane to another and may choose to return to the source on a power plane until they find a convenient path back to the preferred ground plane through a bypass capacitor. While the return current is not flowing on the preferred plane the impedance of a transmission line can be significantly different from what is expected. To assist the return current in staying with the signal line when it changes layers, return current bridges can be installed by using free vias connected to the ground planes or capacitors with fan-out vias near vias used to transition signals from one layer to another.

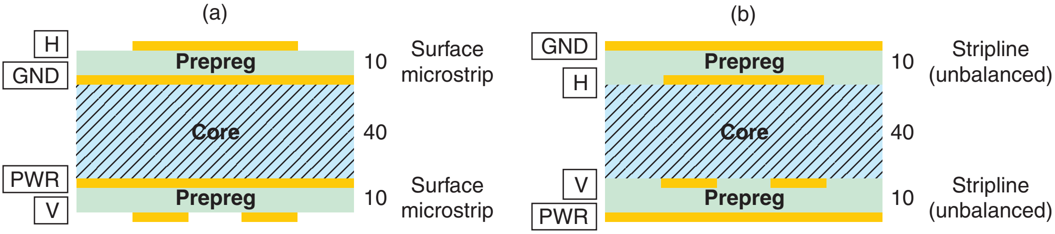
There are several symbols that need to be defined with regard to the stack-up figures. The "H" in the figures implies horizontal routing and the "V" implies vertical routing. In some of the figures an "R" is used to imply nonspecific routing direction. Concentrating the routing strategies in horizontal or vertical directions makes the routing process more efficient in high-density designs and reduces the number of vias required to complete the connections. The symbol "HS" is used to imply high-speed signals that are usually buried between plane layers for extra shielding. The "GND" symbol is used to represent any ground or return plane (for signal or power). The symbols "PWR" or "±PWR" represent any power plane, such as $+5$ V V_{CC} for digital circuits or $+V$ and $-V$ for analog circuits.

There are three basic types of transmission lines: microstrip, stripline, and coplanar. You may not always need a transmission line, but no matter how you route your board one of these types will be represented (even if it is not a close resemblance). Other types of transmission line configurations can be realized by other types of stack-ups, which are not shown here as they will depend on the capabilities and processes of your board manufacturer.

Figure 6-33 shows three different four-layer stack-ups. Indicated thickness is in mils.

Figure 6-33(a) is one of the most common four-layer stack-ups for simple digital or analog PCBs. The land patterns and traces are placed on the outside (top and bottom) of the board and the power and return planes are inside. Placing the traces on the outside enables postfabrication inspection and troubleshooting.

Figures 6-33(b) and 6-33(c) place the power and return planes on the outside of the board and the traces on the inside. This arrangement helps shield the traces from outside EMI and helps contain self-generated radiation between the planes and consequently minimizes radiated EMI. The configuration in Fig. 6-33(c) can be used to route low-density analog circuits that require $+/-V$ for dual-supply op-amps. Power is routed to the amplifiers with wide traces or copper pours and shares the layers used for routing signals.


(a)
H
GND
PWR
V
Prepreg
Core
Prepreg
10
40
10
Surface microstrip
Surface microstrip
(b)
GND
H
V
PWR
Prepreg
Core
Prepreg
10
40
10
Stripline (unbalanced)
Stripline (unbalanced)

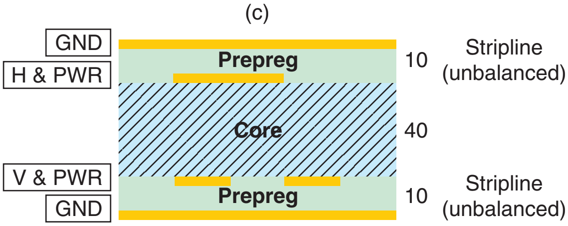
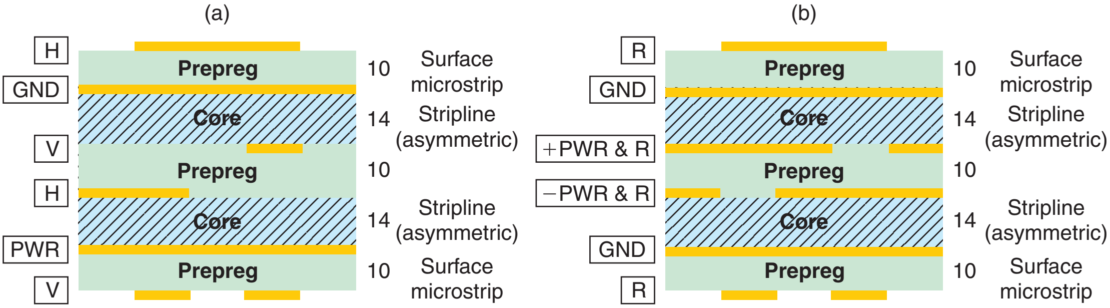

(c)
GND
H & PWR
V & PWR
GND
Prepreg
Core
Prepreg
10
40
10
Stripline (unbalanced)
Stripline (unbalanced)

Figure 6-33 Typical four-layer stack-ups.

Figure 6-34 shows examples of six-layer PCB stack-ups. Figure 6-34(a) is a typical stack-up for digital circuits or analog circuits that do not require dual power supplies. This arrangement provides four routing layers and two plane layers. The inner routing layers can be used for the higher speed signals since they are shielded by the ground and power planes. For analog circuits that require dual power planes, the stack-up in Fig. 6-34(b) provides a highly


(a)
H
GND
V
H
PWR
V
Prepreg
Core
Prepreg
Core
Prepreg
10
14
10
14
10
Surface microstrip
Stripline (asymmetric)
Stripline (asymmetric)
Surface microstrip
(b)
R
GND
+PWR & R
−PWR & R
GND
R
Prepreg
Core
Prepreg
Core
Prepreg
10
14
10
14
10
Surface microstrip
Stripline (asymmetric)
Stripline (asymmetric)
Surface microstrip

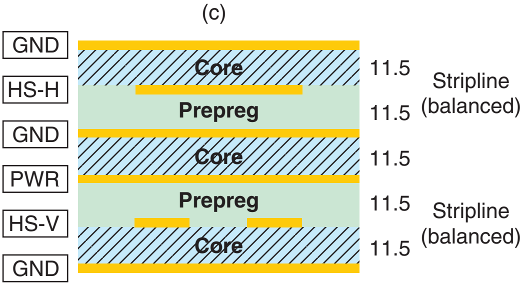

(c)
GND
HS-H
GND
PWR
HS-V
GND
Core
Prepreg
Core
Prepreg
Core
11.5
11.5
11.5
11.5
11.5
Stripline (balanced)
Stripline (balanced)

Figure 6-34 Six-layer stack-up examples.

functional stack-up with two full routing layers, two partial routing layers (which share layers with the +PWR and −PWR layers), and ground planes that are adjacent to all signal and power layers and provide shielding for the inner signal traces. Alternatively the shared power and routing layers can be dedicated to power only, but this limits the board to two routing layers. The stack-up in Fig. 6-34(c) provides two well-shielded, balanced stripline routing layers for high-speed digital circuits and adjacent ground planes for each of the signal and power layers. A limitation of this stack-up is that there are only two routing layers.

Figures 6-35 and 6-36 show examples of 8- and 10-layer stack-ups, respectively. Only a few examples are shown, but by using the different stack-up strategies of the previous examples and capitalizing on the various finished board thicknesses available from most board manufacturers it can be seen that the higher layer stack-ups can provide a multitude of routing possibilities.

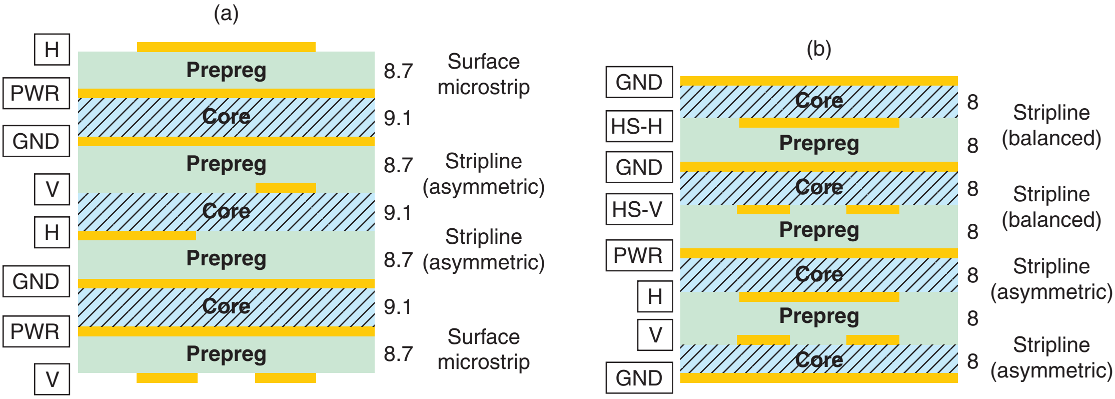

(a)
H
PWR
GND
V
H
GND
PWR
V
Prepreg
Core
Prepreg
Core
Prepreg
Core
Prepreg
8.7
9.1
8.7
9.1
8.7
9.1
8.7
Surface microstrip
Stripline (asymmetric)
Stripline (asymmetric)
Surface microstrip
(b)
GND
HS-H
GND
HS-V
PWR
H
V
GND
Core
Prepreg
Core
Prepreg
Core
Prepreg
Core
8
8
8
8
8
8
8
Stripline (balanced)
Stripline (balanced)
Stripline (asymmetric)
Stripline (asymmetric)

Figure 6-35. Examples of eight-layer PCB stack-ups.

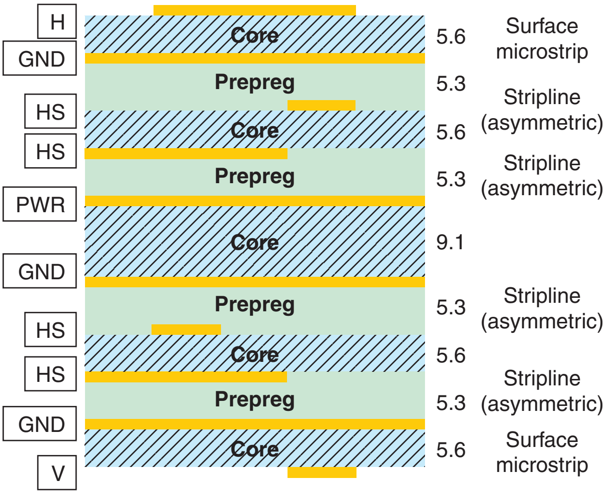

H
GND
HS
HS
PWR
GND
HS
HS
GND
V
Core
Prepreg
Core
Prepreg
Core
Prepreg
Core
Prepreg
Core
5.6
5.3
5.6
5.3
9.1
5.3
5.6
5.3
5.6
Surface microstrip
Stripline (asymmetric)
Stripline (asymmetric)
Stripline (asymmetric)
Stripline (asymmetric)
Surface microstrip

Figure 6-36 A 10-layer PCB stack-up.

Bypass capacitors and fanout

Bypass capacitors serve two main functions, namely to short high-frequency noise to ground and to act as current reservoirs. Consequently there are two basic methods to fanning out power pins. The first method is to route the power pin to the bypass capacitor before the fan-out via and to the power plane as Fig. 6-37(a) shows, and the second method is to route the power pin to the power plane first by placing the fan-out via between the power pin and the bypass capacitor as shown in Fig. 6-37(b). The configuration in Fig. 6-37(b) can also be realized with the shared via (as shown) or when the IC and the capacitor have their own vias.

At first glance there may appear to be no difference electrically speaking, but the differences can be significant at high frequencies and fast rise times. Additionally, other issues such as the method of assembly (wave vs reflow soldering) and the available board real estate often influence orientation and routing of bypass capacitors. Sources in the literature do not all agree with which method is best, but more often Fig. 6-37(a) is recommended for analog circuits and Fig. 6-37(b) for digital circuits.

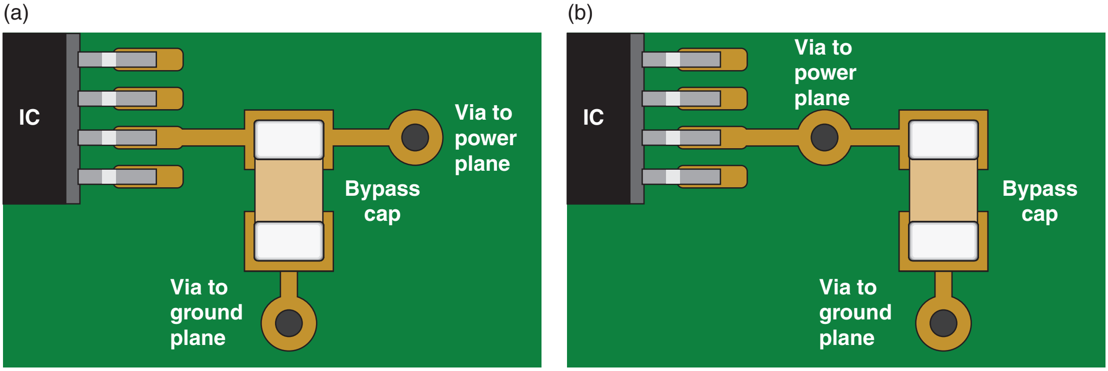


Figure 6-37 Power pin fan-out methodologies. (a) Power pin to bypass capacitor to via. (b) Power pin to via to bypass capacitor.

Trace width for current carrying capability

When current flows through a conductor it will heat up due to I^2R losses. Wider traces exhibit less resistance and therefore less heating. **To determine the minimum trace width** required to minimize heating, determine the maximum current a trace will carry and the thickness of the copper you will use on your board. Use Eq. (17) to calculate the minimum trace width,

$$w = \left[\left(\frac{1}{1.4 \cdot h}\right) \cdot \left(\frac{I}{k \cdot \Delta T^{0.421}}\right)\right]^{1.379}, \tag{17}$$

where w is the minimum trace width (in mils), h is the thickness of the copper cladding (in oz/ft^2), I is the current load of the trace (in amps), $k = 0.024$ is used for inner layers and

$k = 0.048$ is used for outer (top or bottom) layers, and ΔT is the maximum permissible rise in temp (°C) of the conductor above ambient temperature. You can also use the graph shown in Fig. 6-38, which was derived from curves in IPC-2221A.

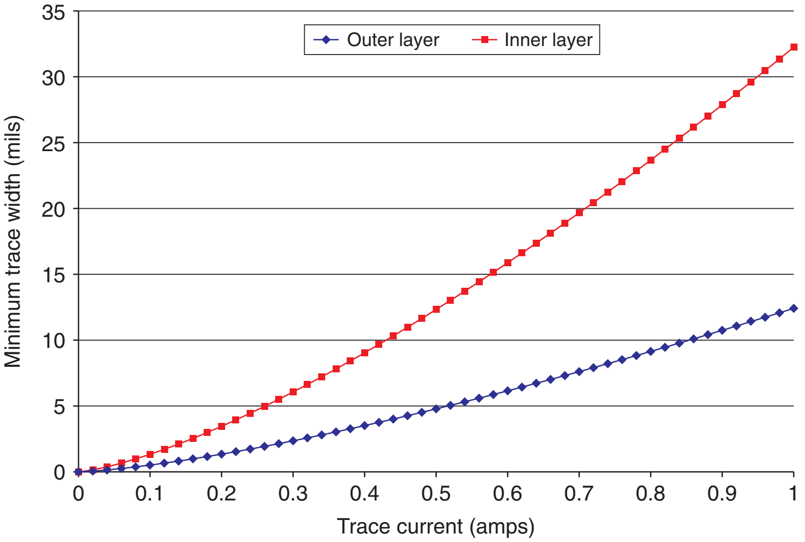


Figure 6-38 Minimum trace widths for 1 oz copper for $\Delta T = 10$°C.

Note 1

- *The glass transition temperature for FR4 is ~125 to 135°C, so as ambient temperature increases, the allowed ΔT decreases and minimum trace width increases. Even if the board will be at room temperature, giving you a $\Delta T = 108$°C, it does not hurt to restrict the temperature rise intentionally just to be safe (e.g., specify $\Delta T = 20$°C even if it could be much higher).*

Note 2

- *Equation (17) was derived from the IPC-2221A standard. Please refer to the standard for the actual equation and additional details.*

You can usually use any of the standard technology files for most small signal applications. Figure 6-38 shows the minimum trace widths for 1 oz inner and outer layer copper with $\Delta T = 10$°C. With 6-mil traces you can run up to about 300 mA on inner traces and about 600 mA on the outer traces, but for manufacturability and reliability considerations they should be as wide as practical. Usually the applications of concern are power supply lines for large circuits and power supply boards in general.

Trace width for controlled impedance

Controlled impedance PCB can be significantly more expensive than standard process PCBs. Before going through the effort and expense of designing controlled impedance transmission lines on the PCB it is a good idea to determine if they are needed by determining if traces are electrically long (and whether controlled impedance is required).

For digital systems, at a minimum, we want the propagation time, PT, to be less than the rise time of the driver (i.e., $PT < ½RT$ or $RT > 2PT$). From the discussion under Reflections another way to look at it is that the length of the trace, L_{trace}, should be less than one-half of the special extent (edge distance) of the rising edge (i.e., $L_{trace} < ½L_{SE}$ or $L_{SE} > 2L_{trace}$). To determine if this condition is met we need to determine RT and PT. RT (or fall time—FT) can be obtained from the data sheet for the device that is driving the trace and will have units of time (e.g., ns). Note that since both the rise and the fall times must fall within limits the smaller value should be used in the calculations. The RT and FT of several logic families are listed in Appendix D.

To calculate PT we need to know the intrinsic propagation delay (t_{PD}), which has units of time/distance. The intrinsic propagation delay for various transmission line configurations is given in Tables 6-6 and 6-7.

Topologies, Z_0, t_{PD}, Trace Width, and Trace Separation Design Equations for Various Transmission Lines

Units for *h*, *w*, and *t* can be mils, cm, in., etc., as long as they are consistent.

Note that in general the values of intrinsic capacitance (C_0) and intrinsic inductance (L_0) are given by [1]

$$C_0 = t_{PD}/Z_0$$

and

$$L_0 = Z_0^2 C_0/1000,$$

where C_0 is in pF/in., t_{PD} is in ps/in., Z_0 is in ohms, and L_0 is in nH/in.

For values of C_0 and L_0 that are specific to particular transmission line topologies, please see the appropriate references as listed.

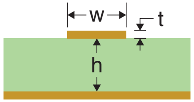
There are two families of transmission lines described here, microstrip and stripline, including their subfamilies, which are as follows:

Microstrip:

1. surface microstrip,
2. surface differential microstrip,
3. embedded microstrip, and
4. embedded differential microstrip.

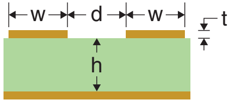
Stripline:

1. balanced (symmetric) stripline,
2. unbalanced (asymmetric) stripline,
3. broadside coupled differential stripline (symmetric), and
4. edge coupled differential stripline (symmetric and asymmetric).

Microstrip transmission lines		Characteristics	Intrinsic propagation delay
Surface	**Topology** 	**Characteristic impedance** $Z_0 = \frac{k}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$ ohms $\boldsymbol{k} = 87$ for $15 < \boldsymbol{w} < 25$ mils [1, 2, 3, 4] $\boldsymbol{k} = 79$ for $5 < \boldsymbol{w} < 15$ mils [3, 4] **Restrictions** $0.1 < \frac{w}{h} < 3.0$ [1] $1 < \varepsilon_r < 15$ [1] **Design equations** Trace routing width to use in Layout $w = 7.475h \cdot e^{\frac{-Z_0\sqrt{\varepsilon_r + 1.41}}{k}} - 1.25t$ (use $\boldsymbol{k} = 87$, then check against width rules, use $\boldsymbol{k} = 79$ if necessary)	$t_{PD} = 84.75\sqrt{0.475\varepsilon_r + 0.67}$ (ps/in.)

Surface differential

Topology



Characteristic impedance

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \text{ ohms}$$

(same as surface microstrip) [5, 6, 7]

$$t_{PD} = 84.75\sqrt{0.475\varepsilon_r + 0.67} \text{ (ps/in.)}$$

Differential impedance

$$Z_{Diff} = 2Z_0\left(1 - 0.48e^{\left(-0.96\frac{d}{h}\right)}\right) \text{ ohm}$$

Restrictions

None specifically noted except as applies to the surface microstrip.

Design equations

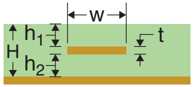
Trace routing width to use in Layout

$$w = 7.475h \cdot e^{\frac{-Z_0\sqrt{\varepsilon_r + 1.41}}{87}} - 1.25t$$

Trace separation:

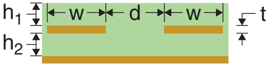
$$d = \ln\left(2.08\frac{-1.04Z_{Diff}}{Z_0}\right)\left(\frac{-h}{0.96}\right)$$

Table 6-6a Microstrip transmission line configurations

Microstrip transmission lines		Characteristics	Intrinsic propagation delay
Embedded	**Topology**  	**Characteristic impedance** $Z_0 = \frac{87}{\sqrt{\varepsilon_r' + 1.41}} \ln\left(\frac{5.98h_2}{0.8w + t}\right)$ (ohms) [2,8,9] where $\varepsilon_r' = \varepsilon_r\left(1 + e^{\left(\frac{-1.55H}{h_2}\right)}\right)$ **OR** $Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h_2}{0.8w + t}\right)\left(1 - \frac{h_1}{0.1}\right)$ (ohms) [1] **Restrictions [8, 10]** $0.1 < w/h_2 < 3.0$ $1 < \varepsilon_r < 15$ Line widths: 0.127 (5 mils) to 0.381 mm (15 mils) Dielectric thickness: 0.127 (5 mils) to 0.381 mm (15 mils) $40 < Z_0 < 90$ ohms **Design equations** Trace routing width to use in Layout $w = 7.475h_2 \cdot e^{-x} - 1.25t$ where $x = \frac{-Z_0\sqrt{\varepsilon_r' + 1.41}}{87}$ for Z_0 from [2, 8, 9] **OR** $Z_0 = \frac{-Z_0\sqrt{\varepsilon_r + 1.41}}{87\left(1 - \frac{h_1}{0.1}\right)}$ for Z_0 from [1]	$t_{PD} = 84.75\sqrt{\varepsilon_r'}$ (ps/in.) OR $t_{PD} = 84.75\sqrt{0.475\varepsilon_r + 0.67}$ (ps/in.) [1]

Embedded differential

Topology



Characteristic impedance

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h_2}{0.8w + t}\right)\left(1 - \frac{h_1}{0.1}\right) \text{ (ohms) [5]}$$

$$t_{PD} = 84.75\sqrt{0.475\varepsilon_r + 0.67}$$

(ps/in.) [5]

Differential impedance

$$Z_{Diff} = 2Z_0\left(1 - 0.48e^{\left(-0.96\frac{d}{h_1+h_2+t}\right)}\right) \text{ (ohms)}$$

Restrictions [5]

Same as embedded microstrip

Design equations

Trace routing width to use in Layout

$$w = 7.475h_2 \cdot e^{-x} - 1.25t$$

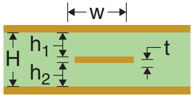
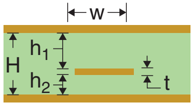
where

$$x = \frac{-Z_0\sqrt{\varepsilon_r + 1.41}}{87\left(1 - \frac{h_1}{0.1}\right)} \text{ [1]}$$

Trace separation of pair:

$$d = \ln\left(2.08 - \frac{1.04Z_{Diff}}{Z_0}\right)\left(\frac{-(h_1 + h_2 + t)}{0.96}\right)$$

Table 6-6b Microstrip transmission line configurations

Stripline transmission lines		Characteristics	Intrinsic propagation delay
Balanced (symmetric)	**Topology** 	**Characteristic impedance** $Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9H}{0.8w + t}\right)$ (ohms) [10,11] **Restrictions** Line widths: 0.127 (5 mils) to 0.381 mm (15 mils) Dielectric thickness: 0.127(5 mils) to 0.381 mm (15 mils) $40 < Z_0 < 90$ ohms **Design equation** Trace routing width in Layout $w = 1.25\left(1.9H \cdot e^{\left(\frac{-Z_0\sqrt{\varepsilon_r}}{60}\right)} - t\right)$	$t_{PD} = 84.75\sqrt{\varepsilon_r}$ (ps/in.)
Unbalanced (asymmetric)	**Topology** 	**Characteristic impedance** $Z_0 = \left(\frac{80}{\sqrt{\varepsilon_r}}\right)\ln\left(\frac{1.9(2h_2 + t)}{0.8w + t}\right)\left(1 - \frac{h_2}{4(H)}\right)$ (ohms) [10, 11]	$t_{PD} = 84.75\sqrt{\varepsilon_r}$ (ps/in.)

Restrictions

$$\frac{w}{h_2 - t} < 0.35$$

$$\frac{t}{h_2} < 0.25$$

Design equation

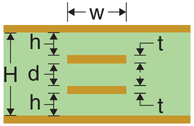
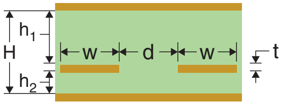
Trace routing width in Layout

$$\boldsymbol{w} = 2.375(2\boldsymbol{h}_2 + \boldsymbol{t})\boldsymbol{e}^{-x} - 1.25\boldsymbol{t}$$

where

$$x = \frac{Z_0\sqrt{\varepsilon_\mathrm{r}}}{80\left(1 - \dfrac{h_2}{4H}\right)}$$

Table 6-7a Stripline transmission line configurations

Stripline transmission lines		Required trace width (in) for desired Z_0 and/or Z_{Diff}.	Intrinsic propagation delay
Broadside coupled differential stripline (symmetric) [12]	**Topology**  	**Characteristic (between conductors) impedance** $Z_0 = \frac{82.2}{\sqrt{\varepsilon_r}}\ln\left(\frac{5.98d}{0.8w+t}\right)(1-e^{(-0.6h)})$ (ohms) **Restrictions** None given in the references **Design equations** Trace routing width to use in Layout $w = 7.475d \cdot e^{-x} - 1.25t$ where $x = \frac{Z_0\sqrt{\varepsilon_r}}{82.4(1-e^{-0.6h})}$	$t_{PD} = 84.75\sqrt{\varepsilon_r}$ (ps/in.)
Edge coupled **differential stripline [12]** For symmetric ($h_1 = h_2$) or asymmetric ($h_1 \neq h_2$) For symmetric ($h_1 = h_2$)	**Topology**  	**Characteristic impedance** For symmetric ($h_1 = h_2$) $Z_0 = \frac{60}{\sqrt{\varepsilon_r}}\ln\left(\frac{1.9H}{0.8w+t}\right)$(ohms) For symmetric ($h_1 \neq h_2$) $Z_0 = \left(\frac{80}{\sqrt{\varepsilon_r}}\right)\ln\left(\frac{1.9(2h_2+t)}{0.8w+t}\right)\left(1-\frac{h_2}{4(H)}\right)$(ohms)	$t_{PD} = 84.75\sqrt{\varepsilon_r}$(ps/in.)

Differential impedance (both)

$$Z_{\text{Diff}} = 2Z_0\left(1 - 0.374e^{\left(-2.9\frac{d}{H}\right)}\right)$$

Design equations

Trace routing width to use in Layout

For symmetric ($h_1 = h_2$)

$$w = 1.25\left(1.9H \cdot e^{\left(\frac{-Z_0\sqrt{\varepsilon_r}}{60}\right)} - t\right)$$

For asymmetric ($h_1 \neq h_2$)

$$w = 2.375(2h_2 + t) \cdot e^{-x} - 1.25t$$

where

$$x = \frac{Z_0\sqrt{\varepsilon_r}}{80\left(1 - \frac{h_2}{4H}\right)}$$

Trace separation in layer stack-up (for symmetric or asymmetric)

$$d = -0.347\ln\left(2.67\left(1 - \frac{Z_{Diff}}{2Z_0}\right)\right)$$

Table 6-7b Stripline transmission line configurations

Next calculate the propagation time, PT, using Eq. (18),

$$\mathrm{PT} = L_{\mathrm{trace}} \times t_{\mathrm{PD}}, \tag{18}$$

where PT is a trace's one-way propagation time, L_{trace} is the length of the trace as measured on the PCB, and t_{PD} is the intrinsic propagation delay from Tables 6-6 and 6-7.

If it is determined that the trace is electrically too long then either it needs to be shortened or the impedances need to be matched. To determine the maximum allowable trace length use Eq. (19).

Since we want $\mathrm{PT} < \frac{1}{2}\mathrm{RT}$ and $\mathrm{PT} = L_{\mathrm{trace}} \times t_{\mathrm{PD}}$, then

$$L_{\mathrm{trace}} < \frac{\mathrm{RT}}{2t_{\mathrm{PD}}}. \tag{19}$$

For analog systems we determine the critical length of a trace with respect to the wavelength rather than the rising edge. The wavelength, λ, is determined using Eq. (20),

$$\lambda = \frac{v_{\mathrm{P}}}{f}, \tag{20}$$

where v_{P} is the intrinsic propagation velocity ($v_{\mathrm{P}} = 1/t_{\mathrm{PD}}$) and f is the frequency of the signal on the trace.

Various trace length limits are stated in the literature: anywhere from $L_{\mathrm{trace}} < 1/6\lambda$ to $L_{\mathrm{trace}} < 1/20\lambda$. IPC-2251 recommends $L_{\mathrm{trace}} < 1/15\lambda$, where L_{trace} is the length of the trace as measured on the PCB and λ is the wavelength of the highest frequency component of the signal (the shortest wavelength).

Tables 6-6 and 6-7 can be used to determine t_{PD} (ps/in.) for critical length calculations for both analog and digital circuits. If it is determined (using Eq. (19) or (20)) that a trace is electrically long, then source and load resistance and the transmission line impedance need to be controlled.

To design a controlled impedance transmission line on a PCB use Tables 6-6 and 6-7 to determine the trace width, w (in.). The trace thickness, t (oz/ft^2), dielectric thickness, h (mils), and dielectric constant, ε_r (unitless), are determined by your board manufacturer.

There is another type of transmission that is not in Tables 6-6 and 6-7: the coplanar transmission line is shown in Fig. 6-39. Typically $d < h$, and w is relatively wide compared to the other configurations. The copper along each side of the trace is a topside return plane and is typically $>5w$ in both directions. The bottomside return plane is not present in some applications.

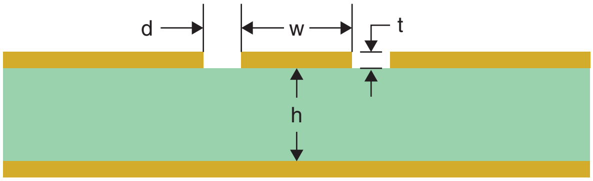


Figure 6-39 A coplanar transmission line.

The equations are not well documented in the literature for this type of coplanar configuration except in the *Transmission Line Design Handbook*, by Brian C. Wadell. The equations are not presented here because they are rather unwieldy, and this type of transmission line is not widely used on FR4. If you need to use this type, please see the reference for a full description of its design, use, and limitations. An approximation of this type of configuration is sometimes attempted using guard traces and copper pours, but because of the relative dimensions (i.e., $h < d$ or $h \approx d$) an accidentally designed surface microstrip is usually the result.

Trace spacing for voltage withstanding

There are two reasons for controlling the spacing between traces: (1) to ensure adequate voltage-withstanding capability (insulation resistance) between high voltage lines and (2) to minimize cross talk between signal lines. Table 6-8, which is an abridged version of a similar table given in IPC-2221A (Table 6-1), shows the required trace spacing for various voltage ranges on internal and external layers. The spacing on external traces depends on both the voltage and the external coating of the board.

Voltage between conductors (V_{DC} or $V_{P\text{-}P}$)	**Internal traces**	**External traces**		
		Bare	**Soldermask only**	**Conformal coating**
0–15	2	4	2	5
16–30	2	4	2	5
31–50	4	24	5	5
51–100	4	24	5	5

After IPC-2221A.

Table 6-8 Minimum Conductor Spacing (Mils)

Trace spacing to minimize cross talk (3*w* rule)

The typical trace spacing used in Layout is shown in Fig. 6-40(a), in which the edge-to-edge spacing between traces is typically one conductor width. If a trace is susceptible to crosstalk from adjacent traces then it should be kept a minimum of two trace widths (edge to edge) from the other traces, as shown in Fig. 6-40(b). This is referred to in the references as the

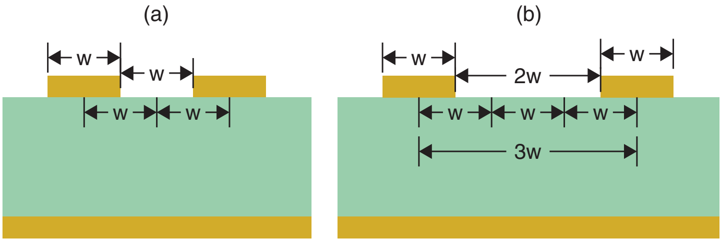
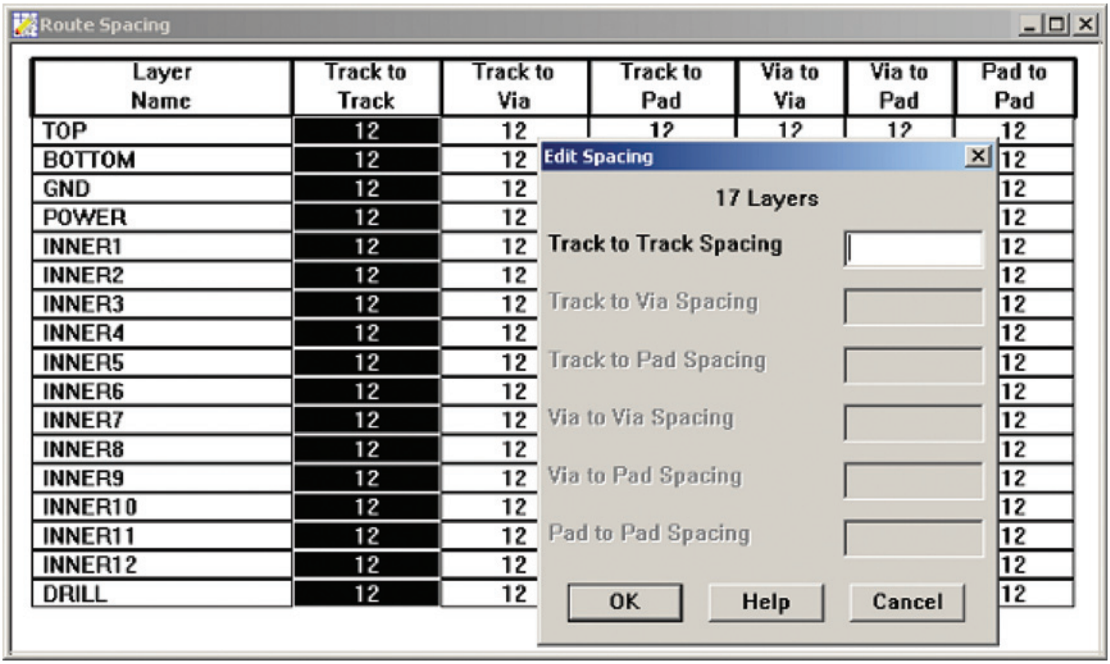


Figure 6-40 Trace spacing methods. (a) Typical trace spacing. (b) 3w spacing to minimize cross talk.

3*w* rule because the center-to-center spacing is 3*w*, as indicated in Fig. 6-40(b). At 3*w*, the traces are out of reach of about 70% of each other's magnetic field if the traces are controlled impedance transmission lines (or reasonable approximations). Keeping the traces 10*w* apart at the centers will keep the traces out of about 98% of each other's field (Montrose 1999, p. 210).

To adjust the trace-to-trace spacing in Layout go to Options → Global spacing to display the Route Spacing spreadsheet as shown in Fig. 6-41. Double click the Track to Track column header and enter the *edge to edge* spacing in the box. Click OK.



Layer Name	Track to Track	Track to Via	Track to Pad	Via to Via	Via to Pad	Pad to Pad
TOP	12	12	12	12	12	12
BOTTOM	12	12				12
GND	12	12				12
POWER	12	12				12
INNER1	12	12				12
INNER2	12	12				12
INNER3	12	12				12
INNER4	12	12				12
INNER5	12	12				12
INNER6	12	12				12
INNER7	12	12				12
INNER8	12	12				12
INNER9	12	12				12
INNER10	12	12				12
INNER11	12	12				12
INNER12	12	12				12
DRILL	12	12				12

Edit Spacing

17 Layers

Track to Track Spacing

Track to Via Spacing

Track to Pad Spacing

Via to Via Spacing

Via to Pad Spacing

Pad to Pad Spacing

Figure 6-41 Setting the trace spacing in Layout.

Traces with acute and 90° angles

Routing high-frequency analog or high-speed digital traces with acute or 90° angles has long been discouraged, but not everyone agrees anymore as to how much of a problem it really is (see Jonson and Graham, p. 174; Montrose 2000, p. 220; Bogatin, p. 317; and Brooks, p. 383). The argument is that the trace width increases by a factor of 1.414 at the corner of the trace (as shown in Fig. 6-42) and causes a change in the characteristic impedance (due to an increase in capacitance) of the trace. As discussed above and demonstrated in Chap. 11 impedance mismatches cause reflections. The reflections in turn cause ringing in digital circuits with fast rise times and standing or traveling waves in high-frequency analog circuits. In theory then, 90° corners should be avoided—at least when routing controlled impedance transmission lines.

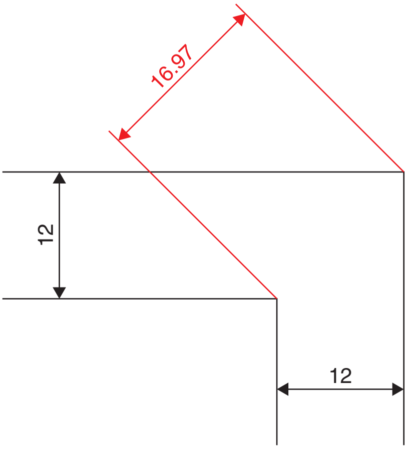


Figure 6-42 Trace geometry of a sharp 90° corner.

A look through the references shows that when using high-end network analyzers and time domain reflectometers to measure the reflection from a 90° corner the effects are evident (Bogatin, p. 318). However, the frequencies at which the reflections occur are high (into the upper GHz for traces greater than 50 mils wide and THz for traces less than 10 mils), and compared to other sources of impedance discontinuities (such as vias) the effects are insignificant.

Another thing to consider is that (with Layout anyway) the corners are not as sharp as shown in Fig. 6-42. Recall from Chap. 1 that pads and traces are drawn as flashes or draws, respectively, by photoplotters with apertures of a given diameter. While square apertures can be used (and are for square pads), Layout uses round apertures for traces in the Gerber codes. A 90° corner produced by Layout is shown in Fig. 6-43(a). Although the corner may look fairly sharp, a close-up of the corner shown in Fig. 6-43(b) shows that the outer edge is rounded and only the inner corner is square. This results in a smaller increase in width than with a square corner.

The difference between a 12-mil trace and a 17-mil trace (at the sharp corner in Fig. 6-42) is about 11.5 Ω for a dielectric constant of 4.2 and a core thickness of 10 mils, and the difference between the 12-mil trace and a 14.5-mil trace (at the rounded corner in Fig. 6-43) is about 6.2 Ω. However, the effect of extra width (and change in impedance) is very small. The excess area shown in Fig. 6-43(b) is 7.73 mils^2 for a 12-mil trace. If the equivalent area is

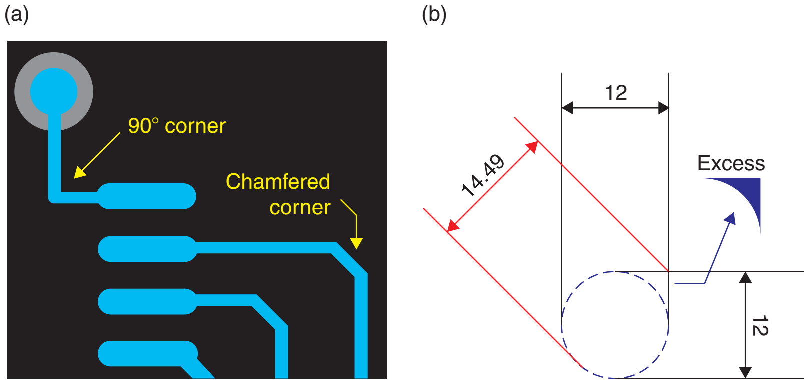


Figure 6-43 Geometry of a 90° corner in Layout. (a) 90° and chamfered corners. (b) Excess copper at a 90° corner.

divided by 2 and each piece is placed on either side of a straight segment of a 12-mil trace (as indicated by the arrow in Fig. 6-44) it is clear that the excess area created by the 90° corner is insignificant compared to other factors such as vias and land patterns. The via shown in the figure is the default VIA1 from the 1bet_any technology file. The literature (Brooks, p. 385) suggests that even acute angles of 135° can be used up to about 1 GHz.

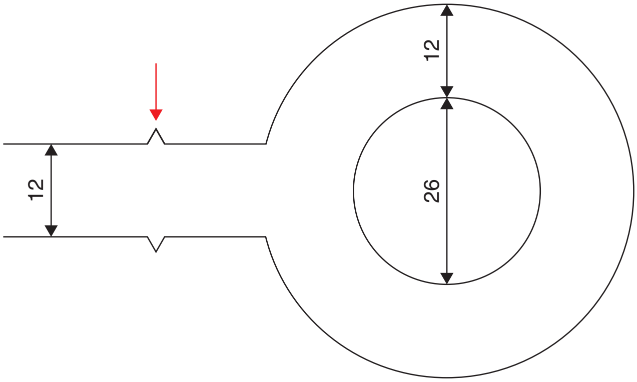


Figure 6-44 Excess area compared to a typical via (Brooks, p. 383; Johnson and Graham, p. 174; Montrose 1999, p. 220; Bogatin, p. 315)

CHAPTER 7

Making and Editing Capture Parts

Capture provides many libraries of parts that you can use to build your schematic, perform simulations, and generate PCB layouts. However, you will need to make your own parts at some point. There are a couple of ways of working with the part libraries. You can build custom parts and save them to existing or new libraries, or modify existing parts and save them to a library, or modify and save parts to just a specific project. Whether you decide to build custom parts or modify existing ones, you need to know about the libraries, the different ways of making parts, how different parts are packaged, what types of pins to use with different parts, and how to connect them properly for board layout and simulation purposes.

The Capture Part Libraries

In the full version of Capture there are 141 parts libraries in the Capture libraries, with 108 PSpice libraries and 34 libraries in the main Capture library, and each library contains many parts. As mentioned in Chap. 2, there are two parts libraries that are supplied with the software, both of which are located in the Capture folder. One type of parts and a PSpice folder are located inside the Capture Library folder. The parts located immediately inside the Capture Library folder are schematic parts that do not have footprints or PSpice models associated with them, but the parts located in Capture's PSpice folder have PSpice models and footprints associated with them. For the purpose of board layout, it does not matter from which library you select parts because it is a simple matter of assigning (or changing) a footprint regardless of which library it came from. Assigning PSpice simulation capabilities to a part is another matter altogether and is discussed later in this chapter.

The libraries are fairly well labeled and, in most cases, particular parts are relatively easy to find. However, there is some overlap between some of the libraries (especially the PSpice libraries), which can make searching for parts in general less than straightforward. For example MOSFET transistors can be found in the discrete.olb and the fairchild.olb libraries, the infineon_x.olb series libraries, and the jpwrmos.olb library, to name a few. Some of the libraries contain mixtures of parts (anlg_dev.olb contains amplifiers, multipliers, and multiplexers), while others contain only certain types of parts (fairchild.olb only contains FETs). So at times you may have to search manually through the libraries to find parts. The first place to begin searching is to open the PSpice library list (lib_list.pdf) located in the lib_list folder in the OrCAD/Doc path. The lib_list lists all of the OrCAD parts in two sections; the first section lists parts by device type and the second section by part library. Using the PDF search tool you can quickly search the entire library list (all 1123 pages).

If you cannot find the part you are looking for in the lib_list or in the actual parts libraries, you may be able to download parts and models from the Internet. Several semiconductor manufacturers generate their own parts and models and provide them free of charge from their Web sites.

If you cannot locate a ready-made part, you will need to make your own. It is highly recommended that you make your own folders and libraries to save your parts in, rather than adding parts to the libraries supplied with the software. Instructions on how to create Capture parts and PSpice models are provided below. You can find additional information on the subject in the Capture and PSpice user's guides in the document folders and on the frequently asked questions (FAQ) section of the OrCAD Web site.

Types of Packaging

Inside one package there can be one or more parts. The parts can all be the same (homogeneous), or the parts can be different (heterogeneous), and either type of part can be passive or active.

Homogeneous parts

Figure 7-1 shows examples of homogeneous packages (a single bipolar junction transistor and a digital IC with four identical NAND gates). In both cases all of the parts within a package are identical (even if there is only one). All of the gates in the IC are active and have to share the two power pins (7 and 14). Homogeneous parts can be placed independently in a schematic. Setting up the gates to share the power pins at the schematic level and the board level is addressed below.

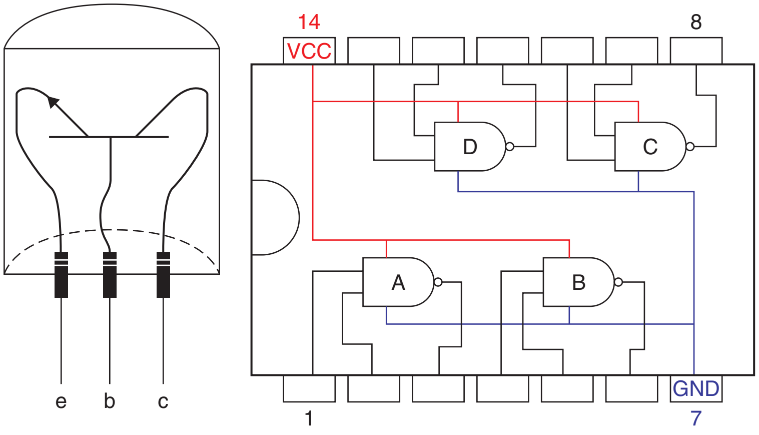


Figure 7-1 Homogeneous—one or more identical parts in a package.

Heterogeneous parts

Figure 7-2 shows an example of a heterogeneous package. This package has three parts, which can be placed independently on the schematic: one relay coil (K) and two sets of contacts (A and B). Although power can be applied to the coil and to one or more of the contacts, it is a passive device and does not have power pins (strictly speaking).

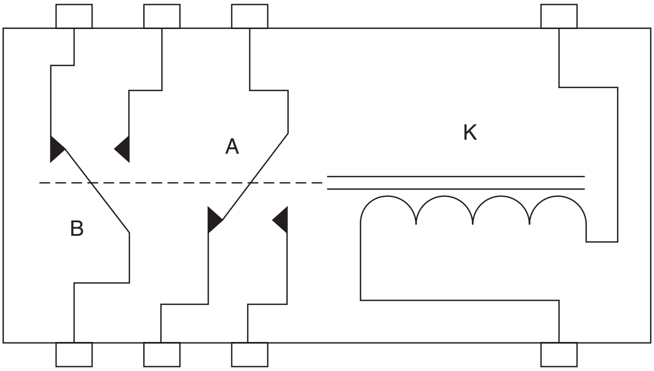


Figure 7-2 Heterogeneous relay—dissimilar parts in a single package.

Pins

When making parts in Capture that will be used to make a PCB design in Layout or perform simulations in PSpice, one of the most important issues in making new parts is properly handling the pins. All of the other lines that make up a part are cosmetic, but how the pins are assigned will determine if you get design rule check errors when checking your schematic, if you will have a PCB laid out correctly, and if a design will simulate correctly.

There are eight different types of pins. Each pin has a pin number, a pin name, and an order number. Each of these pins also has specific characteristics that determine how it performs in the package with regard to what it looks like in the schematic, how it is “judged” during design rule checks, how routing is governed in Layout, etc. Additionally, you can assign pin characteristics that determine what the pins look like once the part is placed into a schematic. Table 7-1 shows a summary of the pin types, shapes, and visibility options.

With regard to PCB layout the pin types are simply power pins and nonpower pins (any of the other types). Power pins require special handling because of their global nature. For example, it needs to be considered if any of the pins will be shared between parts within one package, if they will be visible on all the parts, and if they will be connected to a global net or a nonglobal net. Examples that explain how to deal with pins are given below.

Pin types	Pin shapes	Visibility settings
Power/GND	Clock	A pin's number
Three-state	Dot	A pin's name
Bidirectional	Dot–clock	The pin itself[a]
Open collector	Line	
Open emitter	Short	
Input	Zero length	
Ouput		
Passive		

[a] Applies to power pins only. All other pins are always visible.

Table 7-1 Pin types and attributes

Part Editing Tools

Before we begin making parts we will take a quick look at the part editing tools.

The Select tool and settings

Select tool

The Select tool is used to select pins, text, or any of the graphical objects (lines, arcs, etc.). You can select objects by clicking on them or by dragging a box across or around objects (see Area Select description below).

Snap to Grid

The Snap-to-Grid function is actually a coarse or fine setting and never actually fully disables the snap-to functionality. If the Snap-to-Grid function is active (coarse setting) you can place or move objects only in 0.1-unit increments—this is the default. If the grid function is not active (fine setting) you can place or move objects in 0.01-unit increments. Except when working with graphics, the Snap to Grid should always be active.

Area Select

Objects can be selected by fully enclosing the object with a selection box (using the Select tool) or by just intersecting the object with the selection box. Using the fully enclose method is handy for selecting an object that is surrounded by many closely located objects.

The pin tools

Place Pin tool

The Place Pin tool is used to place pins on a part one at a time.

Place Pin Array tool

The Array tool is used to simultaneously place multiple pins on a part such as a 16-bit output port on a microcontroller. The Array tool enables you to establish a base name that is common to all of the pins and then automatically number each pin chronologically.

The graphics tools

Place Line tool

The Line tool is used to place a single orthogonal or diagonal line segment.

Place Polyline tool

The Polyline tool is used to place multisegment lines. Polylines are orthogonal by default, but can be made diagonal by holding down the Shift key on the keyboard while drawing the line.

Place Rectangle tool

Used to place closed rectangular parallelograms.

Place Ellipse tool

Used to place circles and ellipses.

Place Arc tool

Used to construct arcs and circles.

Place Text tool

Used to place text objects, which have font, color, and rotation settings.

The zoom tools

Zoom In

Zooms in by set increments. You can use the button or press the I key on your keyboard or select Zoom In from the View menu.

Zoom Out

Zooms out by set increments. You can use the button or press the O key on your keyboard or select Zoom Out from the View menu.

Zoom to Region

Use this tool to zoom to a particular region of your design by dragging a box around the area you want to zoom to.

Zoom to All

Use this tool to see the entire design.

Constructing Capture Parts

There are four methods to construct Capture parts. Three of the methods are completed from the Capture Library Manager and the fourth is initiated from the PSpice Model Editor and finished with the Capture Library Manager. PCB footprints can be assigned to any of the parts regardless of how they are constructed, and the footprints can be assigned when the parts are first constructed or not assigned until later when the parts are actually used in a design.

Methods from Capture Library Manager:

1. Design menu → New part,
2. Design menu → New part from spreadsheet,
3. Tools menu → Generate part.

Method from PSpice Model Editor:

4. File menu → Create Capture parts (then use the Capture Library Manager to modify the part's appearance).

Table 7-2 shows which method to use by how the part will be used. The procedure for each method is described below. Later in the chapter it will be shown how to make and download PSpice models, which can be converted to Capture parts using Methods 3 and 4.

Function/purpose of the part	Method of construction
Schematic entry only	Method 1 (easiest) or Method 2
Schematic entry and PCB layout	Method 1 (easiest) or Method 2
Schematic entry and PSpice simulation using functional OrCAD schematic designs (can also assign footprints for PCB layout)	Method 3 (easier) or Method 4
Schematic entry and PSpice simulation using new or existing PSpice models (can also assign footprints for PCB layout)	Method 4

Table 7-2 Methods of constructing parts

Method 1: Constructing Parts Using the New Part Option (Design Menu)

Constructing parts using the New Part option in Capture will be demonstrated through three design examples. The first two examples will be used to design homogeneous parts; the first will be a transformer (a single-part, passive device) and the second will be an operational amplifier (a multipart, active device) with shared power pins. The third example will be a heterogeneous, multipart, passive device.

Design example for a passive, homogeneous part

The first design example is of a transformer with an iron core, a single primary, and a center-tapped secondary. The transformer and its schematic representation are shown in Fig. 7-3.

To begin, start Capture and from the session frame navigate to File → New → Library as shown in Fig. 7-4.

The window that opens is the Capture Library Manager. Select the Library icon (Fig. 7-5(a)) and then select New Part from the Design menu (Fig. 7-5(b)) or right click and select New Part from the pop-up menu.

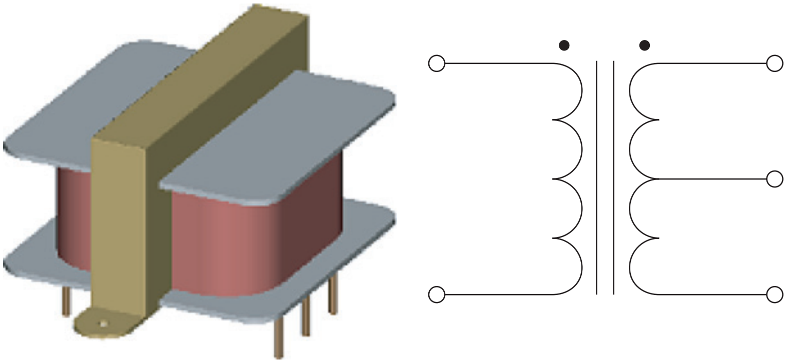


Figure 7-3 Single-part, homogeneous transformer and schematic.

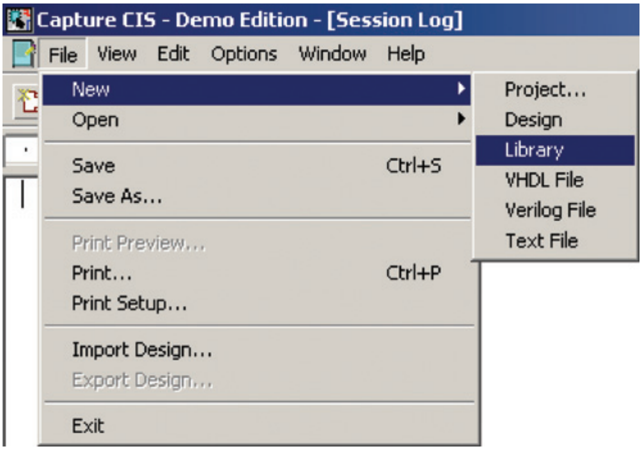

Capture CIS - Demo Edition - [Session Log]
File
View
Edit
Options
Window
Help
New
Open
Save
Ctrl+S
Save As...
Print Preview...
Print...
Ctrl+P
Print Setup...
Import Design...
Export Design...
Exit
Project...
Design
Library
VHDL File
Verilog File
Text File

Figure 7-4 Starting a new part from a new Capture library.

A **New Part Properties** dialog box will open as shown in Fig. 7-6. Enter a name for the part (for example, XFMR S_Pri:CT_Sec) and "T" for the reference prefix. You can also enter a PCB footprint if desired (or known). Leave the Parts per Pkg: as 1 and Package Type as **Homogeneous.** Select Part Numbering as **Numeric** and check **Pin Number Visible** if you want the pin numbers to be visible on the schematic. You can change this later if you are not sure what the footprint is or will be. Click **OK.**

A part editing window will open with a dotted outline as shown in Fig. 7-7. The dotted box defines the boundary of the part. Pins are placed on the boundary (as described below) and text and graphics are placed inside the boundaries. You can also add pictures and IEEE symbols if desired.

The default grid is 0.1 × 0.1 in., with the upper left corner as coordinate (0,0). By default pins and graphical objects are placed on the grid. The snap-to-grid setting can be changed by toggling the Snap-to-Grid tool on, , or off, . The default grid is shown as dots, but

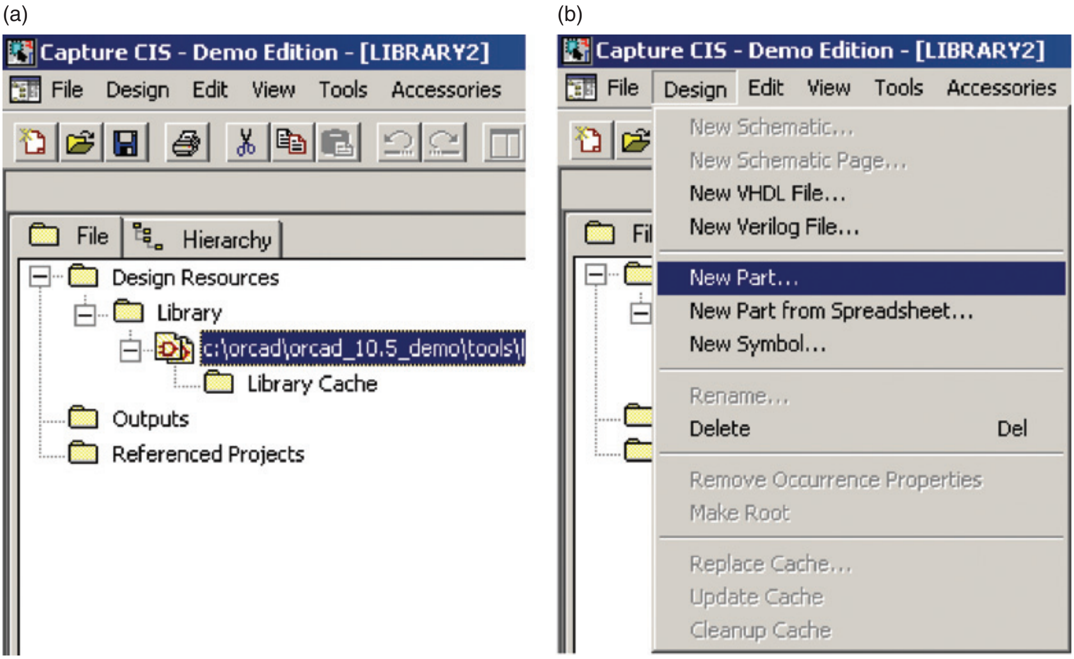
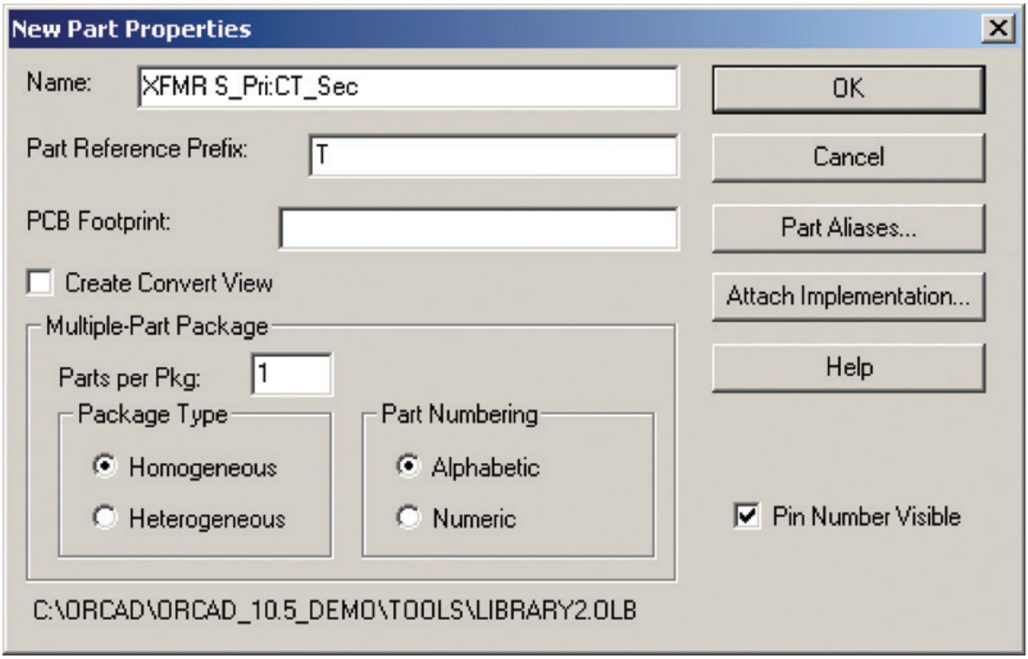

(a)
Capture CIS - Demo Edition - [LIBRARY2]
File
Design
Edit
View
Tools
Accessories
File
Hierarchy
Design Resources
Library
c:\orcad\orcad_10.5_demo\tools\l
Library Cache
Outputs
Referenced Projects
(b)
Capture CIS - Demo Edition - [LIBRARY2]
File
Design
Edit
View
Tools
Accessories
New Schematic...
New Schematic Page...
New VHDL File...
New Verilog File...
New Part...
New Part from Spreadsheet...
New Symbol...
Rename...
Delete
Del
Remove Occurrence Properties
Make Root
Replace Cache...
Update Cache
Cleanup Cache

Figure 7-5 Beginning a new part from the Library Manager.


New Part Properties
OK
Cancel
Part Aliases...
Attach Implementation...
Help

Name: XFMR S_Pri:CT_Sec

Part Reference Prefix: T

PCB Footprint:

☐ Create Convert View

Multiple-Part Package

Parts per Pkg: 1

Package Type

● Homogeneous

○ Heterogeneous

Part Numbering

● Alphabetic

○ Numeric

☑ Pin Number Visible

C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\LIBRARY2.OLB

Figure 7-6 ***New Part Properties*** *dialog box.*

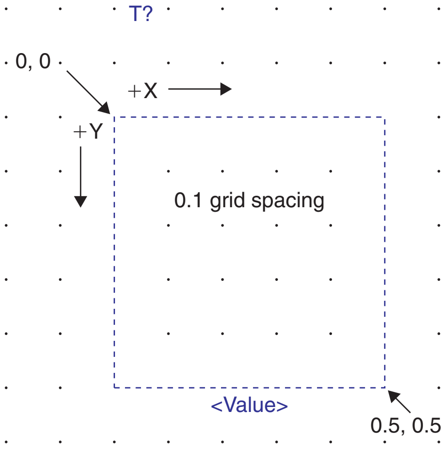
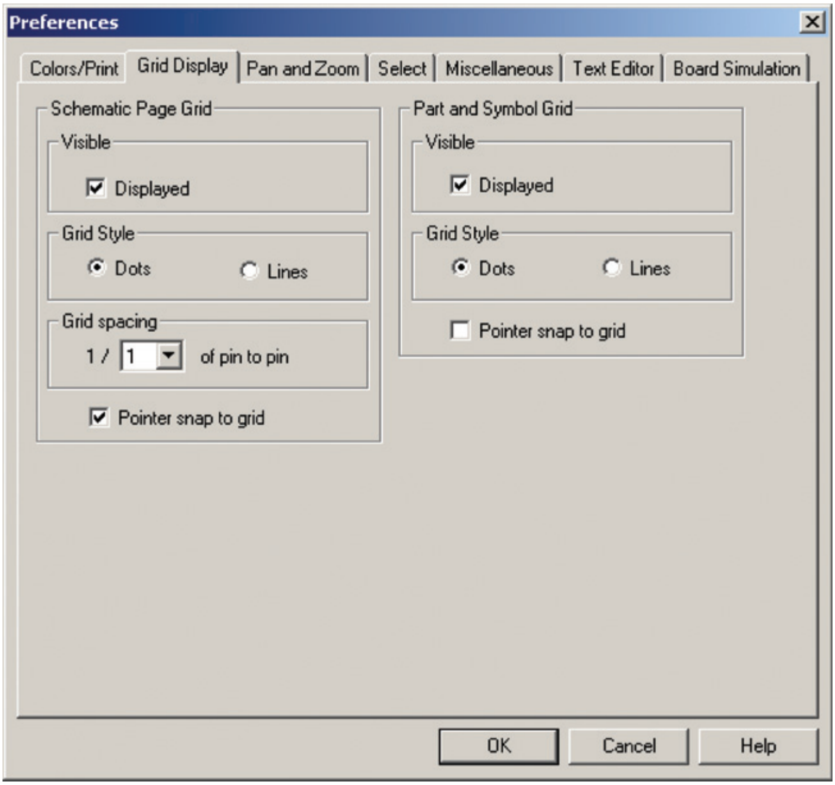


Figure 7-7 The new part shown in the part editing window.

you can change it to lines if so desired. **To make changes to the grid settings**, navigate to Options → Preferences from the menu bar and select the Grid Display tab as shown in Fig. 7-8. Select the desired part and symbol grid properties on the right side of the dialog box.


Preferences

Colors/Print | Grid Display | Pan and Zoom | Select | Miscellaneous | Text Editor | Board Simulation

Schematic Page Grid
Visible
☑ Displayed
Grid Style
● Dots ○ Lines
Grid spacing
1 / 1 of pin to pin
☑ Pointer snap to grid

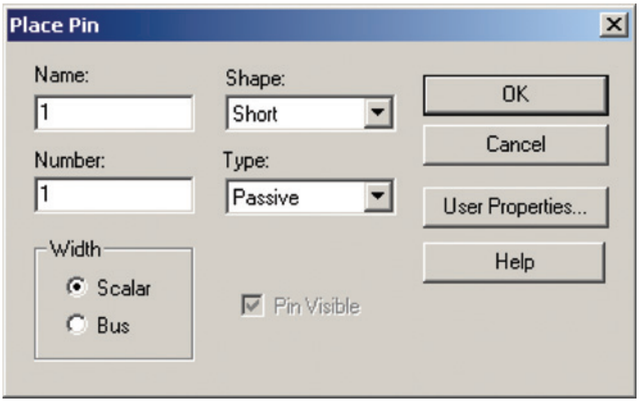
Part and Symbol Grid
Visible
☑ Displayed
Grid Style
● Dots ○ Lines
☐ Pointer snap to grid

OK Cancel Help

*Figure 7-8 Grid settings in **Options** → **Preferences** dialog box.*

The first step to make the transformer is to make the part outline 0.4 in. wide by 0.6 in. tall (for comparison, resistors from the Analog library are 0.2 × 0.2 in.—not including the pin lengths). **To resize the part outline** left click on the dotted border and then click to hold one of the corner squares (handles) and drag the corner to resize the box.

The next step is to add the pins that will make the transformer's five leads. **To add pins to the part**, toggle the pin tool, . The Place Pin dialog box shown in Fig. 7-9 will be displayed.



Name: 1

Number: 1

Shape: Short

Type: Passive

Width
● Scalar
○ Bus

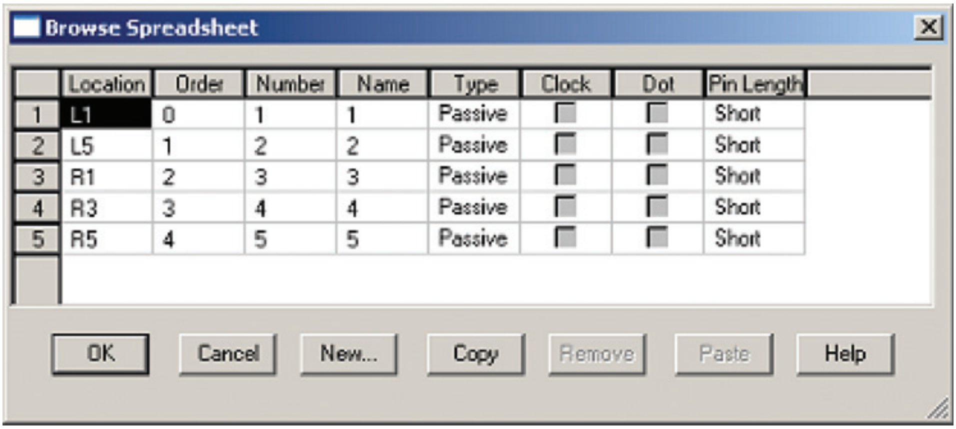
☑ Pin Visible

*Figure 7-9 The **Place Pin** dialog box.*

Select Short for the pin shape and Passive for the pin type; click OK. Place the first two pins on the left side of the border at positions (0.0, 0.1) and (0.0, 0.5) for the primary winding leads and three pins on the right side at positions (0.4, 0.1), (0.4, 0.3), and (0.4, 0.5) for the secondary winding leads. To quit placing pins press the Esc key on the keyboard or right click and select End Command from the pop-up.

The Place Pin tool will automatically increment the name and number of each pin as it is placed. **To change a name or number of a pin**, double click on a pin to bring up the Pin Properties dialog box (which looks exactly like the Place Pin dialog box) and change it as necessary. **To simultaneously change the properties of multiple pins** hold down the Ctrl key and left click each pin to select more than one pin. Then right click and select Edit Properties... from the pop-up menu. The Browse Spreadsheet dialog box shown in Fig. 7-10 will be displayed. More than one pin must be selected to get the spreadsheet, otherwise the Pin Properties dialog box will be displayed.

The pin type and pin length cells have dropdown lists that allow you to select the desired pin properties. The other columns require you to enter the values manually. The number and name are the same as the settings you can choose using the Pin Properties dialog box. Naming pins is flexible, but the **pin numbers you assign in a Capture part must match the pad name in a Layout footprint**. For PCB layout considerations, the pin order is irrelevant. The pin order is extremely important to PSpice, however, and will be discussed in Methods 3 and 4 below.



	Location	Order	Number	Name	Type	Clock	Dot	Pin Length
1	L1	0	1	1	Passive	☐	☐	Short
2	L5	1	2	2	Passive	☐	☐	Short
3	R1	2	3	3	Passive	☐	☐	Short
4	R3	3	4	4	Passive	☐	☐	Short
5	R5	4	5	5	Passive	☐	☐	Short

*Figure 7-10 Use the **Browse Spreadsheet** dialog box to modify pin parameters.*

The next step is to **place graphics** to build the transformer coils. Turn the Snap to Grid off (toggle the button so that it turns red). Select the Place Arc tool, . Arcs are defined by three points as shown in Fig. 7-11. The first point you click defines the center of the arc,

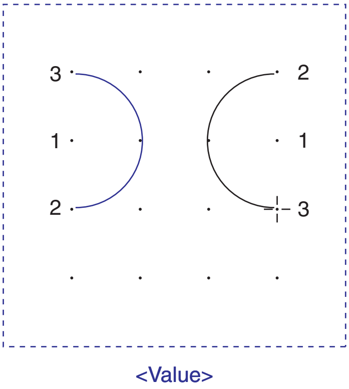
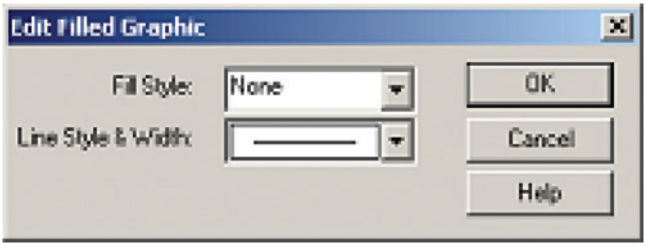


Figure 7-11 Making coils with the Place Arc tool.

the second point defines where the arc starts, and the third point defines the end. The arc is drawn counterclockwise from point 2 to point 3, so the location of point 2 depends on the direction you want the arc to face. After you have placed the first couple of arcs, you can copy and paste the rest in place. **To copy graphic objects**, toggle the Select tool, , and select the objects you want to copy. Left click once to select a single object, or use Ctrl + left click to select multiple objects. Copy and Paste the objects as shown in Fig. 7-13 using typical Windows copy/paste techniques. You can also left click once to select an object, then hold down the Ctrl key, left click and hold the part and "drag a duplicate part" out of the first, release the mouse button to place the copy, and then release the Ctrl key.

Next, place two parallel lines between the arcs to represent the core. Use the Place Line tool, ╲, to draw them. Then make the dots for the dot–coil indicator by using the Place Ellipse tool, ○. Draw a small circle near one of the coils, then hit the Esc key to exit drawing mode. Change the circle to a filled dot by using the Edit Filled Graphic dialog box shown in Fig. 7-12. To display the dialog box, use the Select tool to select the circle and then right click and select Edit Properties from the pop-up. You can leave the Line Style as is but change the Fill Style to Solid. Click OK.



Fill Style: None

Line Style & Width:

Figure 7-12 Use the **Edit Filled Graphic** dialog box to fill objects with patterns.

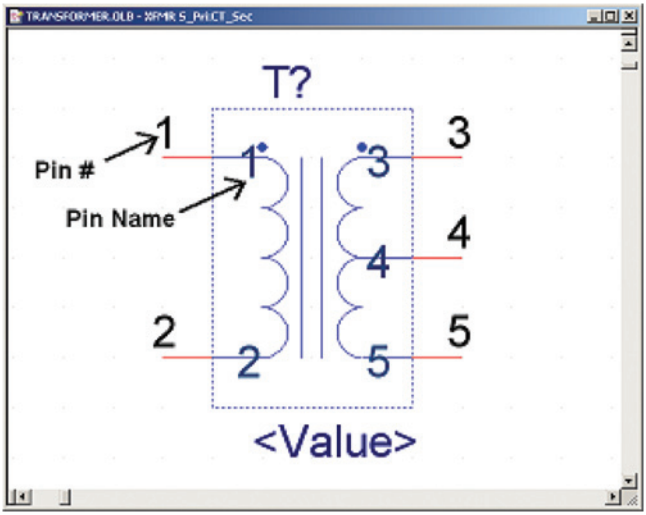
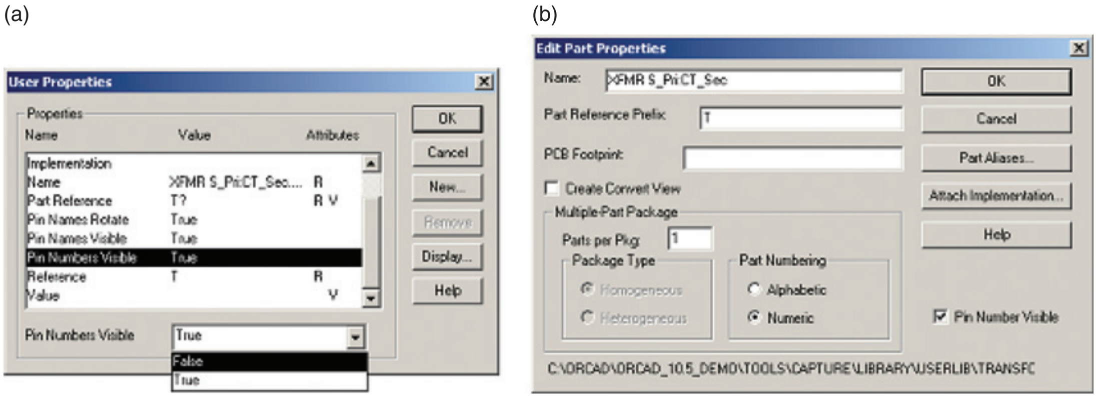


Figure 7-13 Completed part with pin names and numbers visible.

Figure 7-13 shows the transformer design so far. Note that the pin numbers are on the pin outside the boundary and pin names are inside the boundary with the graphics.

You can **use the User Properties dialog box to change the visibility of the pin names and numbers**, shown in Fig. 7-14(a). To display the User Properties dialog box, select Part Properties from the Options menu. Use the User Properties dialog box to make the pin names and numbers invisible. You can also change the visibility of the pin numbers using



(a)

User Properties

Properties

Name	Value	Attributes
Implementation		
Name	XFMR S_Pri:CT_Sec....	R
Part Reference	T?	R V
Pin Names Rotate	True	
Pin Names Visible	True	
Pin Numbers Visible	True	
Reference	T	R
Value		V

Pin Numbers Visible: True

(b)

Edit Part Properties

Name: XFMR S_Pri:CT_Sec

Part Reference Prefix: T

PCB Footprint:

☐ Create Convert View

Multiple-Part Package

Parts per Pkg: 1

Package Type: ● Homogeneous ○ Heterogeneous

Part Numbering: ○ Alphabetic ● Numeric

☑ Pin Number Visible

C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\CAPTURE\LIBRARY\USERLIB\TRANSFC

Figure 7-14 ***User Properties*** *dialog box from* ***Options*** *→* ***Part Properties*** *menu. (a)* ***User Properties*** *dialog box (****Part Properties****). (b) Edit Properties dialog box (****Package Properties****).*

the check box in the Edit Part Properties dialog box shown in Fig. 7-14(b). **To display the Edit Part Properties dialog box**, select Package Properties from the Options menu. The completed part is shown in Fig. 7-15.

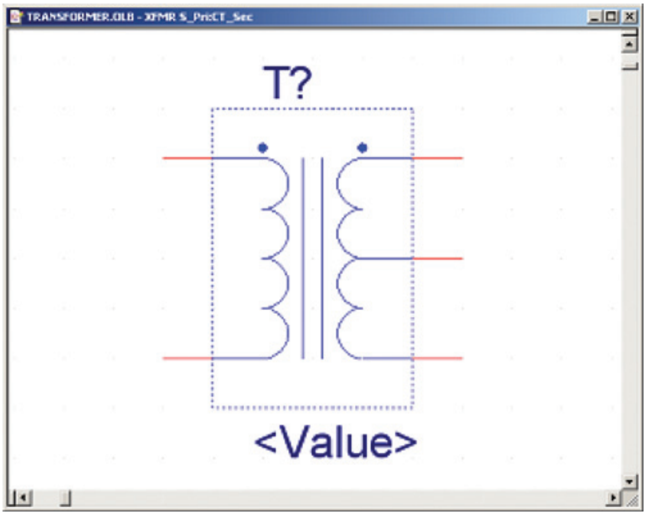


Figure 7-15 Completed homogeneous part (pin names and numbers not visible).

The final task is to save the new part (and the library if it is new). **To save the part**, close the part editing window and click Yes at the Save changes to part *name*? prompt. **To save the library**, select the Library icon in the Project Manager, right click, and select Save As. . . from the pop-up. Save the library with a new name in your UserLibrary in the Capture/ Library path.

Design example for an active, multipart, homogeneous component

The second example shows how to construct the dual op-amp component shown in Fig. 7-16. The parts are identical (homogeneous) and share the power pins.

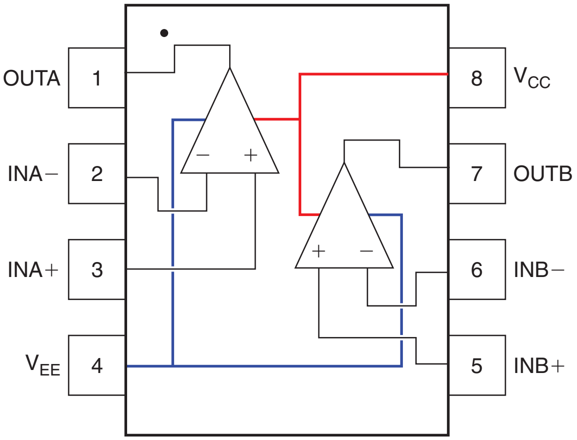
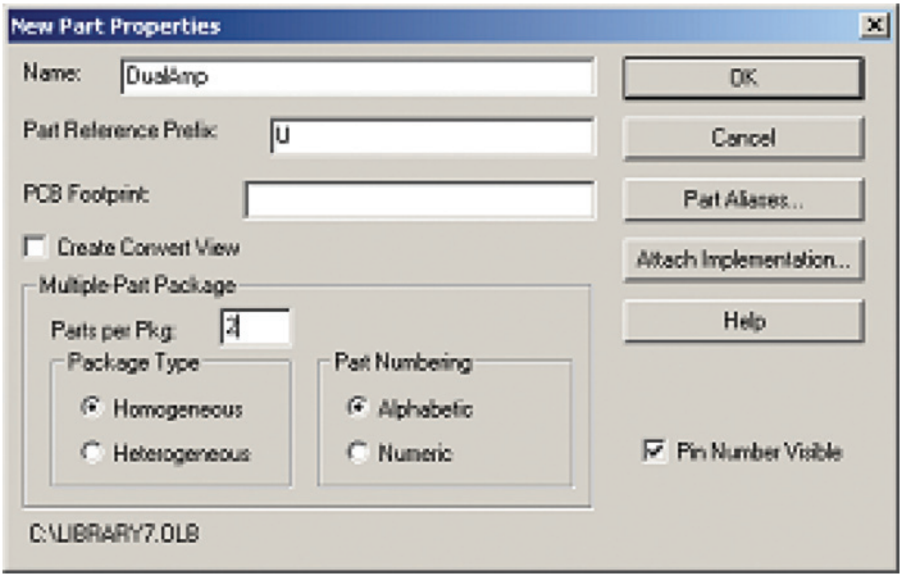

OUTA
1
INA−
2
INA+
3
V_{EE}
4
8
V_{CC}
7
OUTB
6
INB−
5
INB+
−
+
+
−

Figure 7-16 Data-sheet diagram for a dual op-amp component.

Begin as you did with the transformer by selecting New Library from the File menu in the Capture session frame. Select the Library icon in the Library Manager, right click, and select New Part from the pop-up. In the New Part Properties dialog box (Fig. 7-17) enter a


New Part Properties
OK
Cancel
Part Aliases...
Attach Implementation...
Help

Name: DualAmp

Part Reference Prefix: U

PCB Footprint:

☐ Create Convert View

Multiple Part Package

Parts per Pkg: 2

Package Type

● Homogeneous

○ Heterogeneous

Part Numbering

● Alphabetic

○ Numeric

☑ Pin Number Visible

C:\LIBRARY7.OLB

*Figure 7-17 New **Part Properties** dialog box for a dual op-amp.*

name for the op-amp, make "U" the part reference prefix, and change the parts per package to 2. Leave the package type as homogeneous, assign alphabetic part numbering, and make the pin numbers visible. Click OK when you are finished.

In the part editing window, make the part border 0.4 × 0.4 in. Then make the triangular body of the op-amp using the Place Line tool (see Fig. 7-18).

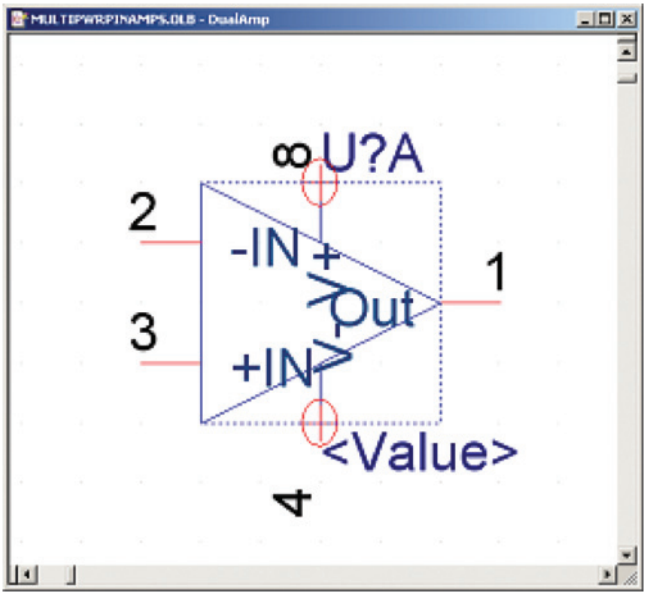
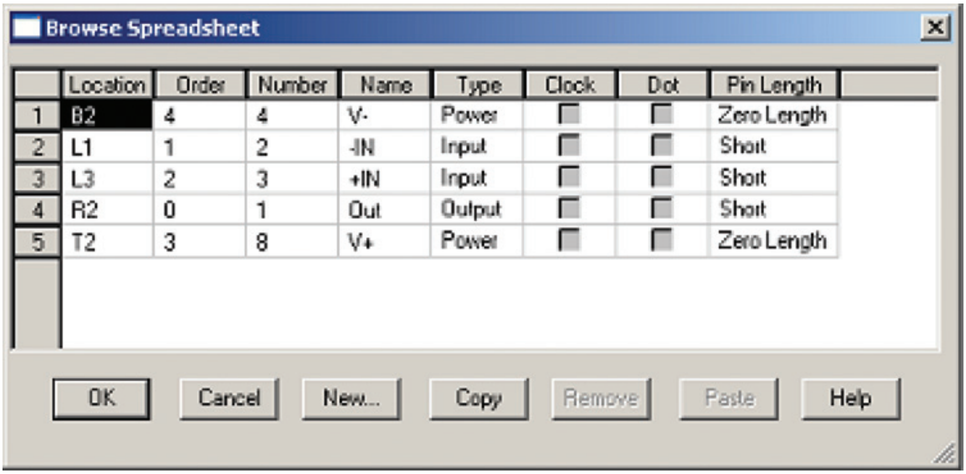


Figure 7-18 Dual op-amp, part A.

Use the Place Pin tool to begin placing pins as shown in Fig. 7-18. Label and place pins for part A per the data sheet (Fig. 7-16). You can either correctly name and number each pin as you place it or place all the pins and then go back and fix the names and numbers after they have all been placed. Whichever method you use, set the pin characteristics as shown in Fig. 7-19. Remember that to change a name or number of a pin, double click on a pin to bring up the Pin Properties dialog box, and to change the properties of multiple pins simultaneously hold down the Ctrl key and left click each pin to select more than one pin. Then right click and select Edit Properties... from the pop-up menu. Finally, add short graphic lines between the op-amp body and the power pins using the Place Line tool, . You will need to turn off the Snap to Grid to do this. Remember to turn the snap to grid back on when you are finished with the graphics.

As you can see from Fig. 7-18, the op-amp looks cluttered because the pin names run into each other and are not optimally spaced with respect to each of the pins. You can fix this by making the pin names *not* visible and adding your own text. First, **turn the pin names off** by setting the Pin Names Visible to False in the User Properties dialog box (from the Options → Part Properties menu). Use the Place Text tool or the Place Line tool to add


Browse Spreadsheet
OK
Cancel
New...
Copy
Remove
Paste
Help

	Location	Order	Number	Name	Type	Clock	Dot	Pin Length
1	B2	4	4	V-	Power	☐	☐	Zero Length
2	L1	1	2	-IN	Input	☐	☐	Short
3	L3	2	3	+IN	Input	☐	☐	Short
4	R2	0	1	Out	Output	☐	☐	Short
5	T2	3	8	V+	Power	☐	☐	Zero Length

Figure 7-19 Pin characteristics for part A of the dual op-amp.

"−" and "+" signs in place of the −IN and +IN pin names. Add text near the power pins to indicate which is the positive supply pin and which is the negative supply pin.

For the time being, that completes part A. There are a couple of ways to get to part B. **To view a specific part of a multipart device** go to the View menu and select Package to see both parts as shown in Fig. 7-20. Then double click on part U?B. Alternatively you can select Next

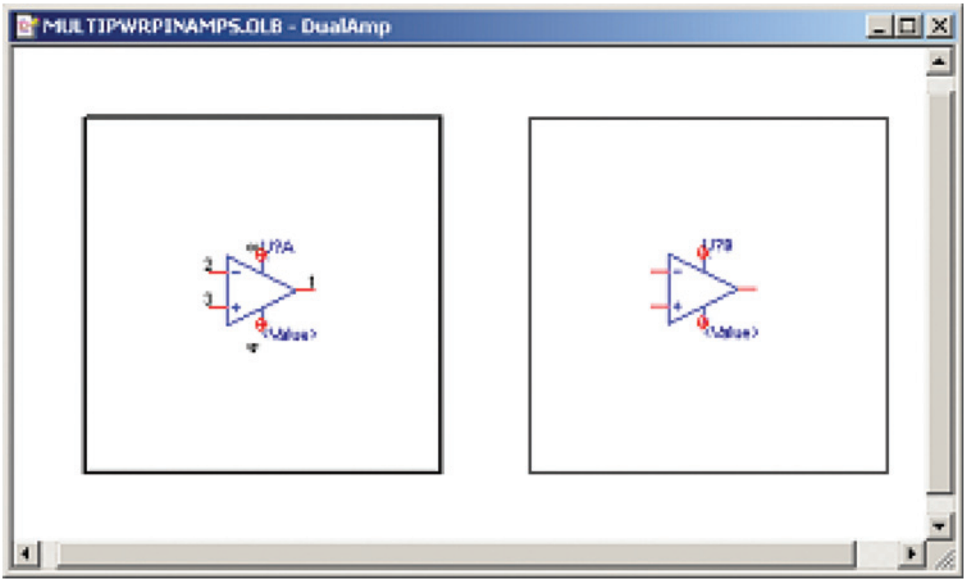
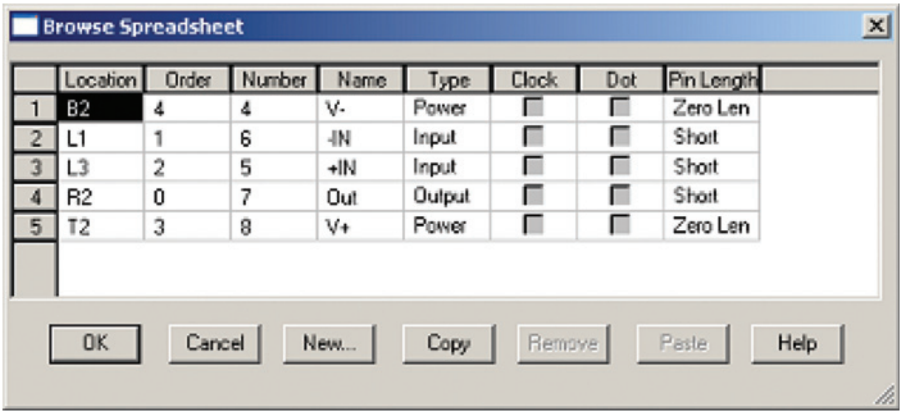

MULTIPWRPINAMPS.OLB - DualAmp
U?A
2
3
1
−
+
<Value>
U?B
−
+
<Value>

Figure 7-20 Package view of dual op-amp part.

(or Previous) Part from the View menu, or use Ctrl + N or B on your keyboard to toggle through the parts.

Once you have part B in the editing window, select all of the pins and set the parameters as shown in Fig. 7-21 using the procedure described above.



	Location	Order	Number	Name	Type	Clock	Dot	Pin Length
1	B2	4	4	V-	Power	☐	☐	Zero Len
2	L1	1	6	-IN	Input	☐	☐	Short
3	L3	2	5	+IN	Input	☐	☐	Short
4	R2	0	7	Out	Output	☐	☐	Short
5	T2	3	8	V+	Power	☐	☐	Zero Len

Figure 7-21 Pin characteristics for part B of the dual op-amp.

Assigning power pin visibility

If you compare Fig. 7-19 to Fig. 7-21, you see that parts A and B share pins 4 and 8. Shared power pins require special handling to make the parts look and function properly between Capture, PSpice, and Layout. The type and visibility of **shared pins** can be power and visible, power and nonvisible, or nonpower and visible. *Digital parts usually share nonvisible power pins*, while *active analog parts typically share either visible power pins or nonpower-type pins* (such as input or passive pins), which are always visible. The type and visibility are initially established at the part level in the library, but you can change these parameters at the schematic level after you have placed the part into your design.

There are several methods for changing the part properties on the schematic and each method has slightly different effects. If you add up all the combinations of the possible pin settings with the various methods of setting them, you will find that there are over 200 possible combinations! Some of the combinations can cause severe errors that will prevent you from creating netlists, others cause various types of warnings, and still others cause no errors or warnings but fail to route correctly on the board. We will not discuss all 200+ combinations here, but we will look at various scenarios in Chap. 9. For now, to keep things simple and to follow typical convention we will make the shared power pins visible power pins since this is an analog part.

To set a power pin's properties, select pin 8 and then right click and select Properties from the pop-up (or just double click the pin) to bring up the Pin Properties dialog box (see Fig. 7-9 as an example). Make sure that the Pin Visible box is checked, an option that is available only for power pins (since all other types of pins are always visible). If you use the

User Properties dialog box (Options → Part properties) you can set only the visibility of the pin's names or numbers, not the visibility of the pin itself. The completed op-amps are shown in Fig. 7-22. Save the parts as described above.

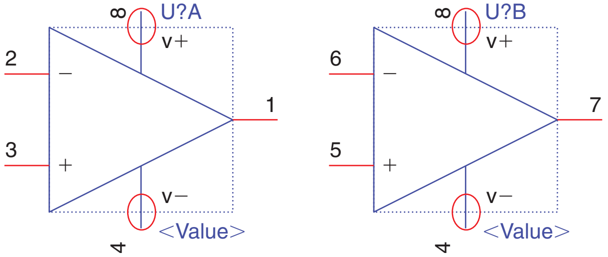


Figure 7-22 The finished op-amps.

When you use a part with shared pins in a schematic and then create a Layout netlist you may get the warning, WARNING [MNL0016] Duplicate pin number '4' on 'LM324'. If the part was constructed properly you can ignore the warning.

Design example for a passive, heterogeneous part

In this design example we will make a passive, heterogeneous part, namely a double-pole, double-through relay as shown in Fig. 7-23. The relay consists of three parts: two sets of identical double-throw contacts and an operating coil with its clamping diode.

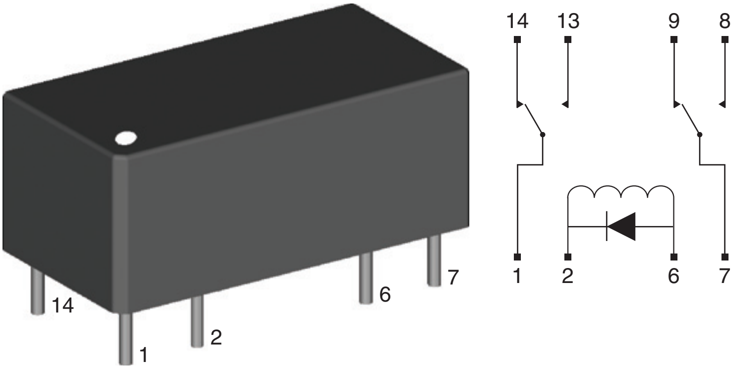
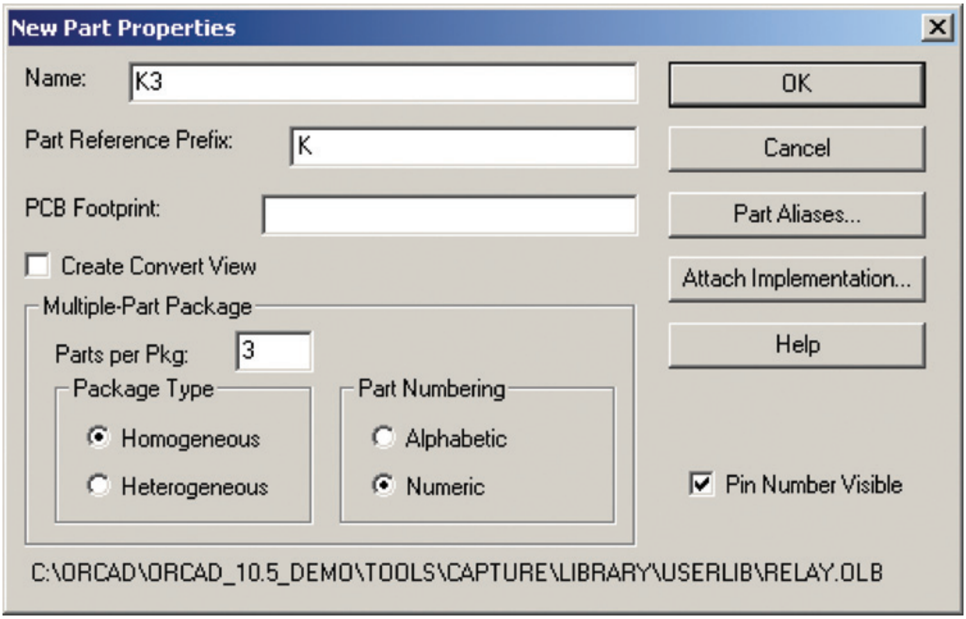


Figure 7-23 A heterogeneous, multipart relay. (a) Relay package. (b) Relay schematic.

Begin by navigating to File → New → Library from the Capture session frame as described in the examples above. Select the Library icon and select New Part from either the Design menu or the pop-up after right clicking on the icon. Fill out the New Part Properties dialog box as shown in Fig. 7-24. Make sure you select 3 parts per package and select the heterogeneous



Name: K3

Part Reference Prefix: K

PCB Footprint:

☐ Create Convert View

Multiple-Part Package

Parts per Pkg: 3

Package Type

● Homogeneous

○ Heterogeneous

Part Numbering

○ Alphabetic

● Numeric

☑ Pin Number Visible

C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\CAPTURE\LIBRARY\USERLIB\RELAY.OLB

*Figure 7-24 **New Part Properties** dialog box for the heterogeneous relay.*

package type. Click OK. From the View menu go to the Package view to make sure that you have three parts.

Begin by constructing the relay coil and clamping diode as part K?-1. Bring up K?-1 in an editing window; double click on the K?-1 window if you are in the package view or use Ctrl + N on your keyboard to toggle through the parts if you are in the part view. Resize the border so that it is 0.3 in. wide by 0.6 in. tall. Using Fig. 7-25 as a guide, use the Place Pin tool to place two pins on the left side of the part border. Define the top pin as number 2 with name C+ and the bottom pin as number 6 with name C−. Make both pins short, passive lines, and make the names nonvisible. Use the Place Line and Place Arc tools to add the coil, diode, and "+" graphics to the part as described in the previous examples.

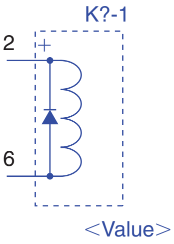
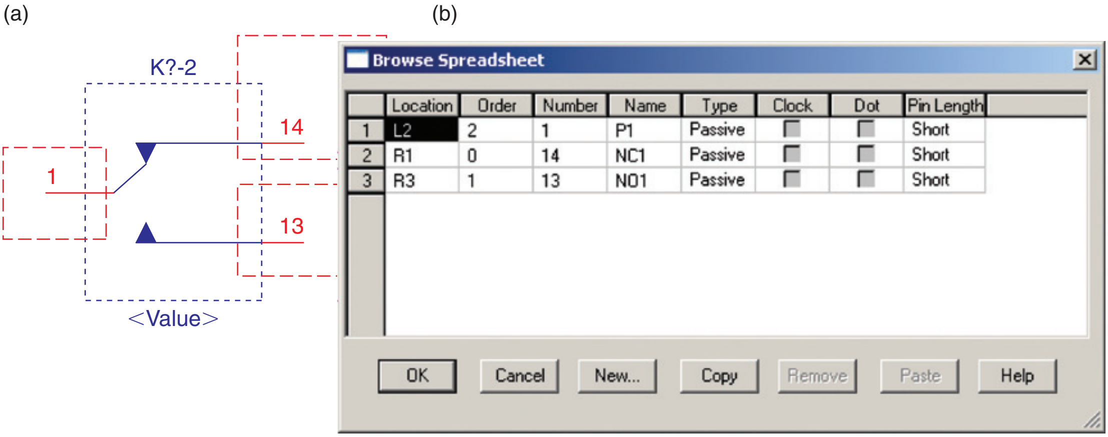


Figure 7-25 Relay coil and diode.

The next step is to add the first set of contacts. Toggle to part K?-2. Resize the border to 0.4 in. wide by 0.6 in. tall. Using Fig. 7-26(a) as a guide, add two pins to the right side of the border and one on the left. Set the pin parameters as shown in Fig. 7-26(b), make the pin names nonvisible. Use the Place Line tool to add the pole and the lines leading from the pin to the throws (the contacts).


(a)

(b)

	Location	Order	Number	Name	Type	Clock	Dot	Pin Length
1	L2	2	1	P1	Passive	☐	☐	Short
2	R1	0	14	NC1	Passive	☐	☐	Short
3	R3	1	13	NO1	Passive	☐	☐	Short

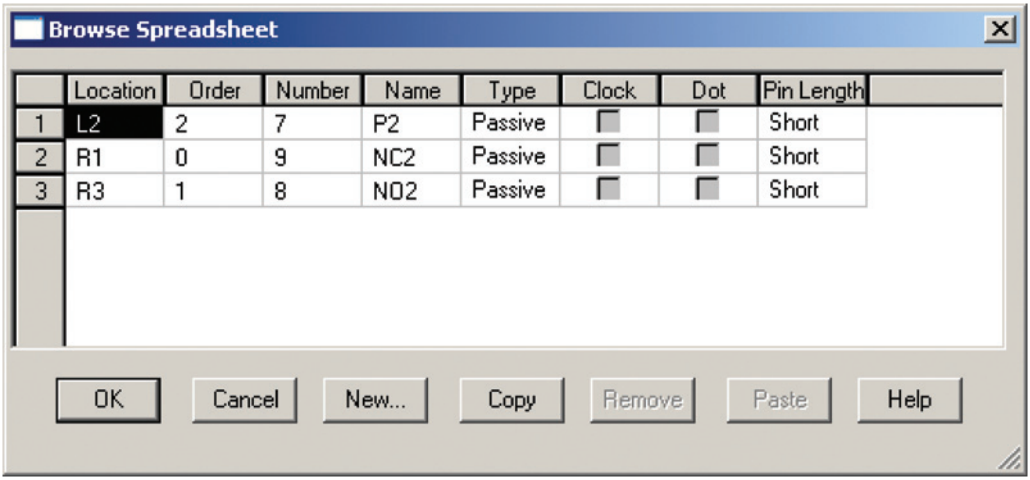
Figure 7-26 (a) Schematic and (b) pin settings for the first set of relay contacts.

Use the Place Polyline tool to draw the throws so that you can make them solid filled. Use the Shift key to make diagonal polylines. After you have the triangle drawn, double click on it to bring up the Edit Filled Graphic dialog box and set the fill to solid.

Once you have the pole and throws for contact assembly K?-2 finished, copy and paste the graphics into the K?-3 part. To copy all of the pieces at one time, hold down the Ctrl key on your keyboard and select each line and polyline one at a time. Once you have them all selected, right click and select Copy from the pop-up (or select Copy from the Edit menu, or use Ctrl + C on your keyboard). Go to the next part, K?-3, by typing Ctrl + N on your keyboard and then paste the copied graphics into the empty part outline (right click and select Paste from the pop-up, or select Paste from the Edit menu, or use Ctrl + V on your keyboard). Add three pins using the Place Pin tool as you did for the previous parts. Set the pin parameters as shown in Fig. 7-27. You will notice that the order starts at “0” for each part. The order of the pins is of concern only when the part is to be used with a PSpice model for performing simulations. We will address that issue in the next sections.

The completed, multipart relay is shown in Fig. 7-28.

When you place the relay in a Capture schematic, use the Part: dropdown list as shown in Fig. 7-29 to place the desired part of the multipart package.



	Location	Order	Number	Name	Type	Clock	Dot	Pin Length
1	L2	2	7	P2	Passive	☐	☐	Short
2	R1	0	9	NC2	Passive	☐	☐	Short
3	R3	1	8	NO2	Passive	☐	☐	Short

Figure 7-27 Pin parameters for the second set of contacts.

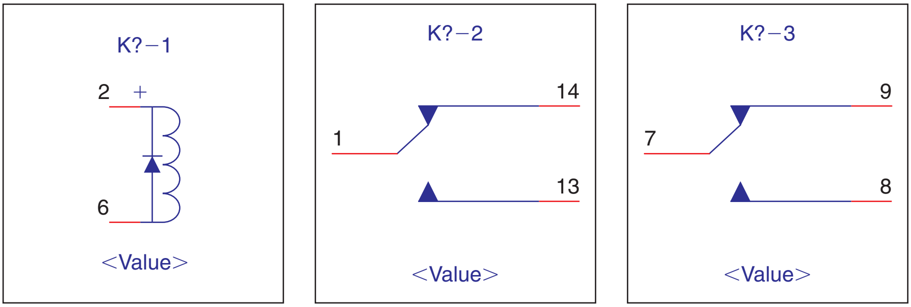
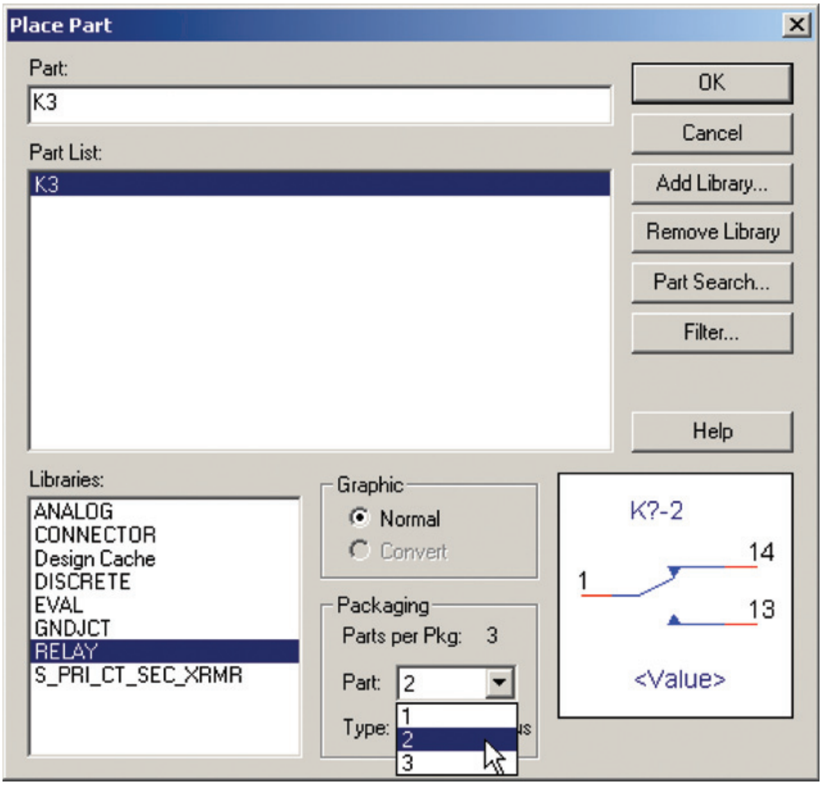


Figure 7-28 Package view of the completed heterogeneous relay.

Method 2: Constructing Parts with Capture Using the Design Spreadsheet

Use this method to automatically generate a single or multipart package. It is similar to the first method except that you define all of the pins up front using the spreadsheet shown in Fig. 7-30. New Part from Spreadsheet generates heterogeneous packages by default, but you can use it to make homogeneous parts. The parts will be defined as heterogeneous but will be homogeneous in effect if there are no differences between the parts.

To construct a part using the design spreadsheet, open an existing Capture library that you want to add a part to, or start a new library as described above. In the Library Manager, select the Library icon and select the New Part from Spreadsheet. . . option, which you can do either from the Design menu or from the pop-up menu by right clicking on the Library icon.



Place Part

Part: K3

Part List:
K3

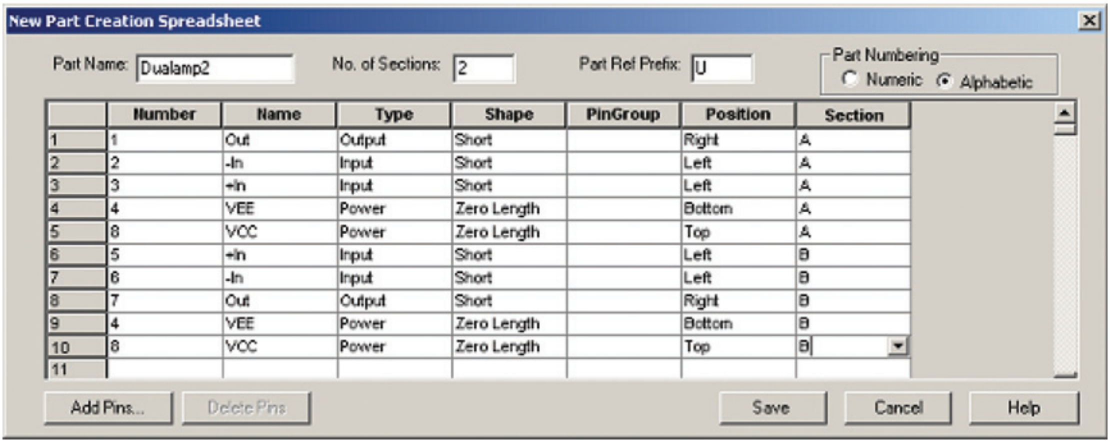
Libraries:
ANALOG
CONNECTOR
Design Cache
DISCRETE
EVAL
GNDJCT
RELAY
S_PRI_CT_SEC_XRMR

Graphic
● Normal
○ Convert

Packaging
Parts per Pkg: 3
Part: 2
Type:

OK
Cancel
Add Library...
Remove Library
Part Search...
Filter...
Help
1
2
3
K?-2
14
1
13
<Value>

Figure 7-29 Selecting a part from a multipart package in a Capture schematic.



New Part Creation Spreadsheet

Part Name: Dualamp2
No. of Sections: 2
Part Ref Prefix: U
Part Numbering ○ Numeric ● Alphabetic

	Number	Name	Type	Shape	PinGroup	Position	Section
1	1	Out	Output	Short		Right	A
2	2	-In	Input	Short		Left	A
3	3	+In	Input	Short		Left	A
4	4	VEE	Power	Zero Length		Bottom	A
5	8	VCC	Power	Zero Length		Top	A
6	5	+In	Input	Short		Left	B
7	6	-In	Input	Short		Left	B
8	7	Out	Output	Short		Right	B
9	4	VEE	Power	Zero Length		Bottom	B
10	8	VCC	Power	Zero Length		Top	B
11							

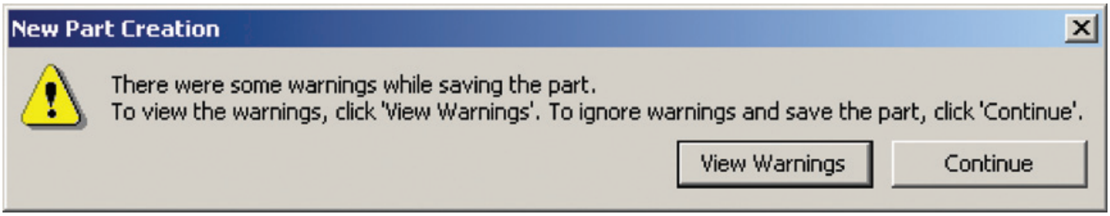
Add Pins...
Delete Pins
Save
Cancel
Help

Figure 7-30 The *New Part Creation Spreadsheet*.

The spreadsheet will initially be blank. Add the pin numbers and parameter settings as needed per the part requirements. The pin settings shown in Fig. 7-30 would generate a part identical to the dual op-amp that was designed in the example above (see Fig. 7-16).

Notice that pins 4 and 8 were added twice, once for each part, to define the shared power pins.

After the pin parameters have been entered into the spreadsheet, click the **Save** button. The information box shown in Fig. 7-31 will be displayed, letting you know that there were warnings (because of the duplicate pins). You can view the warnings or click **Continue** to view the parts.


New Part Creation

There were some warnings while saving the part.
To view the warnings, click 'View Warnings'. To ignore warnings and save the part, click 'Continue'.

Figure 7-31 ***New Part Creation*** *warnings.*

Figure 7-32 shows the package view of the parts generated by the spreadsheet. By default, the "parts" are initially represented by simple boxes. All you have left to do at this point is to modify the graphics to make the op-amps cosmetically correct. In the homogeneous op-amp from the example above, all parts were automatically made identical when you made a graphic in one part. Since this is a heterogeneous part by default (that you cannot change), you will have to modify the graphics on every part individually. Delete the boxes that lie on top of the dotted outline and add the graphics as described in the previous op-amp example.

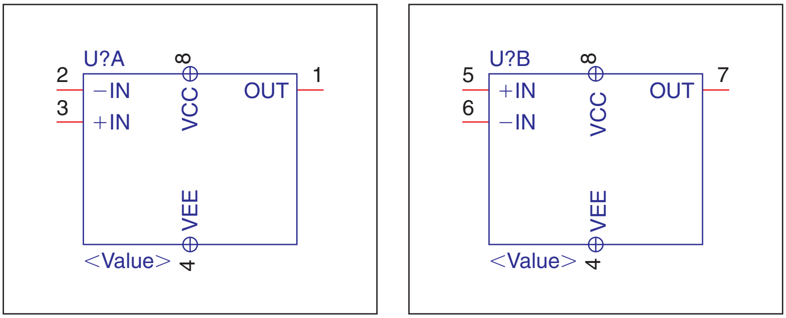
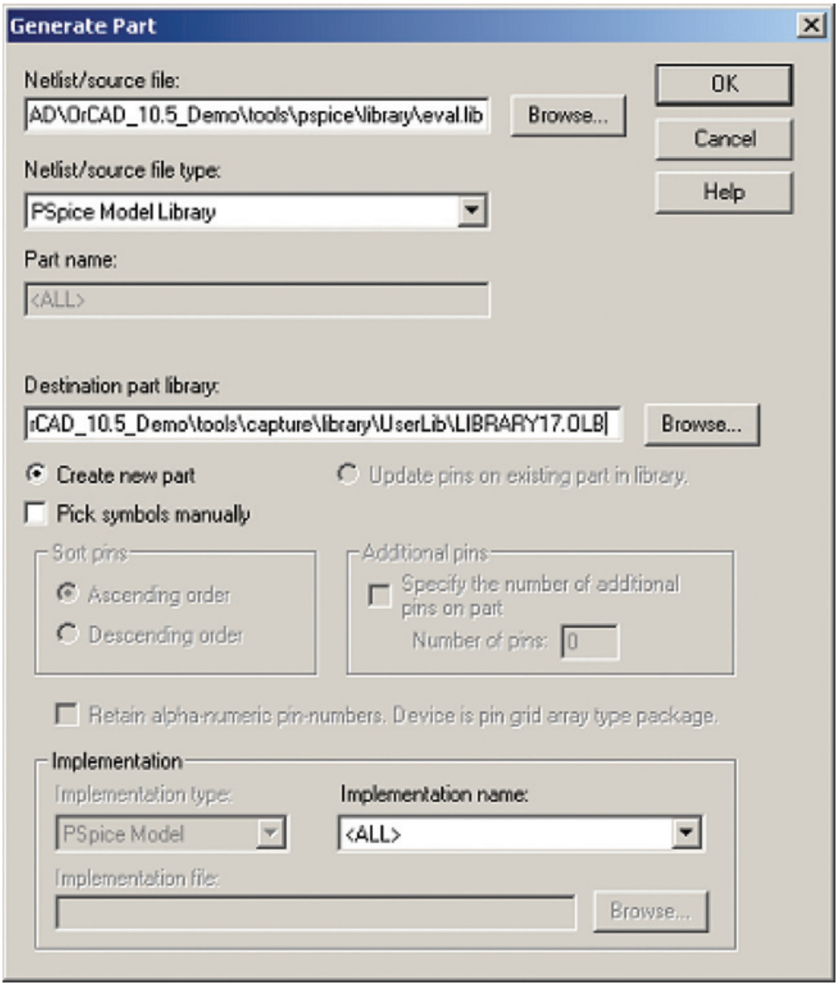


Figure 7-32 Package view of new parts generated using the spreadsheet.

Method 3: Constructing Parts Using **Generate Part** from the **Tools Menu**

Use this method to create a new Capture part (or parts) from a PSpice model library or a Capture project. The part(s) can then be used for schematic entry, PSpice simulations, and PCB layout (if you assign a footprint to it). To use this method, a PSpice model library or a functional schematic design needs to preexist. In the section below several methods for developing or obtaining the PSpice libraries and functional schematic designs are described. For the time being we will go ahead under the assumption that a PSpice library is available so that the part creation process is kept separate from the library/schematic creation process.



Netlist/source file: AD\OrCAD_10.5_Demo\tools\pspice\library\eval.lib

Netlist/source file type: PSpice Model Library

Part name: <ALL>

Destination part library: rCAD_10.5_Demo\tools\capture\library\UserLib\LIBRARY17.OLB

● Create new part ○ Update pins on existing part in library.

☐ Pick symbols manually

Sort pins
● Ascending order
○ Descending order

Additional pins
☐ Specify the number of additional pins on part
Number of pins: 0

☐ Retain alpha-numeric pin-numbers. Device is pin grid array type package.

Implementation
Implementation type: PSpice Model
Implementation name: <ALL>
Implementation file:

Figure 7-33 ***Generate Part*** *dialog box from the Tools menu.*

Begin by starting a new Capture library or open an existing library from the Capture session frame's File menu. Select the Library icon and then select Generate Part. . . from the Tools menu. The Generate Part dialog box will pop up as shown in Fig. 7-33.

Select PSpice Model Library (or Capture Schematic/Design if appropriate) from the Netlist/source file type: list, then select the library (*.lib, etc.) or design (*.dsn, etc.) from the Netlist/source file: list. Make sure that the Destination part library: path and name are what you want and that the library has a .OLB extension. Make sure that the Create new part option is checked and click OK.

After Capture has completed importing the library/design file you selected, you should see the list of parts in the Library Manager. If the Capture library (.olb) you are working with was originally empty, the new parts will be located directly under the Library icon in the Design Resources folder. But if the library already had some parts in it, the new parts and copies of the previously existing parts will be added to both the Library icon and the Library folder under the Design Resources folder (see Fig. 7-34, in which, as an example, the breakout library was added to the analog_p library). The Library folder will also contain a duplicate

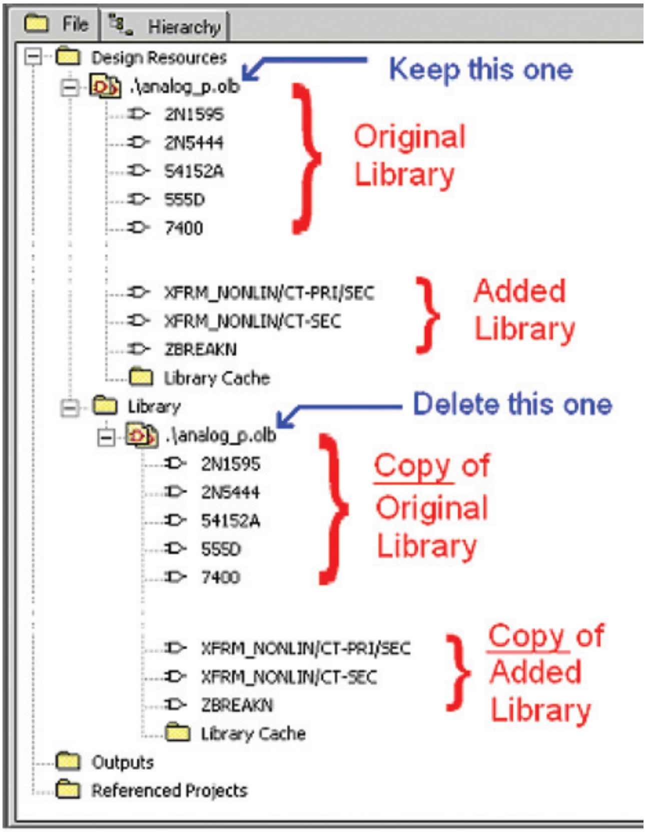

File
Hierarchy
Design Resources
.\analog_p.olb
2N1595
2N5444
54152A
555D
7400
XFRM_NONLIN/CT-PRI/SEC
XFRM_NONLIN/CT-SEC
ZBREAKN
Library Cache
Library
.\analog_p.olb
2N1595
2N5444
54152A
555D
7400
XFRM_NONLIN/CT-PRI/SEC
XFRM_NONLIN/CT-SEC
ZBREAKN
Library Cache
Outputs
Referenced Projects
Keep this one
Original Library
Added Library
Delete this one
Copy of Original Library
Copy of Added Library

Figure 7-34 Structure of Library Manager after copying a library into an existing library.

of the Library icon. This allows you to copy, add, or delete parts to/from the new library. Once you are satisfied with which parts are contained under the Library icon under the Design Resources folder, you can delete the duplicate Library icon and parts in the Library folder, keeping just the library in the Design Resources folder.

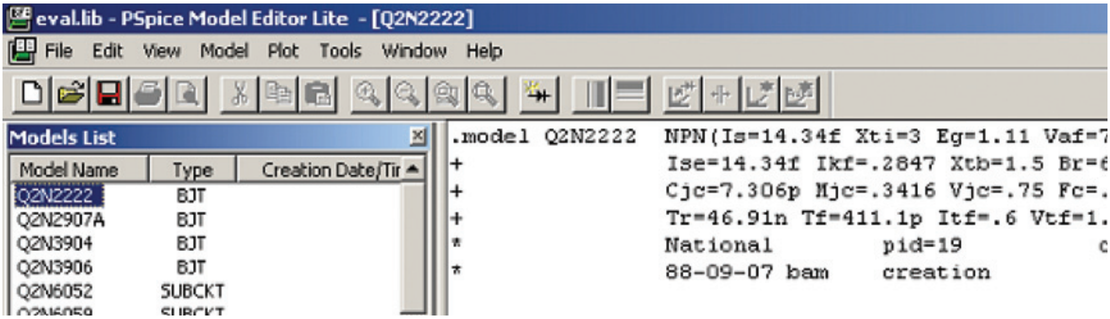
Once you have finished adding parts to the library, you can edit the added part(s), pins, and links to footprints using the Capture Part Editor, and the part and package properties dialog boxes from the Design menu as described in previous examples.

Finally, save and close the library. You can now use the library and its parts in new designs for schematic entry, simulations, and PCB layout.

Method 4: Generating Parts with the PSpice Model Editor

You can use the PSpice Model Editor to make Capture parts that can be used in schematic designs, circuit simulations, and PCB layouts. The difference between using the PSpice Model Editor and the Generate Part method (Method 3) is that you can work directly on and with the PSpice models with the Model Editor.

Start the PSpice Model Editor. Go to Start → All Programs → OrCAD 10.5 → PSpice Accessories → Model Editor. You will begin with a blank Model Editor session window. **To open an existing PSpice library** (*name*.LIB*)*, navigate to OrCAD/tools/pspice/library and select Open from the File menu. Select one of the libraries (e.g., eval.lib) and click Open; then select one of the models from the model list. Figure 7-35 shows the Q2N2222 BJT transistor



Model Name	Type	Creation Date/Tir
Q2N2222	BJT	
Q2N2907A	BJT	
Q2N3904	BJT	
Q2N3906	BJT	
Q2N6052	SUBCKT	

```
.model Q2N2222   NPN(Is=14.34f Xti=3 Eg=1.11 Vaf=7
+                Ise=14.34f Ikf=.2847 Xtb=1.5 Br=6
+                Cjc=7.306p Mjc=.3416 Vjc=.75 Fc=.
+                Tr=46.91n Tf=411.1p Itf=.6 Vtf=1.
*                National         pid=19           c
*                88-09-07 bam     creation
```

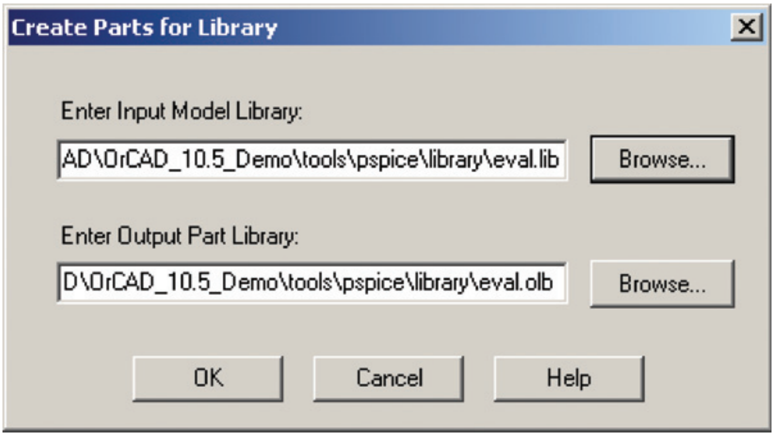
Figure 7-35 A PSpice library as viewed from the Model Editor.

model from the eval library. The Models List window pane shows all of the simulation models contained in the library, and it tells you whether it is a primitive model or a subcircuit model. The text window to the right of the Models List displays the “code” that describes the model.

You can construct new models by using existing model listings as examples and/or the model descriptions found in the PSpice reference guide (pspcref.pdf) found in the OrCAD/doc folder. The following sections describe how to download primitive models (models beginning with .model) from the Internet and how to create your own subcircuit models (models beginning with .subcircuit). The models can then be added to a PSpice library from which you can generate Capture part libraries as described below. Creating custom primitive models is not described here.

Generating a Capture part library from a PSpice model library

Beginning with a PSpice library (.lib) open in the Model Editor (similar to Fig. 7-35), select Create Capture Parts. . . from the Model Editor's File menu. You will be presented with the Create Parts for Library dialog box shown in Fig. 7-36. In the Enter Input Model Library: text box, use the Browse button to find the PSpice library (*.LIB) for which you want to make parts. Use the second Browse button to specify the location for the new Capture library (*.OLB). Remember that the PSpice models and the libraries that contain them are usually stored in the OrCAD/tools/pspice/library path, while the Capture parts that use the models are stored in the. . .OrCAD/tools/capture/libraries/pspice path. Click OK once you have the input and output libraries and paths specified.


Create Parts for Library

Enter Input Model Library:
AD\OrCAD_10.5_Demo\tools\pspice\library\eval.lib

Enter Output Part Library:
D\OrCAD_10.5_Demo\tools\pspice\library\eval.olb

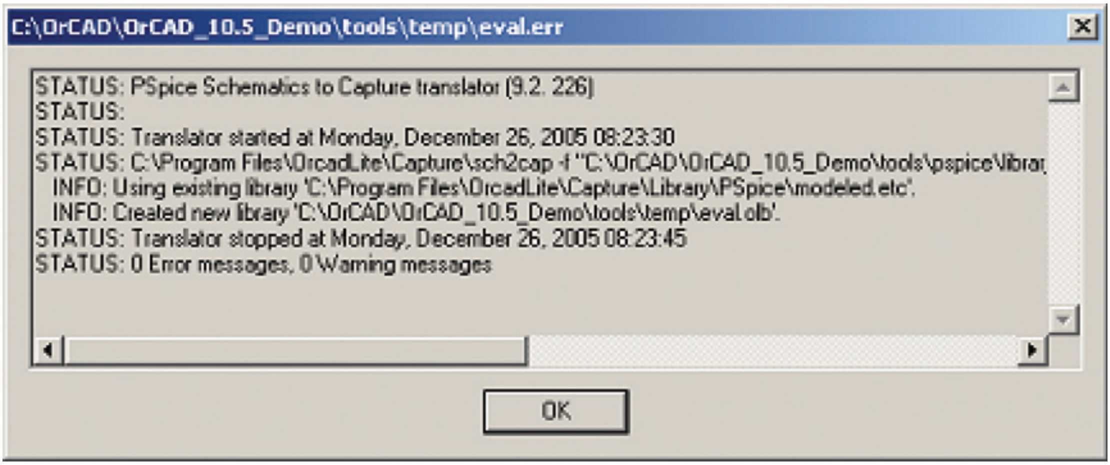
Figure 7-36 The PSpice ***Create Parts for Library*** *dialog box for Capture parts.*

Note

- *A Capture part library (**eval.olb**) already exists in the **Tools/Capture/Library/PSpice** folder for the **eval** PSpice model library (**eval.lib**). The **eval** library is used here for demonstration purposes. If you perform the following procedure on an existing library, save the new library to a temporary or user folder so that you do not overwrite the existing library.*

When the Model Editor has finished, it will display an information box similar to the one in Fig. 7-37. If the Model Editor is successful at generating the Capture part library, the last line will say: 0 Error messages, 0 Warning messages. Click OK to close the information box.

The PSpice Model Editor generates Capture parts with correctly named and numbered pins, but the parts will be generic boxes because the PSpice Model Editor describes only how the



```
STATUS: PSpice Schematics to Capture translator (9.2. 226)
STATUS:
STATUS: Translator started at Monday, December 26, 2005 08:23:30
STATUS: C:\Program Files\OrcadLite\Capture\sch2cap -f "C:\OrCAD\OrCAD_10.5_Demo\tools\pspice\librar
  INFO: Using existing library 'C:\Program Files\OrcadLite\Capture\Library\PSpice\modeled.elc'.
  INFO: Created new library 'C:\OrCAD\OrCAD_10.5_Demo\tools\temp\eval.olb'.
STATUS: Translator stopped at Monday, December 26, 2005 08:23:45
STATUS: 0 Error messages, 0 Warning messages
```

Figure 7-37 New part creation information box.

parts function, not what they look like. You will need to use the Capture Part Editor to modify the graphical appearance of the parts, as described in the earlier examples. To view the new part library start Capture and select Open → Library. . . from the File menu in the Capture session frame.

Making and/or Obtaining PSpice Libraries for Making New Capture Parts

Before you send a final board design to be manufactured, you will at some point in the design process want to simulate your design. A detailed explanation of PSpice model development and simulation process is outside of the scope of this text and many references are available on the subject. But in the interest of completeness, a brief explanation of how to add PSpice models to your Capture parts will be discussed here.

PSpice contains many libraries, but manufacturers continually design new parts, which may not be included with your version of PSpice, so eventually you will want to be able to develop your own Capture parts that have simulation capabilities (and ultimately will be used in a board design).

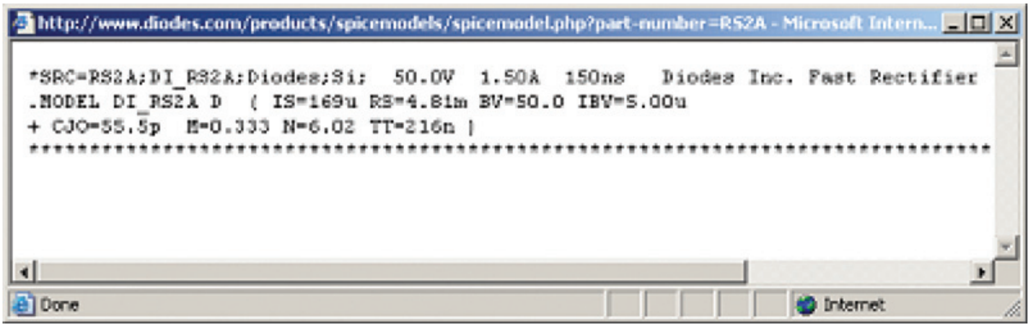
A PSpice library contains primitive models (such as resistors and diodes) and subcircuit models (such as logic gates and op-amps). Primitive models are basically limited to behavioral descriptions of single devices. Subcircuit models can describe the behavior of a single device, multiple devices, or complete circuit designs. Unless specifically noted, a "model" in this text refers to both primitive and subcircuit models in general.

With regard to PSpice model libraries, the models that the libraries contain begin as simple text files that have a .mod extension. A model is added to a library by importing it into the PSpice (.lib) library. Once the model is imported into the library the original .mod file is no longer needed and can be deleted or archived in a separate folder.

Downloading libraries and/or models from the Internet

The easiest way to make a new PSpice model library is to download it from the manufacturer's Web site (when available). You can often download complete libraries, but sometimes OEMs provide only individual models that you can add to your own libraries.

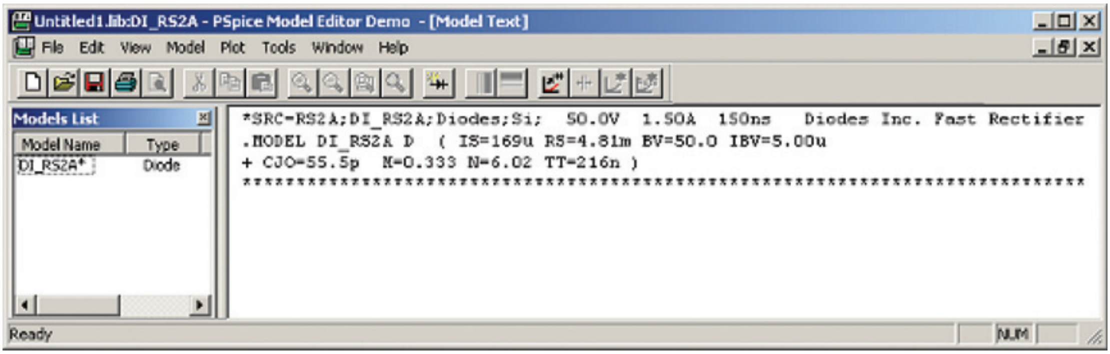
Here is an example. Suppose you were to use an RS2A fast recovery diode (Diodes Incorporated) in your design and need its PSpice model. By going to the Diodes Incorporated Web site (http://www.diodes.com/products/spicemodels/index.php) you can obtain the model for the RS2A diode as shown in Fig. 7-38. Copy the text as is from the Internet Explorer window and paste it into any simple text editor such as Notepad. Save the text file with a .mod file extension (e.g., RS2A.mod) to a convenient folder that is set up for your collection of model files.


http://www.diodes.com/products/spicemodels/spicemodel.php?part-number=RS2A - Microsoft Intern...
Done
Internet

```
*SRC=RS2A;DI_RS2A;Diodes;Si;   50.0V   1.50A   150ns   Diodes Inc. Fast Rectifier
.MODEL DI_RS2A D  ( IS=169u RS=4.81m BV=50.0 IBV=5.00u
+ CJO=55.5p  M=0.333 N=6.02 TT=216n )
********************************************************************************
```

Figure 7-38 Spice diode model downloaded from the Web.

Next start a new PSpice library for Diodes Incorporated parts. From the PSpice Model Editor **File** menu choose **New**. You will be presented with a blank Models List window pane and an unsaved library (**Untitled1.lib**). From the **Model** menu, chose **Import**. From the **Open File** dialog box, navigate to and select the **RS2A.mod** file. Click **Open**. The Models List window should now contain the new model as shown in Fig. 7-39. Save the new library in a user folder


Untitled1.lib:DI_RS2A - PSpice Model Editor Demo - [Model Text]
File
Edit
View
Model
Plot
Tools
Window
Help
Models List
Model Name
Type
DI_RS2A*
Diode
Ready
NUM

```
*SRC=RS2A;DI_RS2A;Diodes;Si;   50.0V   1.50A   150ns   Diodes Inc. Fast Rectifier
.MODEL DI_RS2A D  ( IS=169u RS=4.81m BV=50.0 IBV=5.00u
+ CJO=55.5p  M=0.333 N=6.02 TT=216n )
********************************************************************************
```

Figure 7-39 New RS2A PSpice model in the Model Editor.

with a name such as DiodesInc.lib (select Save As... from the File menu). You now have a PSpice library (with only one part in this case) for which you can make a new Capture part. To make a Capture part for the new library use the Create Capture Parts command from within the PSpice Model Editor as described under Method 4 above, or you can use the Generate Part command from within Capture as described under Method 3 described earlier.

Making a PSpice model from a Capture project

In the event that a PSpice model (or even a generic spice model) cannot be located, you can make your own *.mod file. There are two ways to do this depending on the type of model you are trying to make. If you need to make a primitive model for a device (e.g., a diode or P-channel MOSFET transistor) you will need to compose a .mod file using a text editor and then import the model into a library as described above. To make an accurate model you need to be familiar with model parameters for the part and the "code" that PSpice understands. This will not be described here, but you can read about the details in the PSpice Reference document (pspcref.pdf) located in the OrCAD/doc folder. As a starting point you can also look at examples from the PSpice Breakout library (breakout.lib).

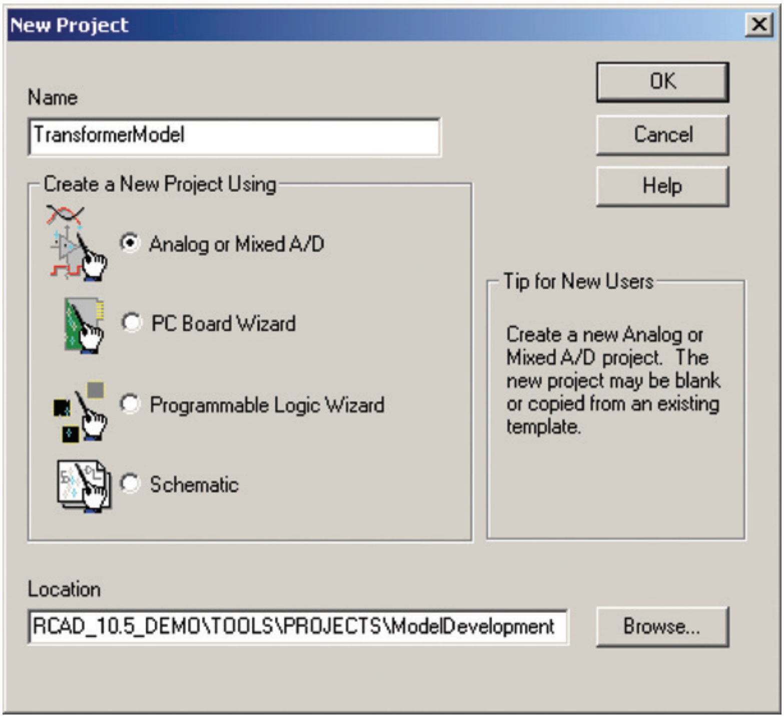
If you need to make a model for a nonprimitive part (an IC or a transformer, for example) you can compose a subcircuit model without having extensive knowledge of model parameters or PSpice code. You simply "draw" the circuit using Capture, have Capture write the subcircuit model for you, and then save it as a PSpice library. Once you have the .LIB file you can use Method 3 or 4 above to make a Capture part with the model attached to it and attach a Layout footprint if so desired.

An example of how to make a PSpice model and subsequent Capture part is given here for a transformer with a single primary winding and a center-tap secondary, similar to the one in Fig. 7-3 (except that the transformer in this example will have a PSpice model—a PSpice template—associated with it). Using this procedure you can specify the inductance and DC resistance of the windings and the coupling between the windings for a specific part as described in a data sheet.

The basic process is as follows:

1. Use Capture to draw a circuit that you can simulate. The circuit will consist of inductors, resistors, and coupling coefficients.
2. After the transformer "circuit" is simulated to verify it behaves correctly, simulation sources are deleted and hierarchical ports are added to the schematic, which will become the leads (pins) of the transformer.
3. Use Capture to create a PSpice library netlist file (.lib) for the circuit. Method 3 or Method 4 is used to generate a Capture part from the .lib file. In this example we will use Method 4 so that we can look at and modify the model prior to making a Capture part for it.

To make a .subcircuit model open Capture and choose New → Project... from the session frame's File menu. From the New Project dialog box choose Analog or Mixed A/D as shown in Fig. 7-40.



New Project

Name
TransformerModel

Create a New Project Using
● Analog or Mixed A/D
○ PC Board Wizard
○ Programmable Logic Wizard
○ Schematic

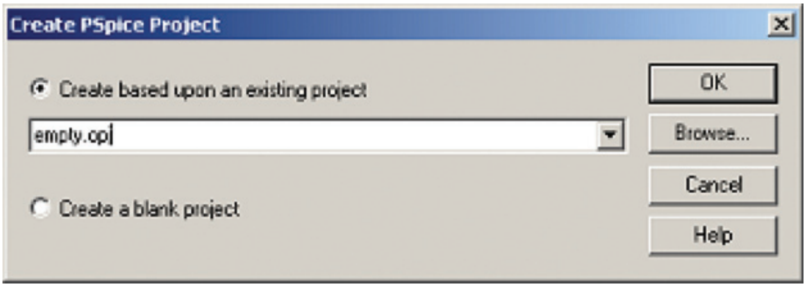
Tip for New Users
Create a new Analog or Mixed A/D project. The new project may be blank or copied from an existing template.

Location
RCAD_10.5_DEMO\TOOLS\PROJECTS\ModelDevelopment

Figure 7-40 ***New Project*** *dialog box for a PSpice project.*

Select the location of the new project using the **Browse** button at the bottom of the dialog box. If you plan on making more models in the future it is a good idea to create a new folder just for model development. Once you have your models fully developed and tested you can copy the finished libraries into the normal Capture and PSpice library folders.

After you click **OK** the **Create PSpice Project** dialog box (Fig. 7-41) will be displayed. Check the **Create based upon an existing project** radio button and select either the **empty.opj** or the **simple.opj** project template. Different templates may be displayed



● Create based upon an existing project
empty.opj
○ Create a blank project

Figure 7-41 The ***Create PSpice Project*** *dialog box.*

depending on which version you have. For what we are going to do in this example it really does not matter which template you start with. Click OK.

In the Project Manager window expand the Design (.dsn) icon if it is not already expanded, and double click the SCHEMATIC1 folder (see Fig. 7-42). The name of the design (*DesignName*.dsn) will become the default name of the PSpice Library (*DesignName*.lib), and

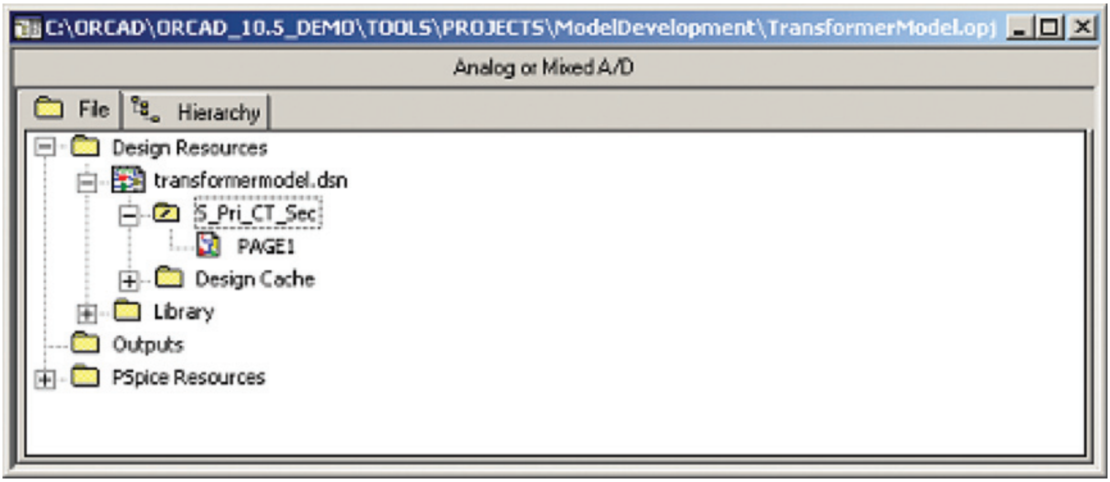

C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\ModelDevelopment\TransformerModel.opj
Analog or Mixed A/D
File
Hierarchy
Design Resources
transformermodel.dsn
S_Pri_CT_Sec
PAGE1
Design Cache
Library
Outputs
PSpice Resources

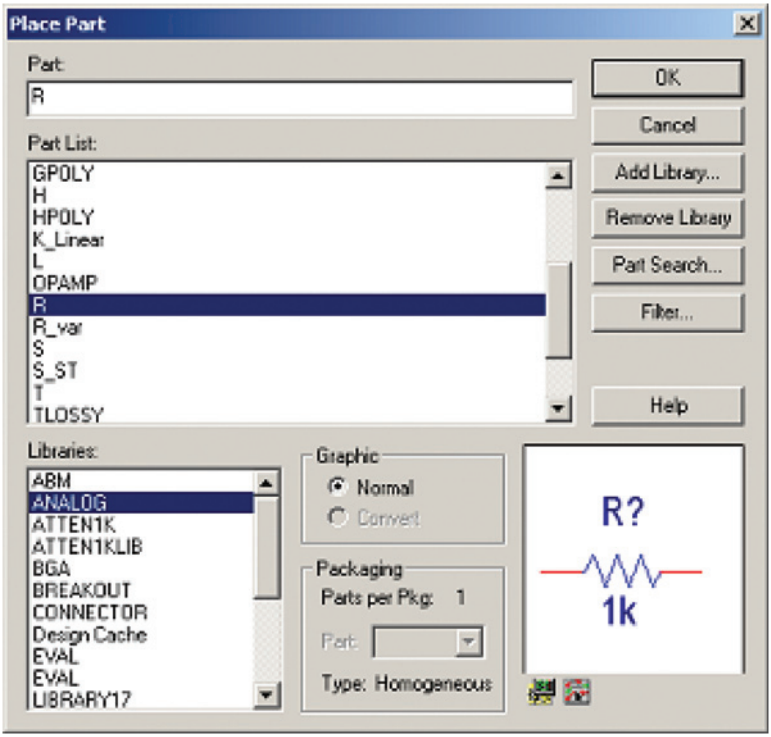
Figure 7-42 Project Manager view of design.

the name of the root folder (*FolderName*) will become the name of the PSpice part model (.subcircuit *FolderName*...) so you will want to change the name of the folder from SCHEMATIC1 to the name you wish for your part.

To rename the schematic folder, select the folder by left clicking once, then right click, and select Rename from the pop-up. Change the name of the schematic folder to the name that you want the part to have (e.g., S_Pri_CT_Sec for single-winding primary, center-tap secondary).

Double click on the PAGE1 icon to display the schematic page (see Fig. 7-42). Delete any parts or text provided by the template by dragging a box around (or across) the parts to highlight them and then hit the Delete key on your keyboard.

Place four resistors from the Analog library (which have PSpice models associated with them) on the schematic page (see Fig. 7-45). The resistors will be used to simulate the DC resistance of the windings and a dummy load resistor. You can get the resistors from the Place Part dropdown list located on the toolbar at the top of the window frame, or you can get them by selecting the Place Part icon , on the toolbar at the right of the schematic page. If you use the Place Part icon, you will be presented with the Place Part dialog box shown in Fig. 7-43. Select ANALOG from the Libraries: list and then scroll down the Part List: and select part R. Notice that the parts in the Analog library have PSpice models and footprints associated with



Place Part

Part: R

Graphic: ● Normal ○ Convert

Packaging: Parts per Pkg: 1

Part:

Type: Homogeneous

Part List:
GPOLY
H
HPOLY
K_Linear
L
OPAMP
R
R_var
S
S_ST
T
TLOSSY
Libraries:
ABM
ANALOG
ATTEN1K
ATTEN1KLIB
BGA
BREAKOUT
CONNECTOR
Design Cache
EVAL
EVAL
LIBRARY17
OK
Cancel
Add Library...
Remove Library
Part Search...
Filter...
Help
R?
1k

Figure 7-43 ***Place Part*** *dialog box.*

them as indicated by the PSpice and Layout icons located under the part preview box in the lower right corner of the dialog box. Click OK. Click on the schematic page in four places to place four resistors (see Fig. 7-45 for reference).

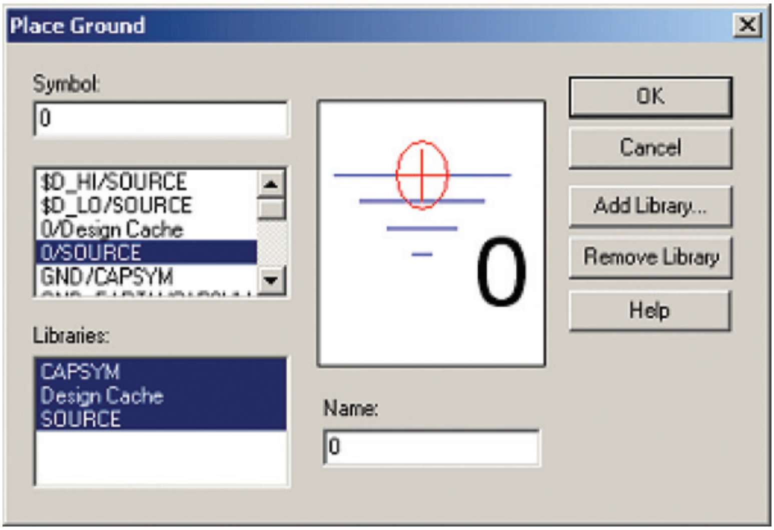
Repeat this procedure to place three inductors (part L) on the schematic page. One inductor will serve as the primary winding, and the other two will serve as the secondary windings. The inductors will be used to define the inductance (the turns ratios) of the primary and secondary windings

Next, place one K_Linear part from the Analog library on the schematic page. K_Linear defines the coupling coefficient of the windings.

Place a VSIN part on the schematic page so that we can test the operation of the transformer. VSIN is located in the SOURCE library.

Finally, place three zero (0) ground references on the schematic page. Click the Place Ground tool, GND and then select 0/SOURCE from the Place Ground dialog box as shown in Fig. 7-44. For schematic entry and Layout you can use any ground symbol, but for PSpice simulations you have to have at least one “0” reference ground.

Position and rename the components, wire the circuit, and change the values of the components as shown in Fig. 7-45. To change the reference designators (e.g., R1 or Rp) or the



Place Ground

Symbol: 0

Libraries: CAPSYM, Design Cache, SOURCE

Name: 0

$D_HI/SOURCE
$D_LO/SOURCE
0/Design Cache
0/SOURCE
GND/CAPSYM
0
OK
Cancel
Add Library...
Remove Library
Help

Figure 7-44 ***Place Ground*** *dialog box.*

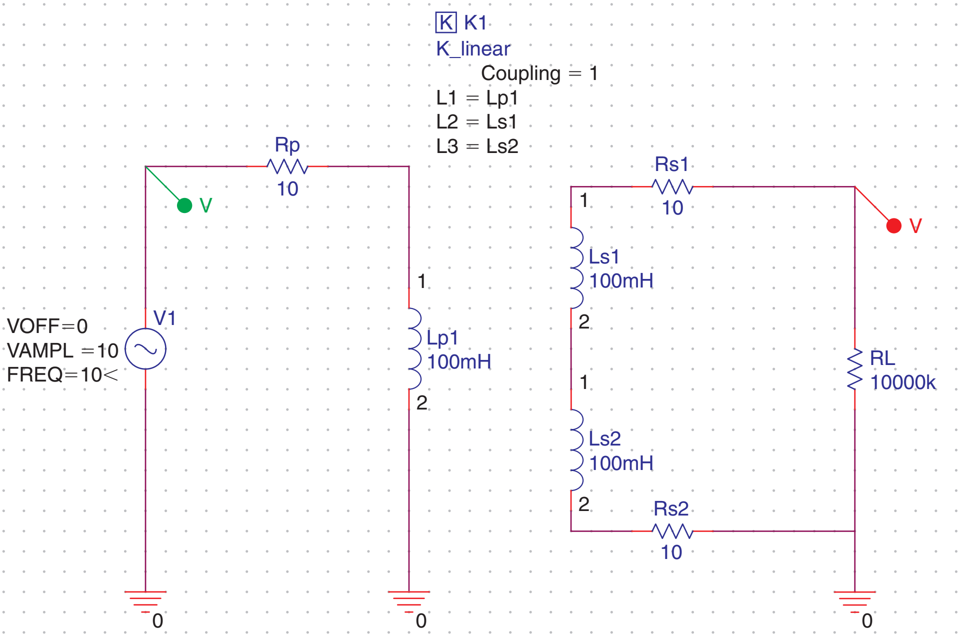
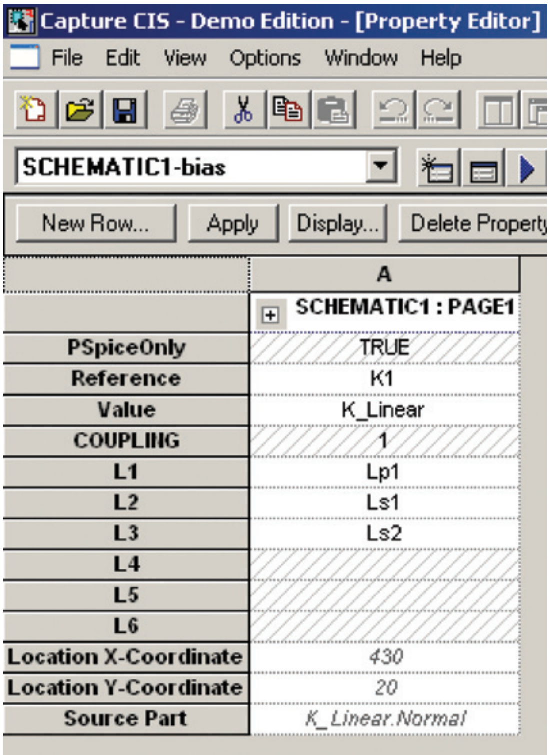

K K1
K_linear
Coupling = 1
L1 = Lp1
L2 = Ls1
L3 = Ls2
Rp
10
V
VOFF=0
VAMPL =10
FREQ=10<
V1
1
Lp1
100mH
2
Rs1
10
1
Ls1
100mH
2
1
Ls2
100mH
2
Rs2
10
V
RL
10000k
0
0
0

Figure 7-45 Schematic of the linear step-up transformer.

component values (e.g., 10 Ω), double-click the property you want to change. In the Display Properties dialog box, enter the appropriate value and click OK.

You can also modify a part's properties by double clicking the part (or click once to select it and then right click and select Edit Properties... from the pop-up). A Property Editor spreadsheet will pop-up as shown in Fig. 7-46. If the properties are listed across in rows instead of vertically in columns you can change the view by selecting the upper left-hand (corner) cell to highlight the entire spreadsheet, then right click and select Pivot from the pop-up. You can also specify how many items are listed by using the Filter by: dropdown list just above the spreadsheet cells. To display all pertinent properties select the Current properties option located at the top of the list.



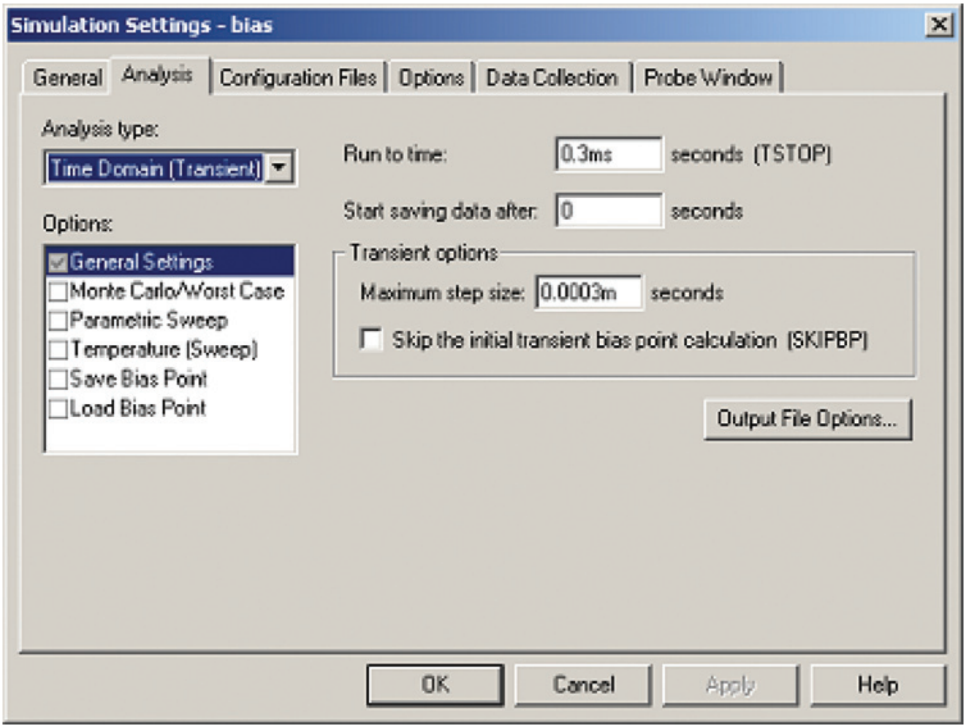
	A
	SCHEMATIC1 : PAGE1
PSpiceOnly	TRUE
Reference	K1
Value	K_Linear
COUPLING	1
L1	Lp1
L2	Ls1
L3	Ls2
L4	
L5	
L6	
Location X-Coordinate	430
Location Y-Coordinate	20
Source Part	K_Linear.Normal

Figure 7-46 Part Property Editor spreadsheet (vertical view).

To modify and display the K_Linear coupling properties, double click the coupling part to bring up the spreadsheet. Make sure that either the Current properties or the OrCAD-PSpice filter option is selected. In the L1 cell, type Lp1 (or whatever you named your primary coil) and then click the Display button, which is located just above the spreadsheet cells. Enter Ls1 in the L2 cell and Ls2 in the L3 cell and click the Display button for both of these parameters too. The L1, L2, etc., cells establish which coils are coupled as part of the transformer. You can have additional/separate coupling coefficients for different sets of coils, but for this example we will have all three equally coupled together using the single linear coupler. Once you have finished, close the spreadsheet by clicking the X button in the upper right-hand corner of the spreadsheet.

Now we need to simulate the part with PSpice. There are several types of simulations you can perform with PSpice. In this example we will perform a **time domain analysis** so that we can see the AC waveforms at the input of the transformer and at the load resistor.

To test the circuit we need to set up a simulation profile. **To set up a simulation profile** choose Edit (or New) Simulation Profile from the PSpice menu. In the Simulation Settings dialog box (see Fig. 7-47) select the Analysis tab. In the Analysis type: dropdown list, select Time Domain (Transient). Set the rest of the parameters as shown in Fig. 7-47 and then click OK.



Simulation Settings - bias

Analysis type: Time Domain (Transient)

Options:
☑ General Settings
☐ Monte Carlo/Worst Case
☐ Parametric Sweep
☐ Temperature (Sweep)
☐ Save Bias Point
☐ Load Bias Point

Run to time: 0.3ms seconds (TSTOP)

Start saving data after: 0 seconds

Transient options

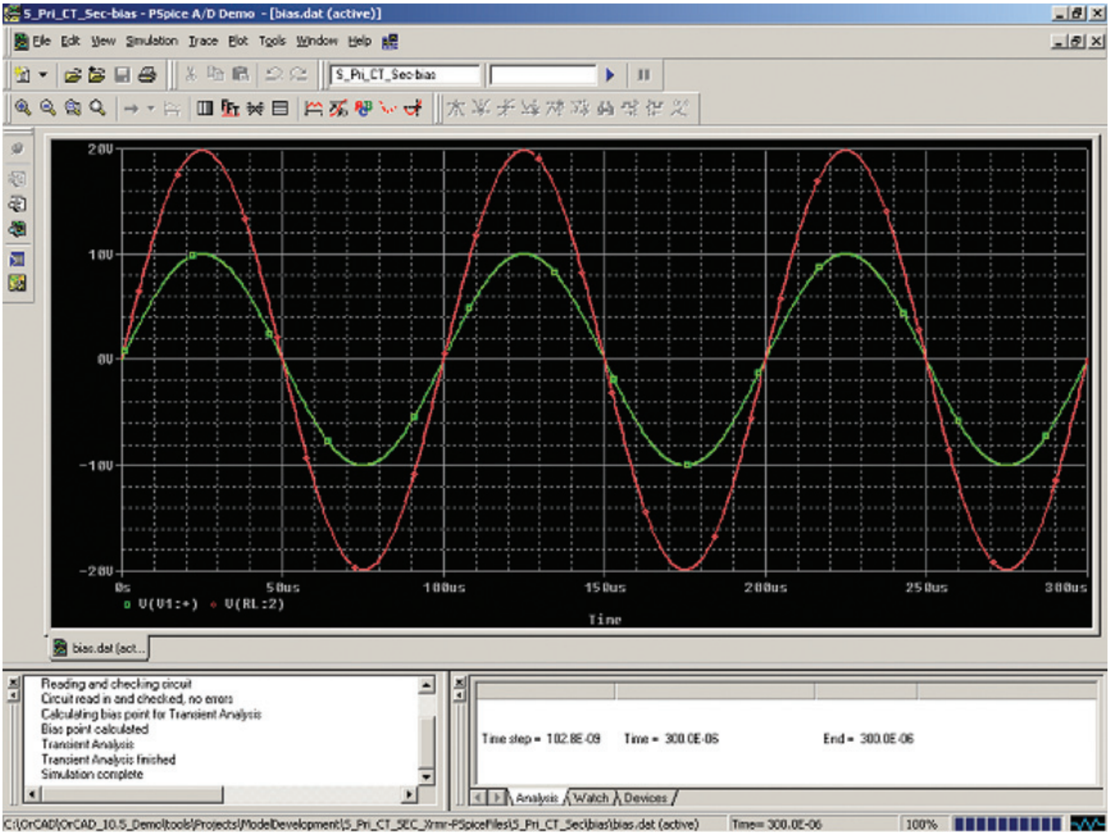
Maximum step size: 0.0003m seconds

☐ Skip the initial transient bias point calculation (SKIPBP)

Figure 7-47 *Simulation Settings dialog box.*

Place voltage markers on the circuit to specify which voltages to display in the PSpice Probe window. Click the button on the toolbar and place a probe on the wire coming from VSIN (green marker) and one (red marker) on the wire going from the secondary winding to the load resistor (RL).

Start the simulation by clicking the Run PSpice button. ▶ PSpice runs the simulation and displays the results in a probe window as shown in Fig. 7-48. The voltage curves show that the transformer functions as a 1:2 step-up transformer since the output (red marker curve) is twice as high as the input (green marker curve). Additional tests (e.g., frequency response) could be performed to validate the circuit model further, but these will not be discussed here.


5_Pri_CT_Sec-bias - PSpice A/D Demo - [bias.dat (active)]
File Edit View Simulation Trace Plot Tools Window Help
5_Pri_CT_Sec-bias
20V
10V
0V
-10V
-20V
0s
50us
100us
150us
200us
250us
300us
V(V1:+)
V(RL:2)
Time
bias.dat (act...
Analysis
Watch
Devices

```
Reading and checking circuit
Circuit read in and checked, no errors
Calculating bias point for Transient Analysis
Bias point calculated
Transient Analysis
Transient Analysis finished
Simulation complete
```

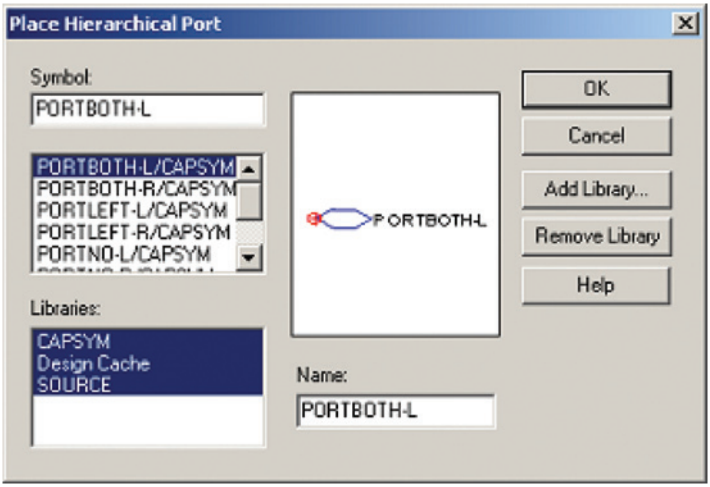
```
Time step = 102.8E-09     Time = 300.0E-06          End = 300.0E-06
```

```
C:\OrCAD\OrCAD_10.5_Demo\tools\Projects\ModelDevelopment\5_Pri_CT_SEC_Xrmr-PSpiceFiles\5_Pri_CT_Sec\bias\bias.dat (active)   Time= 300.0E-06   100%
```

Figure 7-48 PSpice probe window for the center-tap transformer.

Since the circuit model has been validated, we will now prepare to make a PSpice model of the circuit. Begin by deleting the VSIN source, the load resistor RL, and all of the ground references.

Add ports to the schematic, which will serve as the leads of the transformer. Click the Place Port tool, ᗉP. Select the PORTBOTH-L port from the Place Hierarchical Port dialog box as shown in Fig. 7-49. All of the port symbols behave identically in Capture, PSpice, and Layout. The only difference is the appearance on the schematic. Since the transformer is a passive device, we will use the symbol that indicates that an applied signal can go either


Place Hierarchical Port
OK
Cancel
Add Library...
Remove Library
Help
PORTBOTH-L

Symbol:
PORTBOTH-L

PORTBOTH-L/CAPSYM
PORTBOTH-R/CAPSYM
PORTLEFT-L/CAPSYM
PORTLEFT-R/CAPSYM
PORTNO-L/CAPSYM

Libraries:
CAPSYM
Design Cache
SOURCE

Name:
PORTBOTH-L

Figure 7-49 ***Place Hierarchical*** *Port dialog box.*

direction. Click OK and place five of the ports on the schematic page (two for the primary and three for the secondary).

Reposition, connect, and label the ports as shown in Fig. 7-50.

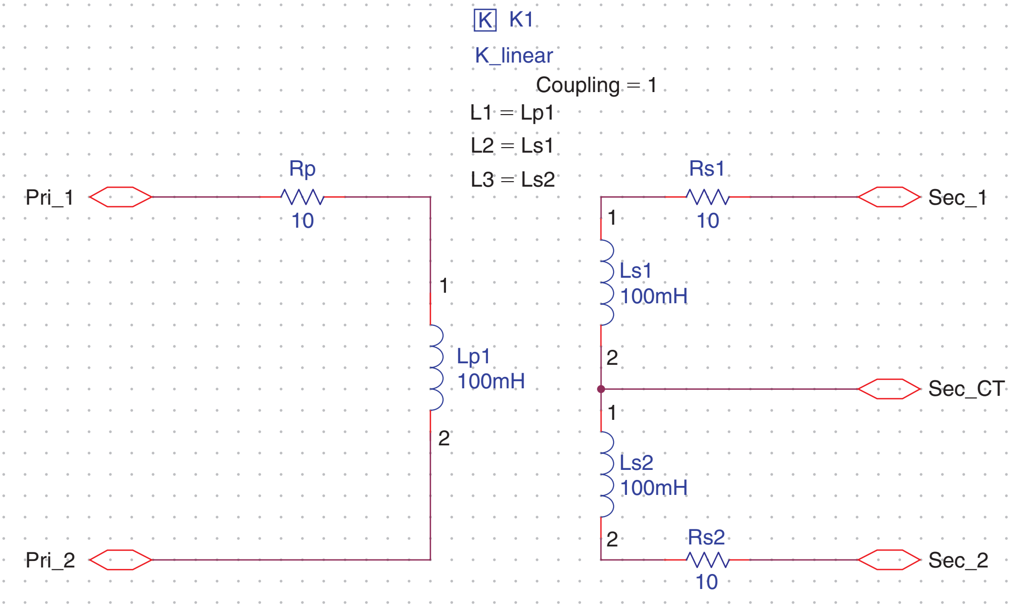
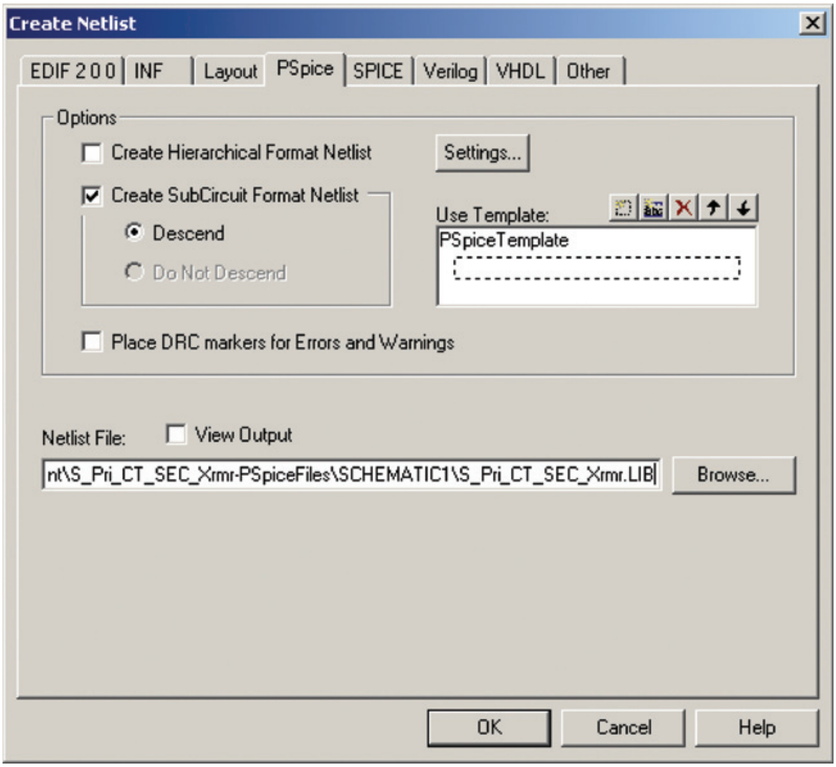

K K1
K_linear
Coupling = 1
L1 = Lp1
L2 = Ls1
L3 = Ls2
Pri_1
Rp
10
1
Lp1
100mH
2
Pri_2
Rs1
10
1
Ls1
100mH
2
Sec_1
Sec_CT
1
Ls2
100mH
2
Rs2
10
Sec_2

Figure 7-50 Hierarchical ports in the circuit design.

Display the Project Manager window by minimizing the schematic page or by selecting 2 C:/OrCAD... *ProjectName*.opj from the Window menu. Select the Design icon and then select Create Netlist from the Tools menu.

In the Create Netlist dialog box (Fig. 7-51), select the PSpice tab. Check the Create SubCircuit Format Netlist box and the Descend radio button. A default name will be given to the netlist. Modify the path and name as desired. Make sure the name ends with the .LIB file extension. Click OK.



Options

☐ Create Hierarchical Format Netlist

☑ Create SubCircuit Format Netlist

● Descend

○ Do Not Descend

Use Template: PSpiceTemplate

☐ Place DRC markers for Errors and Warnings

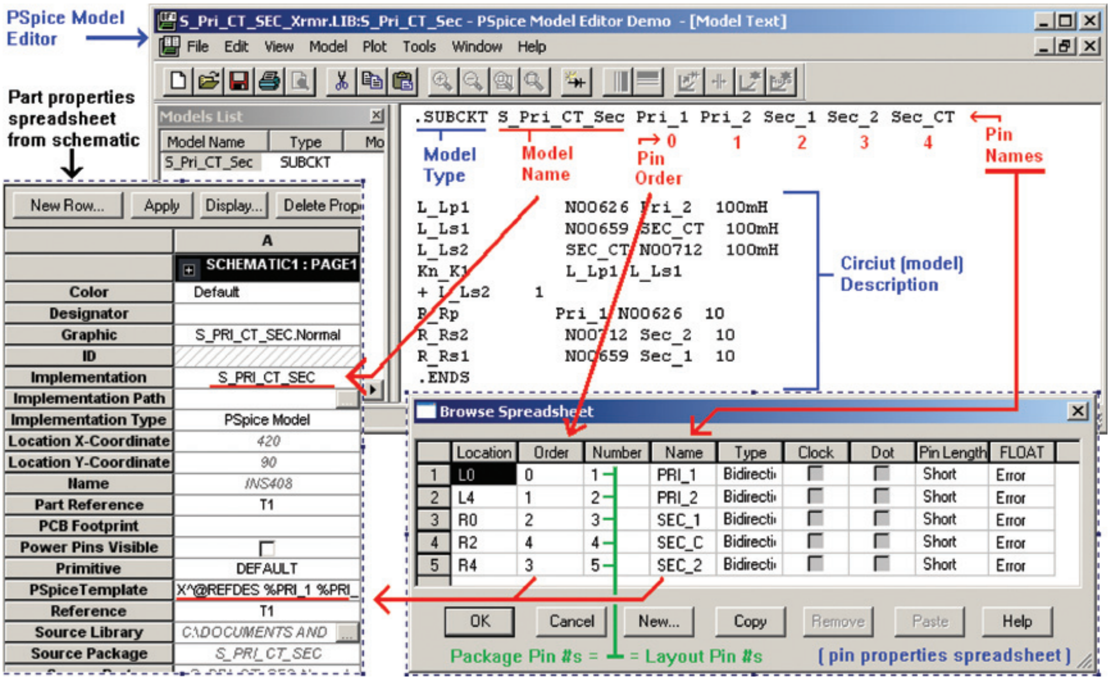
Netlist File: ☐ View Output

nt\S_Pri_CT_SEC_Xrmr-PSpiceFiles\SCHEMATIC1\S_Pri_CT_SEC_Xrmr.LIB

Figure 7-51 ***Create Netlist*** *dialog box.*

You now have a PSpice library file with one model (the transformer) in it. You can use Method 3 or 4 to generate a Capture part library from this model or add it to an existing part library. To complete the example we will use Method 4 so that we can take a look at the PSpice model that was generated by Capture.

Start the PSpice Model Editor again. From the File menu, select Open and navigate to the transformer library that you made above. Click on the S_Pri_CT_Sec model to display the model in the editing window as shown in Fig. 7-52. Notice that the model type is .SUBCKT (a subcircuit). The name of the library is whatever you specified as the netlist file in the


PSpice Model Editor
Part properties spreadsheet from schematic
S_Pri_CT_SEC_Xrmr.LIB:S_Pri_CT_Sec - PSpice Model Editor Demo - [Model Text]
File
Edit
View
Model
Plot
Tools
Window
Help
Models List
Model Type
Model Name
Pin Order
0
1
2
3
4
Pin Names
Circiut (model) Description
Browse Spreadsheet
OK
Cancel
New...
Copy
Remove
Paste
Help
Package Pin #s = = Layout Pin #s
(pin properties spreadsheet)
New Row...
Apply
Display...
Delete Prop

Model Name	Type	Mo
S_Pri_CT_Sec	SUBCKT	

```
.SUBCKT S_Pri_CT_Sec Pri_1 Pri_2 Sec_1 Sec_2 Sec_CT
L_Lp1         N00626 Pri_2  100mH
L_Ls1         N00659 SEC_CT  100mH
L_Ls2         SEC_CT N00712  100mH
Kn_K1         L_Lp1 L_Ls1
+ L_Ls2     1
R_Rp         Pri_1 N00626  10
R_Rs2         N00712 Sec_2  10
R_Rs1         N00659 Sec_1  10
.ENDS
```

	A
	SCHEMATIC1 : PAGE1
Color	Default
Designator	
Graphic	S_PRI_CT_SEC.Normal
ID	
Implementation	S_PRI_CT_SEC
Implementation Path	
Implementation Type	PSpice Model
Location X-Coordinate	420
Location Y-Coordinate	90
Name	INS408
Part Reference	T1
PCB Footprint	
Power Pins Visible	☐
Primitive	DEFAULT
PSpiceTemplate	X^@REFDES %PRI_1 %PRI_
Reference	T1
Source Library	C:\DOCUMENTS AND
Source Package	S_PRI_CT_SEC

	Location	Order	Number	Name	Type	Clock	Dot	Pin Length	FLOAT
1	L0	0	1	PRI_1	Bidirecti	☐	☐	Short	Error
2	L4	1	2	PRI_2	Bidirecti	☐	☐	Short	Error
3	R0	2	3	SEC_1	Bidirecti	☐	☐	Short	Error
4	R2	4	4	SEC_C	Bidirecti	☐	☐	Short	Error
5	R4	3	5	SEC_2	Bidirecti	☐	☐	Short	Error

Figure 7-52 PSpice transformer model generated from a Capture project.

Create Netlist dialog box, and the name of the part is the schematic folder name in the Capture design (see Fig. 7-42). At this point you could modify the part to add specific requirements that will carry forward into the Capture part. Once the model editing (if any) is completed, generate the Capture part as described above using Method 3 or Method 4.

Note that, as shown in Fig. 7-52, the pin *names* and *order* in the Capture part (as indicated in the pin properties spreadsheet) and the PSpice Template (as indicated in the part properties spreadsheet) must match the pin *names* and *order* in the PSpice model exactly or simulations will fail. The Implementation name in the part properties spreadsheet must also match the model name in the PSpice model file. And finally, the part's pin *numbers* must match the pin (padstack) *numbers* in Layout, which is governed by the part's datasheet. If the part's pin number is a letter instead of a number (e.g. "A" for the anode of a diode) then the pad in layout must be named accordingly or the AutoECO will fail.

Adding PSpice templates (models) to preexisting Capture parts

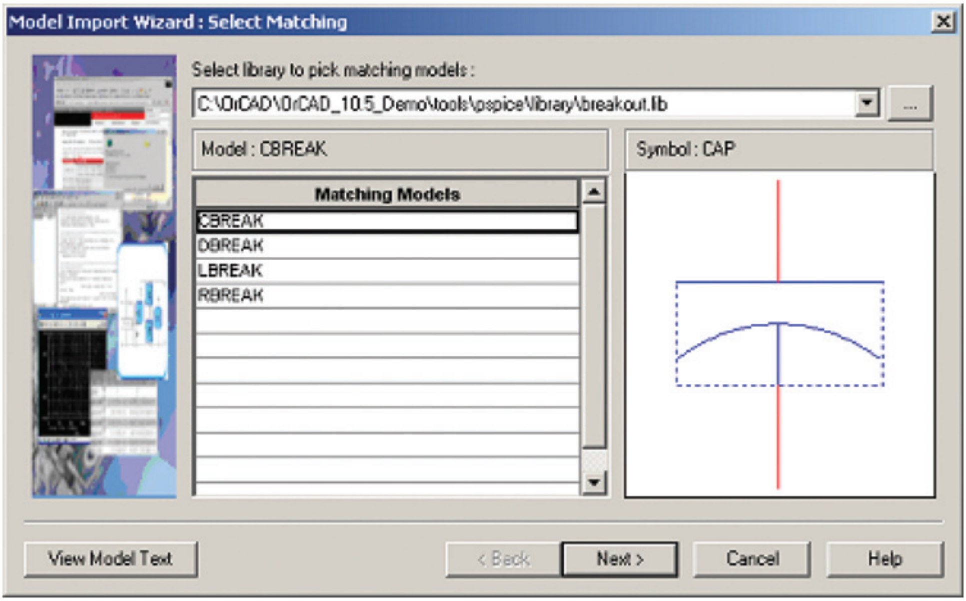
Rather than using Method 3 or 4 to make a new part from the transformer PSpice library, you might wonder why we did not just add the PSpice model to the transformer that was already created in the first example (for which Method 1 was used). In older versions of OrCAD this was somewhat of a challenging task (e.g. you have to know what "X^@REFDES %A %B %Y %VCC %GND @MODEL PARAMS:\n+ IO_LEVEL=@IO_LEVEL MNTYMXDLY=@MNTYMXDLY" means). Fortunately, it is a simpler matter with version 10.5.

In this example we will see how to add an existing PSpice model to an existing Capture part. The Demo version does not allow doing this with parts that have more than two leads. So we will add a basic capacitor model to one of Capture's capacitor parts that does not have a model associated with it.

If you recall from Chap. 2 we used a basic capacitor (part C or CAP) from Capture's discrete.olb library. The part did not have a Layout footprint or PSpice model associated with it. We will add a PSpice model to the part now. The location of the basic PSpice capacitor model that we will use is in the PSpice breakout library (breakout.lib).

To add a PSpice model to an existing Capture part, start Capture and select Open → Library and select the library with the part to which you want to add a PSpice model (use discrete.olb for this example). Find the capacitor (C or CAP, for example) in the Capture Library Part Manager and click the part's icon to select it. Right click and select Associate PSpice Model... from the pop-up.

At the Import Model Wizard dialog box (Fig. 7-53), use the Browse button in the upper right-hand corner to find the PSpice model that you want to associate with the Capture part.



Select library to pick matching models : C:\OrCAD\OrCAD_10.5_Demo\tools\pspice\library\breakout.lib

Model : CBREAK

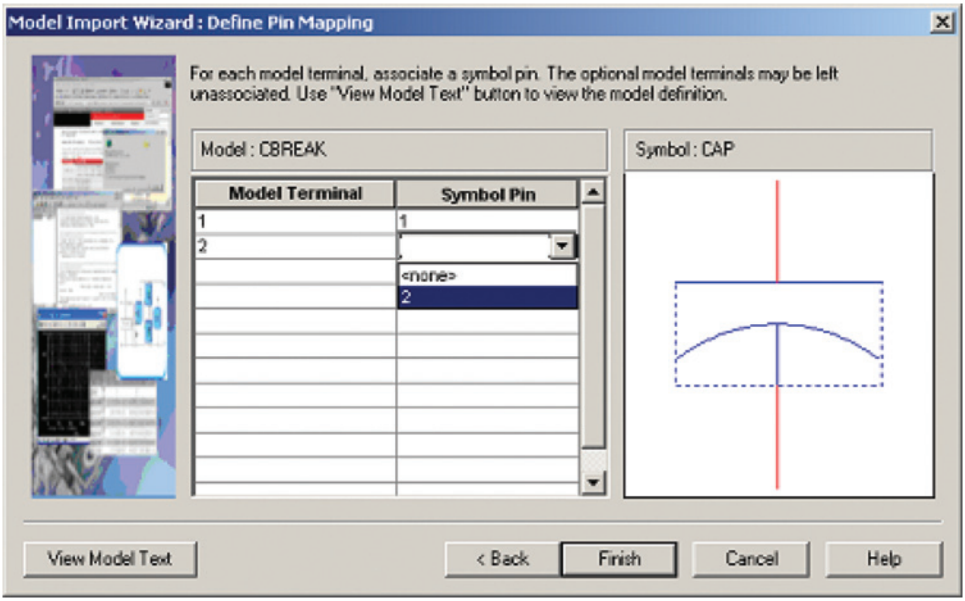
Symbol : CAP

Matching Models:
CBREAK
DBREAK
LBREAK
RBREAK

Figure 7-53 Matching parts with the Model Import Wizard.

The wizard automatically searches through the PSpice library and lists all models in the Matching Models window that have the same number of pins as the Capture part you selected in the Part Library Manager. Select the CBREAK model and click Next.

The wizard then displays the Pin Matching tool shown in Fig. 7-54. This is where you connect the PSpice model pin to the Capture part pin. Click Finish when the pins are matched. The


Model Import Wizard : Define Pin Mapping
Model Terminal
Symbol Pin
<none>
View Model Text
< Back
Finish
Cancel
Help

For each model terminal, associate a symbol pin. The optional model terminals may be left unassociated. Use "View Model Text" button to view the model definition.

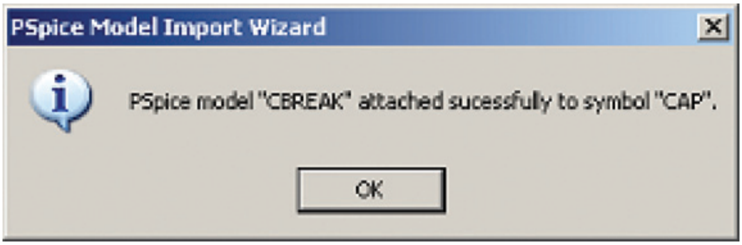
Model : CBREAK

Symbol : CAP

Model Terminal	Symbol Pin
1	1
2	2

Figure 7-54 Mapping pins with the Model Import Wizard.

information box shown in Fig. 7-55 should be displayed, indicating that the capacitor now has a PSpice model attached to it.


PSpice Model Import Wizard
OK

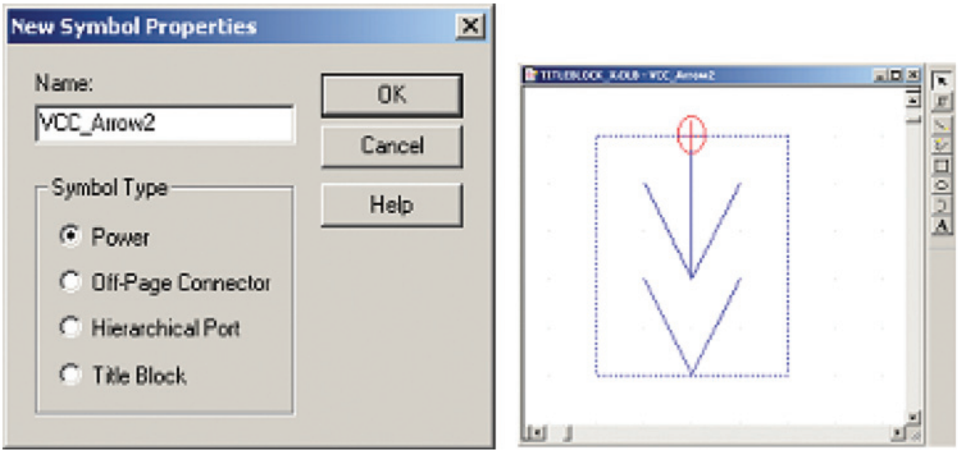
PSpice model "CBREAK" attached sucessfully to symbol "CAP".

Figure 7-55 Model successfully added to a Capture part.

Constructing Capture Symbols

There are four different types of symbols used in Capture: (1) power/ground symbols, (2) off-page connectors, (3) hierarchical ports, and (4) title blocks.

To make a new power symbol open the capsym.olb library. Select the Library icon under the Library folder. From the Design menu, choose New Symbol. In the New Symbol Properties dialog box (Fig. 7-56), enter the name and select the appropriate radio button from the Symbol Type group box. Click OK. A part editing window and drawing toolbar will be displayed. Use the graphics tools to make the symbol. Close the editing window and save the symbol. Save and close the library.



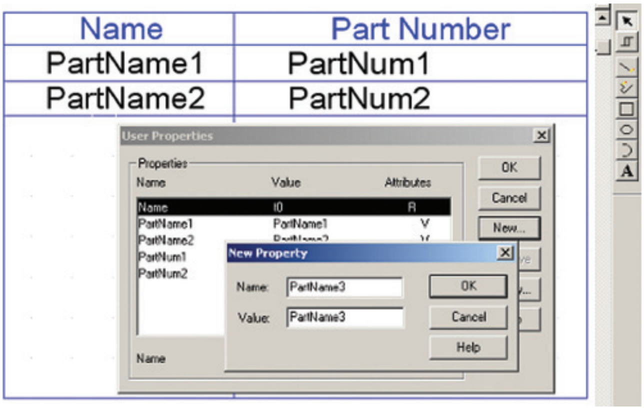
Name: VCC_Arrow2

Symbol Type
- ● Power
- ○ Off-Page Connector
- ○ Hierarchical Port
- ○ Title Block

Figure 7-56 Making a new power symbol.

The construction methods for power symbols, off-page connectors, and hierarchical ports are similar (although they all have their own functionality). The title block is different from the other three. There are two types of title blocks: default and optional. Every new project has a default title block, which you can specify for each project by going to Options → Design Template... on the schematic page menu. You can also add optional title blocks by going to Place → Title Block..., also on the schematic page menu. The title blocks are located in the capsym library. You can construct your own title blocks and save them with the others or make your own library of power symbols and title blocks, etc.

To make a new title block open or make a new Capture library, select the Library icon, and from the Design menu select New Symbols. At the New Symbol Properties dialog box (Fig. 7-56) select Title Block and click OK. Just as with the power symbols, you will be presented with a part editing window. Use the graphics tools to construct the box (Fig. 7-57



Name	Part Number
PartName1	PartNum1
PartName2	PartNum2

Properties

Name	Value	Attributes
Name	I0	R
PartName1	PartName1	V
PartName2	PartName2	V
PartNum1		
PartNum2		

Name

Name: PartName3

Value: PartName3

Figure 7-57 Example of a new title block used as a parts list.

shows an example of a parts list) and the Text tool to add titles and headers. To enter the text that can be modified on schematic pages double click in a free area within the window to display the User Properties dialog box. Click the New... button to create new text objects. The name field is required but you can either leave the value field empty or enter a default value. Click OK. To make an object field visible select Part Properties from the Options menu and click the Display button in the User Properties dialog box for the field of interest. After you have saved the block you can add it to any schematic page.

That completes the chapter on making Capture parts and symbols.

CHAPTER 8

Making and Editing Layout Footprints

Footprints provide a means of physically attaching components to your PCB, and they provide electrical connectivity as defined by the netlist generated in Capture. While the Demo version of Layout contains only a few footprints in the Ex-gui.LLB library, version 10.5 contains thousands of footprints within many different libraries. Although the libraries are comprehensive, there will be times when you will need to make your own.

This purpose of this chapter is to:

1. introduce the Library Manager,
2. introduce Layout's footprint libraries and naming conventions,
3. discuss the composition of a footprint,
4. demonstrate the basic process of making a footprint,
5. provide a detailed explanation of padstacks,
6. provide footprint and padstack design examples, and
7. demonstrate how to use the pad array generator for pin grid arrays (PGAs) and ball grid arrays (BGAs).

Introduction to the Library Manager

The padstacks, footprints, and footprint libraries in OrCAD Layout are handled using the Library Manager. To use the Library Manager, open Layout and, from the session frame, select Library Manager from the Tools pulldown menu, or if you have a design (.MAX) file open, you can click the button on the toolbar. The Library Manager is shown in Fig. 8-1. Within the main window are two windows: the Library Manager itself and an editing window. At the top of the editing window the title Library—Pin Tool (DRC Off) will be displayed if you have the Pin Tool button selected or Library—Obstacle Tool (DRC Off) if you have the Obstacle Tool button selected.

The main window has the standard Layout toolbar and buttons, but buttons associated with routing traces, etc., are grayed out since there are no traces to work with—only pins, obstacles, and text. The Library Manager lists the available Layout package libraries and, once

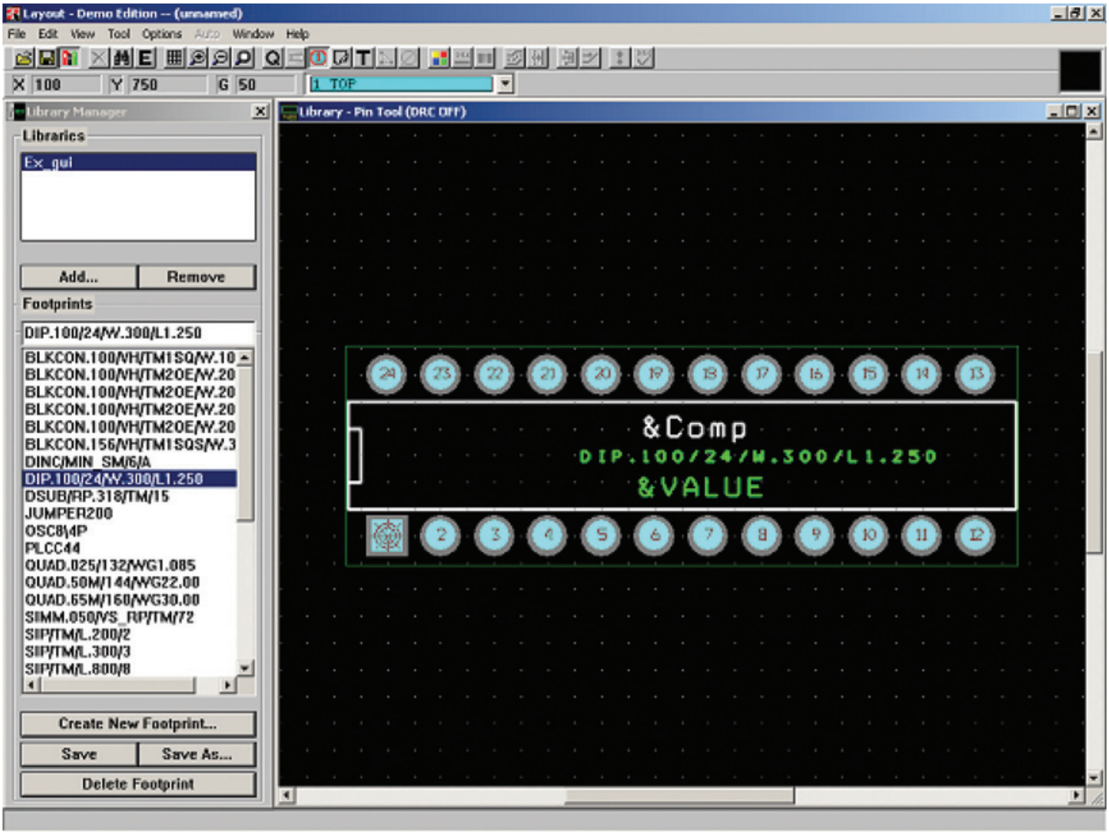

Layout - Demo Edition -- (unnamed)
File
Edit
View
Tool
Options
Auto
Window
Help
X 100
Y 750
G 50
1 TOP
Library Manager
Libraries
Ex_gui
Add...
Remove
Footprints
DIP.100/24/W.300/L1.250
BLKCON.100/VH/TM1SQ/W.10
BLKCON.100/VH/TM2OE/W.20
BLKCON.100/VH/TM2OE/W.20
BLKCON.100/VH/TM2OE/W.20
BLKCON.100/VH/TM2OE/W.20
BLKCON.156/VH/TM1SQS/W.3
DINC/MIN_SM/6/A
DIP.100/24/W.300/L1.250
DSUB/RP.318/TM/15
JUMPER200
OSC8\4P
PLCC44
QUAD.025/132/WG1.085
QUAD.50M/144/WG22.00
QUAD.65M/160/WG30.00
SIMM.050/VS_RP/TM/72
SIP/TM/L.200/2
SIP/TM/L.300/3
SIP/TM/L.800/8
Create New Footprint...
Save
Save As...
Delete Footprint
Library - Pin Tool (DRC Off)
24
23
22
21
20
19
18
17
16
15
14
13
&Comp
DIP.100/24/W.300/L1.250
&VALUE
2
3
4
5
6
7
8
9
10
11
12

Figure 8-1 A 24-pin DIP as seen in the Library Manager.

you select a particular library, the footprints that are stored inside the library are listed in the Footprints window. When you select a particular footprint within a library, the footprint is displayed in the editing window. From the Library Manager you can create new footprints or save an existing footprint that has been modified, you can create a new library using the Save As... button, and you can delete existing footprints. You can read additional information on the Library Manager in Chap. 3 and Chaps. 12–14 of the *Layout User's Guide* (layug.pdf). We will be working extensively with the Library Manager in the next few sections.

Introduction to Layout's Footprint Libraries and Naming Conventions

While the Demo version has only one library (Ex-gui.LLB), which contains 36 footprints, version 10.5 contains more than 50 libraries with over 6000 footprints. Chances are that one of the libraries has the footprint you are looking for (or one close to it), so before you spend time creating a new footprint, it is a good idea to find out if it already exists. The trick to finding a particular footprint is in knowing what libraries are available and what footprints they contain.

Layout's footprint libraries

Layout lists its footprints by mounting technology and lead style as well as body style. For example, an LT1363 op-amp is available in both the eight-pin through-hole DIP (dual inline package) and the surface-mount SOIC (small outline integrated circuit) packages. If you look through the 6000 footprints included with the full version of Layout you ***will*** find an eight-pin DIP footprint (DIP.100/8/W.300/L.400) in the DIP100T library, but you ***will not*** find any libraries or footprints labeled SOIC. Since SOIC packages have gull-wing-type leads, Layout's SOIC packages are placed in the SOG library (small outline gull-wing lead), where one of the three available SOIC-8 packages is called SOG.050/8/WG.244/L.200.

So how does one go about finding the desired footprint without having to search through 50 or so libraries? Eventually you will just know where particular footprints are (and which ones do not exist). But while you are still becoming familiar with the libraries, you can simplify the search by answering a couple of questions up front. The questions you should answer are:

1. What type of *component* is it (discrete, IC, or a connector)?
2. How is the part *attached* to the board (e.g., through-hole, solder mount)?
3. What type of *leads* does the package have (e.g., “J”, axial, radial)?

Table 8-1 shows Layout's 50 libraries (included in the full version only) categorized by package type and method of part attachment to the board. By answering question 1 above, you can narrow your search to just one of the four rows. Then by answering question 2, you can narrow the options to one column. This narrows the options to a single block of footprints (where the row and column intersect). Within the one block, the correct library is often evident by its name. In some cases though, you may need to answer the third question above. For example, if you are looking for an eight-pin SOIC, then you would look in the IC row and the surface mount column, which narrows the options to four choices. BGA and DIP are obviously not correct, so the list is further reduced to just SOG or SOJ. Answering question 3 above suggests that the SOG library is the correct choice since SOIC packages are small outline packages that have gull-wing-type leads, not the J-leads.

Naming conventions

Once you find the correct library for the type of footprint you are looking for, the next task is to identify the correct footprint (i.e., correct number of pins and pin spacing, etc.). Land pattern naming conventions are specified by standards organizations such as IPC, JEDEC, or EIA. For example, IPC-7351 (Table 3-15) lists the land pattern naming conventions for many industry package types. Layout uses a similar form for its naming convention. Only a brief explanation and a few examples are provided here, but Appendix C provides a detailed list of package types.

Within a given library, many of the footprint naming conventions will often follow a pattern. However, not all of the libraries follow the same pattern—if there is one at all. The Ex_gui library included with the Demo edition of Layout contains 36 footprints from 12 different

	Method of attachment to board				
Package type	**Surface mount**	**Mixed: surface mount and through-hole**	**Through-hole**	**Mixed: through-hole and copper area**	**Copper area**
Discrete components	SM.LLB	RELAY.LLB SIP.LLB TO.LLB VRES.LLB	TM_AXIAL.LLB TM_CAP_P.LLB TM_CYLND.LLB TM_DIODE.LLB TM_DISC.LLB TM_RAD.LLB		
Integrated circuits	BGA.LLB DIP100B.LLB SOG.LLB SOJ.LLB	CLCC.LLB PLCC.LLB QUAD.LLB QUADB.LLB	DIP100T.LLB PGA.LLB		
Connectors		TELE.LLB	BCON100T.LLB BCON156T.LLB DCON050T.LLB DCON085T.LLB DSUBT.LLB ECON100T.LLB FBUS.LLB LCON100T.LLB PC104.LLB PCON100T.LLB PCON156T.LLB RF.LLB SBUS.LLB SIMM050T.LLB SIMM100T.LLB WCON100T.LLB ZIGZAG.LLB	DIN.LLB PCI.LLB XT.LLB	DIMM050F.LLB ISA.LLB SIMM050F.LLB SIMM100F.LLB
Other			JUMPER.LLB TRAINING.LLB		

Table 8-1 Foot print library categories (full version only)

libraries, which are normally included with the full version of Layout, so the naming conventions appear to vary considerably. We will take a look at a couple of examples so that you can get an idea of the naming conventions.

The first example is of the 24-pin DIP package shown in Fig. 8-1. The footprint, DIP.100/24/W.300/L1.250, is located in the Ex_gui library in the Demo edition and in the DIP100T library in the full version. The general format for the through-hole DIP footprints is shown in Fig. 8-2.

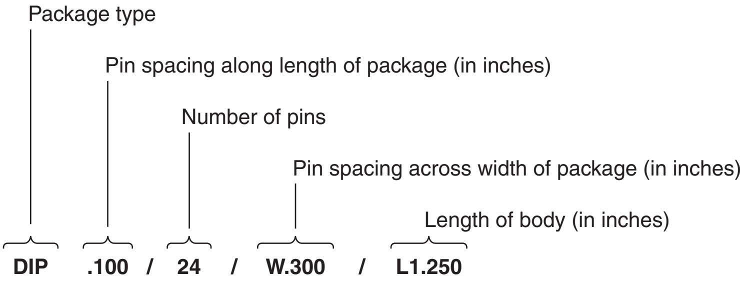

Package type
Pin spacing along length of package (in inches)
Number of pins
Pin spacing across width of package (in inches)
Length of body (in inches)
DIP .100 / 24 / W.300 / L1.250

Figure 8-2 Naming convention for a 24-pin DIP package.

Comparing this description to the dimensions of the DIP-24 package shown in Fig. 8-3, it can be seen that some of the numbers describe pin spacing while others describe body dimensions. For instance, the length of the body is included in the name since the length of the body is greater than the space that is defined by the 12 pins that are spaced 0.100 in. apart (1.250 in. is greater than 1.100 in.). The width of the IC body is not used in the name since its “space” is accounted for within the pin spacing defined by the 0.300-in. dimension. So the intent of the naming convention is to define the pin spacing adequately and indicate the amount of board real estate occupied.

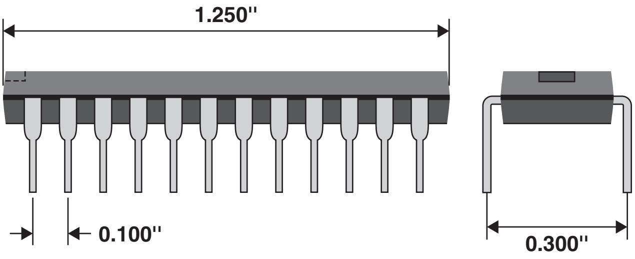

1.250"
0.100"
0.300"

Figure 8-3 A 24-pin dual inline package (DIP-24) and its dimensions.

Another example of this type of naming convention is the SOIC package shown in Fig. 8-4. Its footprint, SOG.050/16/WG.244/L.400, is located in the Ex_gui library in the Demo edition and in the SOG library in the full version.

Figure 8-5 shows the 16-pin SOIC footprint used in Layout and an OEM-recommended land pattern. Notice that the Layout pads are not the same as the OEM pads except that in both cases the pads are 0.050 in. apart. Layout uses the generic SOG nomenclature because packages such as SOIC, SIOC-150, Narrow body SOIC, and SOP have essentially the same basic footprint with the exception of slight variations in body width or pin extension length, etc. Component

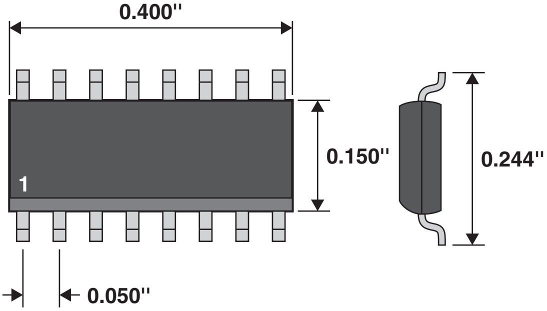


Figure 8-4 A 16-pin SOIC package and its significant dimensions.

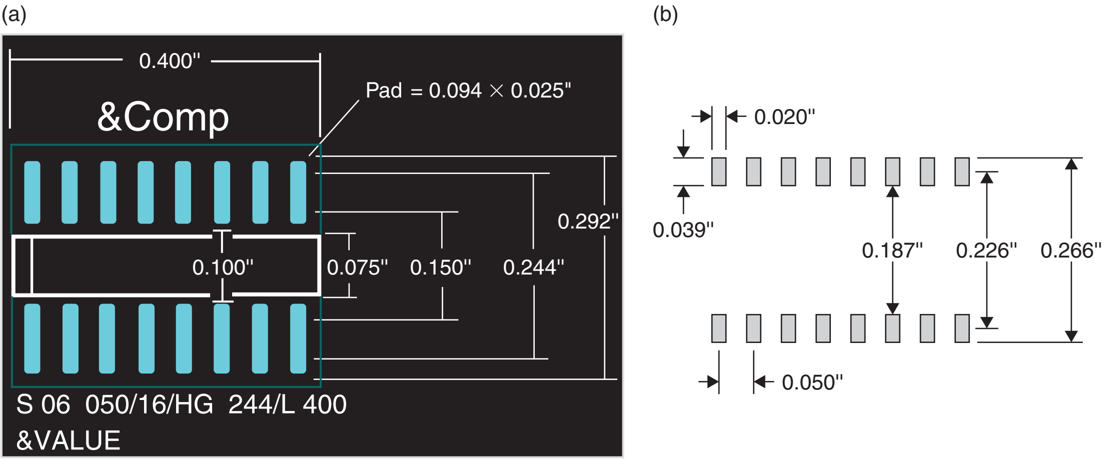


Figure 8-5 PCB footprints for the 16-pin SOIC package. (a) Layout footprint from ***SOG.LLB.*** *(b) OEM-suggested land pattern.*

manufacturers may have specific footprint specifications for their part, but PCB design and device packaging standards (such as MIL-STD-782 or IPC-7351 or JEDEC standards) specify baseline design requirements, which Layout tends to follow for the most part. So rather than make a library for each variation of the small outline package, one library contains footprints that accommodate as many of these packages as possible while meeting minimum baseline design standards. For further reading on design requirements, please see Chap. 4 for a list of industry standards and Appendix C for more information on packages and footprints.

Not all of the footprints in the libraries use the naming convention described above. Discrete components are often simply listed by their name with certain optional descriptions. For example, surface-mount resistors located in **SM.LLB** (the library for discrete surface-mounted devices) are simply SM/R_0805 or SM/R_1206, etc., and capacitors are SM/C_0805 or SM/C_1206, etc. Discrete transistor footprints are named in a similar way. Surface-mount transistors (also in SM.LLB) are listed as SM/SOT23_XXX, where the XXX refers to the names of the pins rather than the physical dimensions of the pins (e.g., XXX can be EBC, for emitter base collector). Through-hole transistors are in the TO.LLBlibrary and are listed simply by body style (e.g., TO18) or by body style and optional information (e.g., TO92/100/EBC, where 100 is the lead spacing in mils and EBC is used as described above).

Some of the library naming conventions may not be obvious. Not only do some of the names resemble a code, but the multitude of different types of packages available in industry can add to the confusion. Good sources for package information can be found at the following Web sites:

- IPC Web site—free land pattern viewer based on IPC-7351 standard;
- http://www.fairchildsemi.com/products/discrete/packaging/pkg.html;
- http://www.national.com/packaging/parts/;
- http://www.intersil.com/design/packages/hermetic.asp;
- http://www.diodes.com/datasheets/ap02002.pdf.

The Composition of Footprints

A Layout footprint consists of **numbered padstacks** (pads), **obstacles** (graphical objects), **text**, and **datums** (orientation marks such as the origin and insertion point). The most important component of a footprint is the padstack.

Padstacks

Pads in Layout are called “padstacks”.

Figure 8-6 shows an example of a multilayer padstack from a PCB’s perspective. Padstacks define every aspect of how a component’s pins will be fastened to the PCB and how traces will be connected to them. Padstack definitions specify areas for copper pads on outer and inner routing layers, thermal reliefs and clearance areas in plane layers, openings in soldermasks, and solder paste (optional). From the PCB designer’s perspective, the drill hole may also be considered part of the padstack definition, but the copper used to plate through-holes and vias is not. This is because the plating thickness is controlled by the board manufacturer and is typically insignificant relative to the drill and lead diameters. More about the lead-to-hole diameter is discussed in an example below and in Chap. 5.

Figure 8-7 shows a “virtual” multilayered padstack from Layout’s perspective. Within Layout, the padstack elements are two-dimensional disks. Each disk resides on its own layer, and the distance between each layer is zero. The pads in Fig. 8-7 are shown in the same “order” as the pads shown in Fig. 8-6 for comparison. In Layout, however, the disks are not necessarily in the order that you would consider to be from the top to the bottom of the board. You will also notice that plane layers (whether copper or silk screen) are shown in the negative view; this helps keep the board from becoming too distracting. Objects that are “global” can be found on a single layer (a thermal relief for example) or can be on all layers at the same time (a board outline, for example). A global object usually has a distinct color regardless of which layer it is on so that it is easy to differentiate it from objects on other layers.

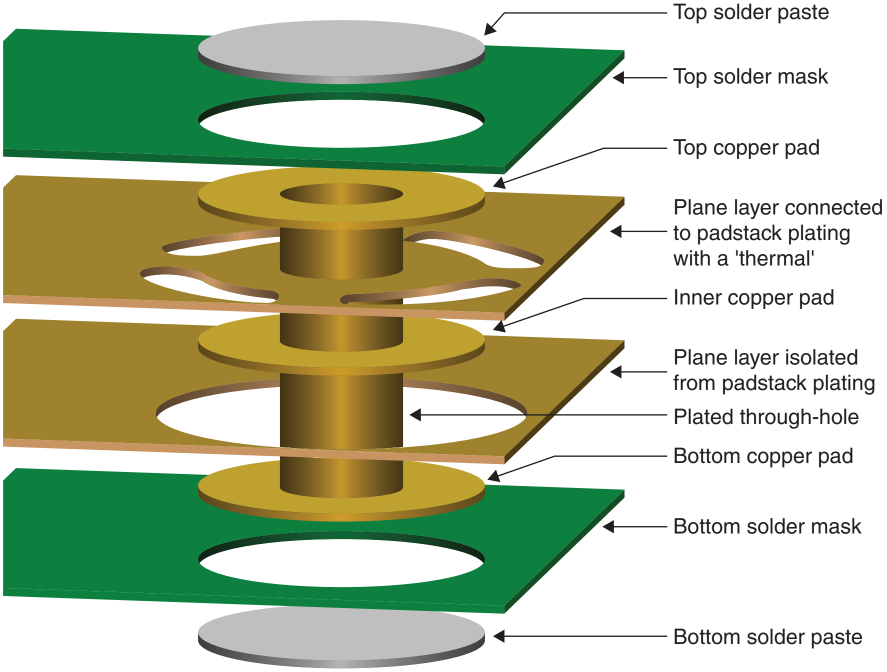

Top solder paste
Top solder mask
Top copper pad
Plane layer connected to padstack plating with a 'thermal'
Inner copper pad
Plane layer isolated from padstack plating
Plated through-hole
Bottom copper pad
Bottom solder mask
Bottom solder paste

Figure 8-6 The elements of a padstack as used in a multilayer PCB.

Figure 8-8(a) shows how a padstack is actually displayed in Layout. When a particular layer is made active (using the **Layer** selection menu shown in Fig. 8-8(b)), the pad on that layer is brought to the front of the view, while pads on inactive layers are pushed behind. The pin number of the padstack is displayed regardless of which layer is active, and oversized pads (such as the clearance area shown in gray) can be seen sticking out past the edges of an active pad.

Obstacles

Obstacles are graphical objects (lines, arcs, etc.) placed on footprints and board layouts to show information that is not defined by padstacks (such as the outline of a part). Obstacles may be visible on the final board, or the obstacles may be visible only in the design files. Obstacles that are visible on the board include silk-screen markings (component outlines, for example), while obstacles visible only in the design files include things like board outlines, assembly outlines, and autorouter boundaries (e.g., keep-out areas where traces and components are not allowed).

There are 15 types of obstacles that can be used in Layout, but usually only 3 or 4 types are used when making footprints (i.e., detail obstacles, place outlines, insertion outlines, and occasionally copper areas). Detail obstacles are usually used to indicate silk-screen markings that will be visible on the board and on assembly layers to provide information during assembly. Place outlines are used by Layout's autoplacement and DRC utility to maintain required distance between parts while laying out the board. An insertion outline can be added around a

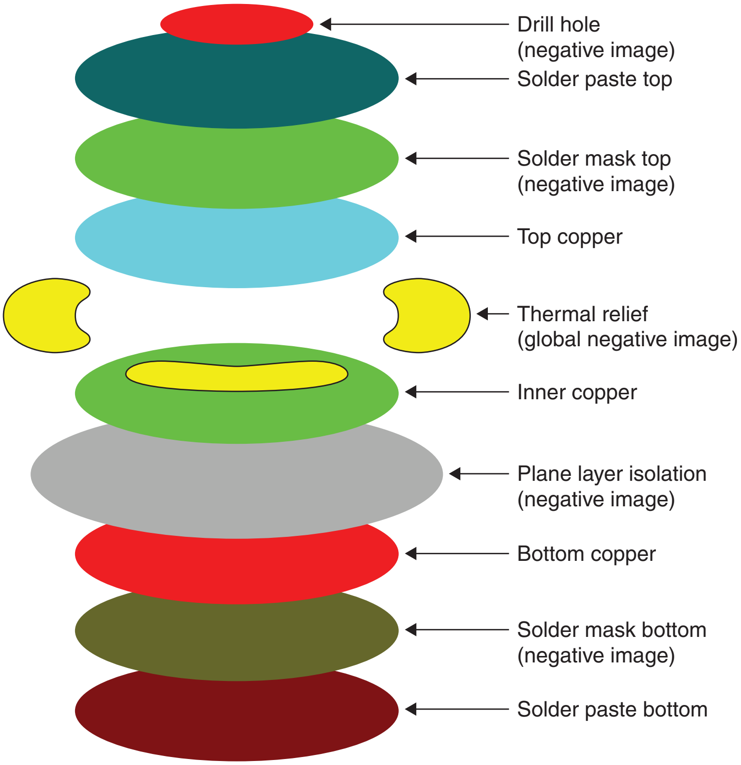

Drill hole
(negative image)
Solder paste top
Solder mask top
(negative image)
Top copper
Thermal relief
(global negative image)
Inner copper
Plane layer isolation
(negative image)
Bottom copper
Solder mask bottom
(negative image)
Solder paste bottom

Figure 8-7 Layout's "virtual" padstack.

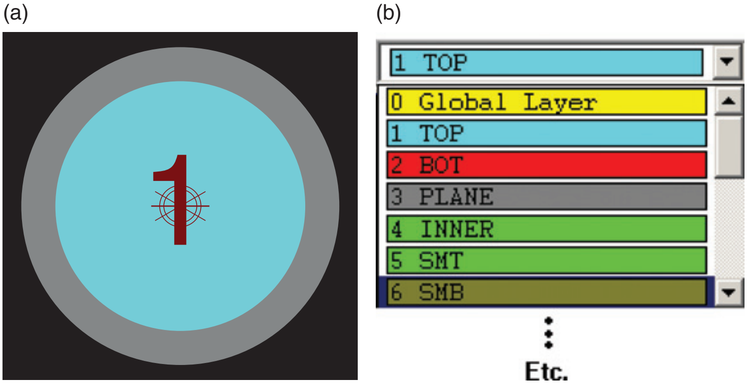

(a)
1
(b)
1 TOP
0 Global Layer
1 TOP
2 BOT
3 PLANE
4 INNER
5 SMT
6 SMB
Etc.

Figure 8-8 A Layout padstack (a) as displayed in a footprint and (b) as displayed in the layer selection list.

component to provide a safe clearance for that the component so that it is not hit by the head of automated insertion equipment when adjacent components are being placed on the board. On routing layers, copper areas can be used as heat spreaders or mini-ground planes for components that require them, and on plane layers copper areas are used to remove copper, since plane layers are negative images. Examples of how to use these obstacles are given in Chap. 9. If you want to read more about the others and what they are used for, you can also go to the Layout online help and search for “detail” (not “obstacle” as you might think), or go to Chap. 5 of the *Layout User’s Guide.*

Text

Like obstacles, text objects can be visible on a PCB or visible only within the design files. Text objects on PCBs are often part of the silk screen and may be used for such purposes as component reference designators and displaying board serial numbers or design revisions. Text that is visible only in the design files might be placed on one of the assembly or documentation layers to show board dimensions or special manufacturing instructions.

Five types of text objects are automatically generated when you make a new footprint (see Fig. 8-11). The first is text that displays the component reference designator (&COMP), which is placed on a silk-screen layer and is visible on the PCB. The remaining four text objects are on the assembly layer and are visible only in the design files; these text objects are the footprint name; component package (&PACK), if one is assigned; component value (&VALUE); and another reference designator (&COMP).

Datums and insertion origins

There is a board datum and a footprint datum. The board datum will be discussed in Chap. 9. Footprint datums are located on pin 1 by default as shown in Fig. 8-9(a). A closer look at the padstack shows that the marks consist of two types of marks—the datum point (Fig. 8-9(b)) and the insertion origin (Fig. 8-9(c)). The datum point is the local origin (0,0) of the footprint and is used as a reference from which the other pads are located. The datum can be changed to any location on the place grid, but the default and normal location for the datum is pin 1.

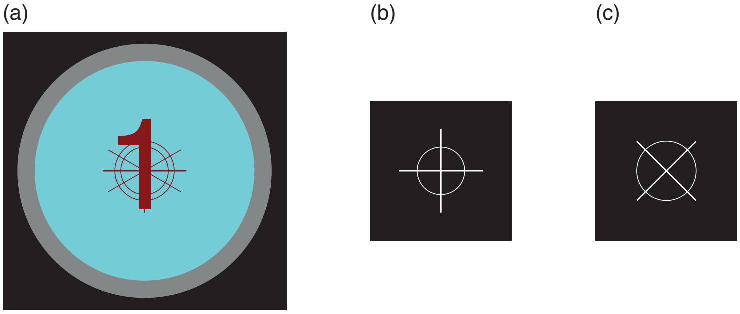


Figure 8-9 Orientation and center marks on Pad 1. (a) Default pad. (b) Datum point. (c) Insertion origin.

The insertion origin defines the location of the part. It is used as a “handle” in the insertion report for the autoplacement utility (Layout Plus only) and in assembly Gerber files for pick-and-place machines during board assembly. The default location for the insertion point is also pin 1, but it may be (and often is) moved to the geometric center of the footprint with respect to the pads. This is demonstrated in the surface-mount design example below.

The Basic Footprint Design Process

Before we go into more detail we will go through a quick footprint design example so that you can see the overall process. The design process is:

1. Start Layout and open the Library Manager from the session frame’s Tools menu.
2. Start a new footprint using a footprint template.
3. Copy the default padstack provided by the template and paste new ones in the desired locations.
4. Add obstacles for the body outline on the silk-screen layers, etc.
5. Save the new footprint.

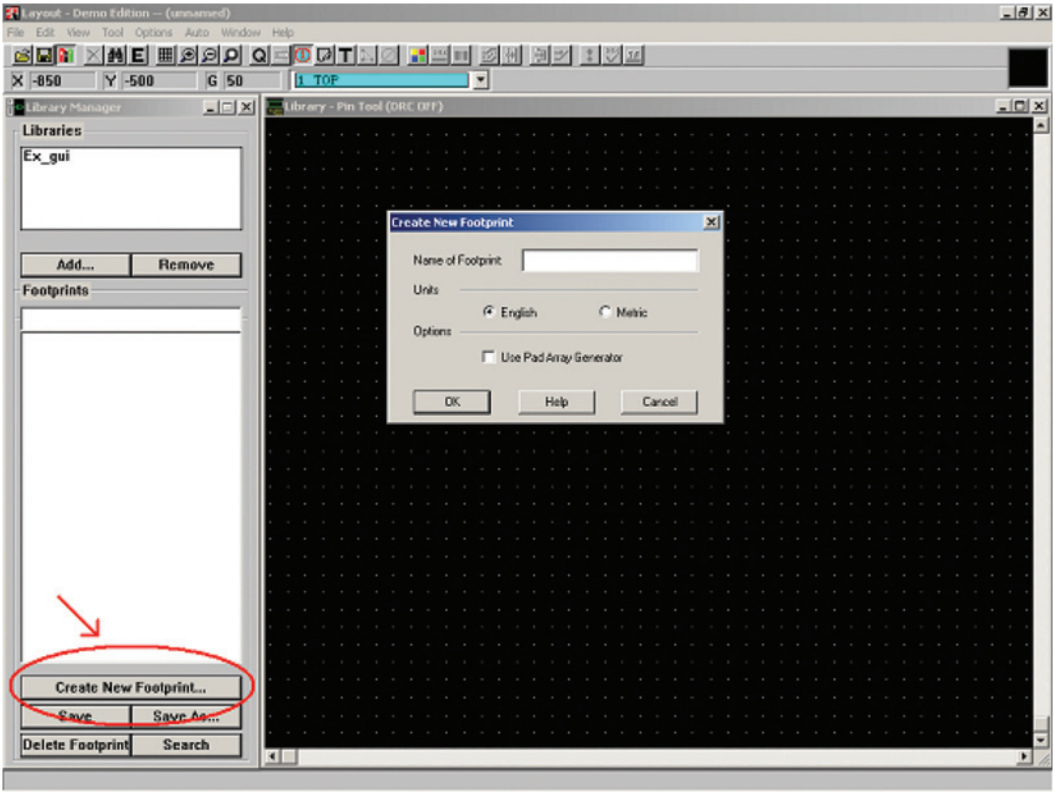
To begin a new footprint, start Layout and from the main session window select Library Manager from the Tools menu. Click the Create New Footprint button at the bottom left of the Library Manager to display the Create Footprint dialog box as shown in Fig. 8-10.

Enter a name (for example AXIAL-0) for the new footprint and click OK. You will start with the footprint template as shown in Fig. 8-11, which consists of one padstack (pin 1), five text objects, and the datum and insertion markers on pin 1.

The white text object is the component reference designator that will ultimately show up on the PCB silk screen. When a part uses this footprint, Layout uses the ampersand (&) to automatically place the component’s reference designator from the schematic (e.g., R1 or U23) on the board in place of the &Comp place holder. The same is true for the &Value and &Pack text objects, except that they are only on the assembly layer(s) and will not be visible on the silk screen. You can view text object properties by selecting the text spreadsheet, which you invoke by clicking the spreadsheets tool button, ▦ and selecting Text from the pop-up. An example of a text spreadsheet is shown in Fig. 8-12.

The next step is to add a second padstack to the footprint. Make the Pin Selection tool, ① active and select the default padstack by holding down the Ctrl button on your keyboard and left clicking once. Copy it by right clicking and selecting Copy from the pop-up. A new padstack will be attached to your pointer. Use the X-Y coordinates indicator at the bottom left corner of the Library Manager and move the pointer over 300 mils or so and left click your mouse to place the padstack.

The next step is to place a component outline obstacle (called a detail) on the silk-screen layer. Activate the top silk-screen layer by selecting 9 SST from the layer selection dropdown


Layout - Demo Edition -- (unnamed)
File Edit View Tool Options Auto Window Help
X -850 Y -500 G 50
1 TOP
Library Manager
Libraries
Ex_gui
Add...
Remove
Footprints
Create New Footprint...
Save
Save As...
Delete Footprint
Search
Library - Pin Tool (DRC OFF)
Create New Footprint
OK
Help
Cancel

Name of Footprint

Units

● English ○ Metric

Options

☐ Use Pad Array Generator

Figure 8-10 Starting a new footprint from the Library Manager.

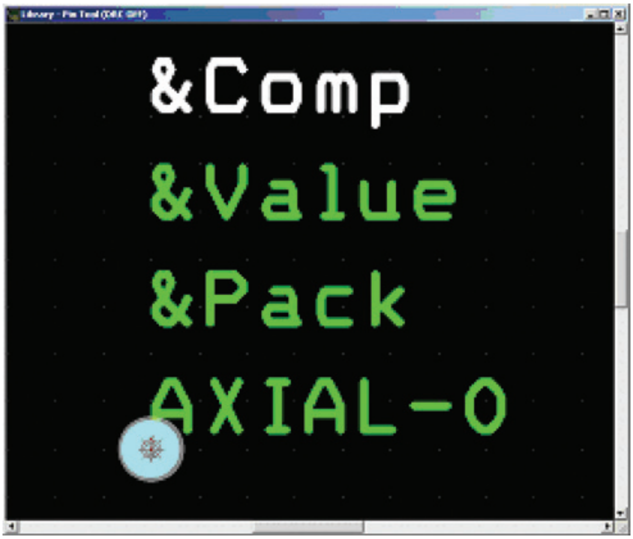
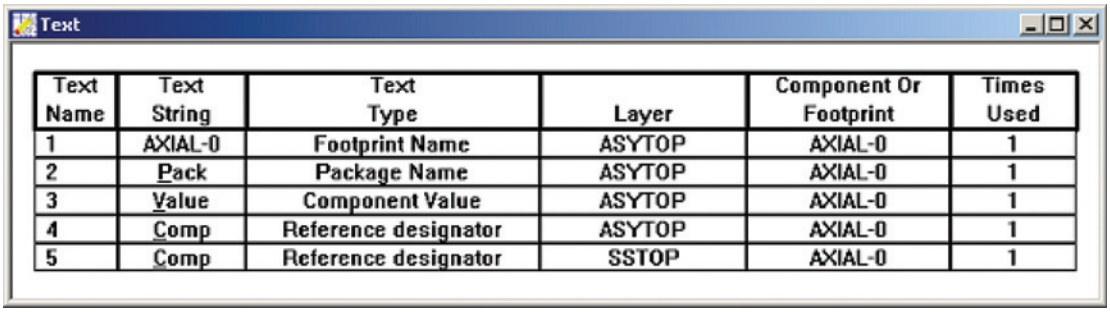

Library - Pin Tool (DRC OFF)
&Comp
&Value
&Pack
AXIAL-0

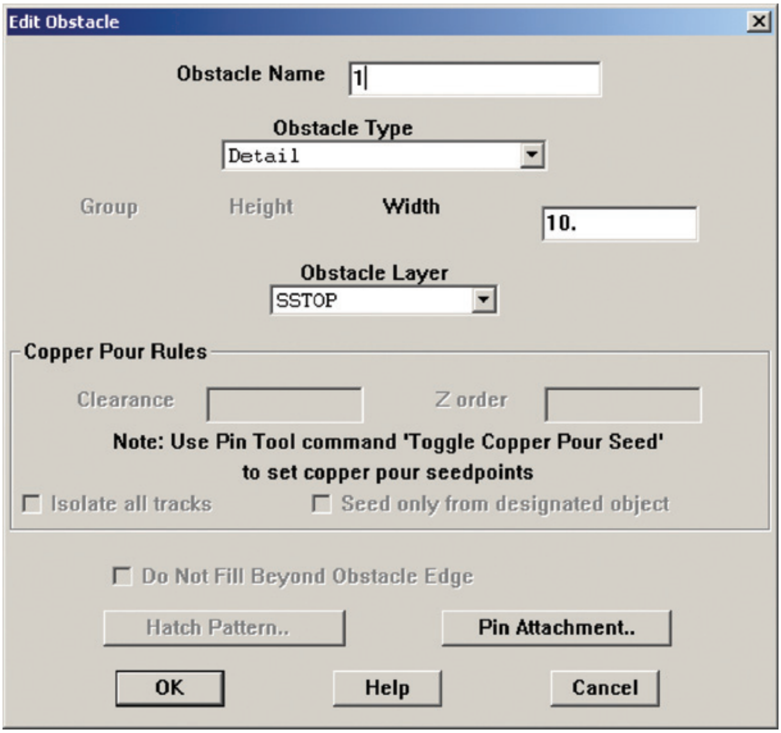
Figure 8-11 Starting a new footprint with the template.



Text Name	Text String	Text Type	Layer	Component Or Footprint	Times Used
1	AXIAL-0	Footprint Name	ASYTOP	AXIAL-0	1
2	Pack	Package Name	ASYTOP	AXIAL-0	1
3	Value	Component Value	ASYTOP	AXIAL-0	1
4	Comp	Reference designator	ASYTOP	AXIAL-0	1
5	Comp	Reference designator	SSTOP	AXIAL-0	1

Figure 8-12 ***Text*** *spreadsheet.*

menu (see Fig. 8-8). Select the Obstacle tool by toggling the ✎ button on the toolbar. Right click anywhere in the editing workspace and click **New** from the pop-up. Right click again and select **Properties** from the pop-up. The **Edit Obstacle** dialog box will be displayed as shown in Fig. 8-13. Select **Detail** from the **Obstacle Type** dropdown list. Make sure that SSTOP is selected in the **Obstacle Layer** dropdown list. Click **OK.**


Edit Obstacle
Group
Height
Copper Pour Rules
Clearance
Z order
Hatch Pattern..
Pin Attachment..
OK
Help
Cancel

Obstacle Name: 1

Obstacle Type: Detail

Width: 10.

Obstacle Layer: SSTOP

Note: Use Pin Tool command 'Toggle Copper Pour Seed' to set copper pour seedpoints

☐ Isolate all tracks ☐ Seed only from designated object

☐ Do Not Fill Beyond Obstacle Edge

Figure 8-13 The ***Edit Obstacle*** *dialog box.*

Make the box centered between the padstacks and add lead lines as shown in Fig. 8-14. Begin the box by left clicking and holding the mouse at one of the corners of the outline, drag a box to the opposite corner, and release the mouse button. To draw the lead lines right click anywhere in the editing workspace and click New from the pop-up again. Right click and select Properties from the pop-up again. Again, set up the Edit Obstacle dialog box as shown in Fig. 8-13. To draw a segment left click and release the mouse button to place the first endpoint, move the mouse to the second endpoint, and then left click and release, right click, and select End Command from the pop-up to stop the tool.

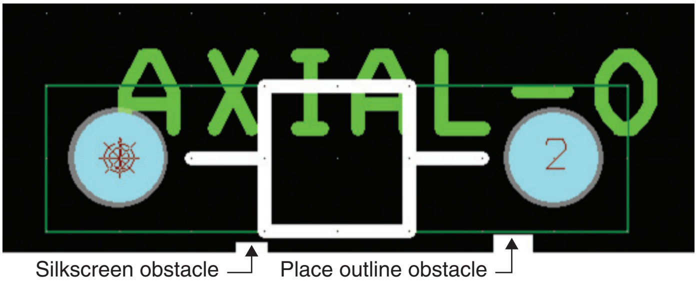


*Figure 8-14 New footprint with numbered padstacks (with orientation marks on pin 1), **Silkscreen** and **Place Outline** obstacles, and text.*

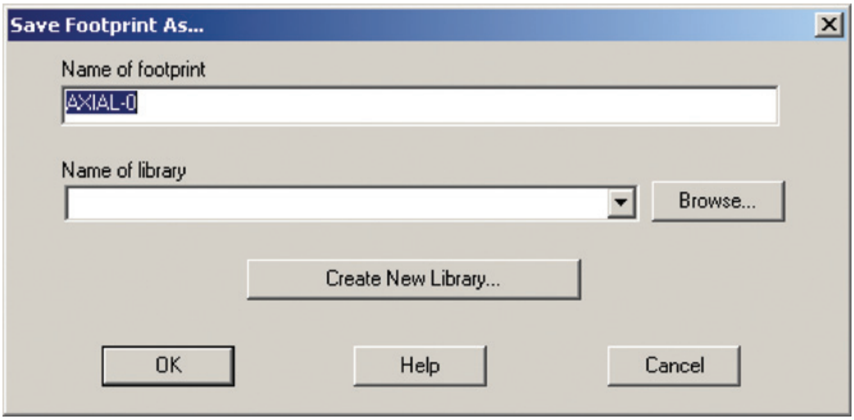
Note

- *Instead of dragging a box to create a closed polygon (particularly if it is an irregularly shaped one) you can left click and release at each vertex to define the sides of the polygon, then right click, and select **Finish** from the pop-up to close the polygon. If you select **End Command** instead, the obstacle will not be a closed polygon but a series of segments.*

Next, place a component outline obstacle on the top assembly layer. Select 11 AST from the Layer selection dropdown list (see Fig. 8-8). You can either follow the same procedure that you used to make the component outline on the silk-screen layer, or you can simply paste copies of the obstacles from the silk-screen layer to the assembly layer. To perform the latter, select (Ctrl + left click) the component outline obstacle on the silk-screen layer, right click, and select Copy, then paste the copy in a convenient place in the work area (right click and Paste or hit the Insert key on your keyboard). Select the pasted object(s) (using Ctrl + left click), then right click, and select Properties from the pop-up to change the layer properties using the Edit Obstacle dialog box (see Fig. 8-13). Change the Obstacle Layer selection list to ASYTOP. After you have changed the obstacles to the top assembly layer, select the pasted objects (Ctrl + left click), then left click, and hold to move them to the same location as the silk-screen obstacles. Remember to use the End Command after you move the pieces so that they stay where you put them.

Finally, make a place outline obstacle around the silk-screen obstacles and the padstacks as shown in Fig. 8-14. Use the procedures described above, except make the obstacle a Place Outline obstacle and place it on the Global layer.

Save the new footprint in a new library called UserLib.LLB (for example). **To save a footprint**, click the Save As... button on the Library Manager to bring up the dialog box as shown in Fig. 8-15. From here you can save the footprint in an existing library by using the Browse... button or create a new, custom library. To save the footprint in a new library, press the Create New Library... button and, from the Windows Save As... box, navigate to the C:\OrCAD\OrCAD_10.5Demo\tools\Layout\library folder (if you are using the Demo version). Type the new library name in the File Name: text box and click Save.



Name of footprint: AXIAL-0

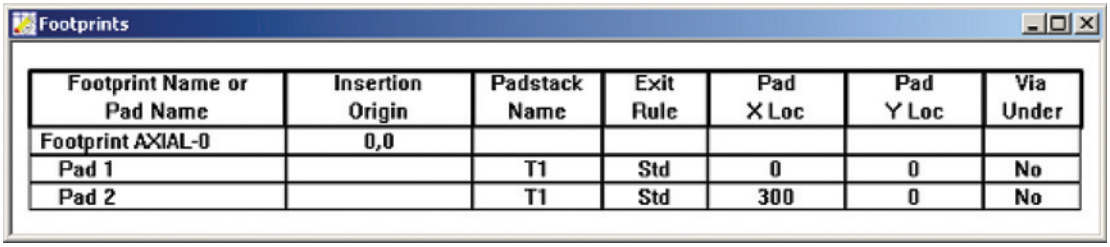
Name of library:

Figure 8-15 The ***Save Footprint As...*** *dialog box.*

If you ever need to look at the overall characteristics of a footprint you can use the Footprints spreadsheet as shown in Fig. 8-16. **To display the Footprints spreadsheet**, click the View Spreadsheet button, ▦ and select Footprints from the pop-up. From the spreadsheet you can get an overall summary of the footprint. You can change any of the parameters listed by right clicking any of the cells and selecting Properties from the pop-up menu.

Note

- *If you have messed around with footprints/pads before, you might recall seeing footprint names like R_AX.400_REV1 or a padstack name such as T1_1 show up somehow. Layout assigns a default name to a padstack when you edit footprints or padstacks without saving them with a new name to differentiate it from the original.*



Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint AXIAL-0	0,0					
Pad 1		T1	Std	0	0	No
Pad 2		T1	Std	300	0	No

*Figure 8-16 The **Footprints** spreadsheet.*

Those are the basics of making a footprint. In the example above, a default padstack was used. You will see in the examples below that most of the work involved with footprints is in dealing with the padstacks. The following sections will demonstrate how to assign existing padstacks to footprints and how to make new padstacks if the ones you need do not exist.

Working with Padstacks

There are two basic kinds of padstacks: through-hole padstacks (for leaded components and vias) and surface-mount pads. Through-holes are made using padstacks that allow connections from any one layer to any other layer (as in Fig. 8-6). Surface-mount pads are isolated from all layers except for the top layer and therefore do not use drilled and plated holes. Surface-mount pads may be on the top or bottom layer (or both in the case of edge connector footprints). Connecting a surface-mount pad to another layer is accomplished using a special padstack called a fanout (also called a stringer pad). A fanout is not part of the footprint; it is added to a PCB when placing parts and routing traces. You will see how to do this in Chap. 9.

Layout provides seven padstack templates for through-hole padstacks; they are labeled T1 through T7. All other padstacks (including surface-mount pads) are derived from these templates. The templates can be separated into four basic padstack families: **IC pads** (T1 and T2), **discrete pads** (T3 and T4), **connector pads** (T5 and T6), and a single padstack type (T7) for **fanouts and vias**. The odd-numbered padstacks are round, and the even-numbered ones are square. The templates are not directly accessible to the user, but Layout provides a means of saving and editing *copies* of them through special dialog boxes and spreadsheets that we will look at shortly. Any new or modified padstacks are either saved in a public padstack library (padstack.llb, which is not included with the Demo version) or become local entities of a footprint and are saved with the footprint. For additional information about the padstack templates, please see “Defining Padstacks” in Chap. 4 of the *Layout User’s Guide.*

Through-hole padstacks are often named by their shape and size. There are eight different pad shapes in Layout: round, square, oval, annular, oblong, rectangle, thermal relief, and undefined. One padstack naming convention used in Layout is “DRd,” where D is the outer diameter, R is the shape (R for round, S for square, etc.), and d is the inner diameter—the drill size (see Fig. 8-17). For example, if the outer dimension of a round pad is 62 mils (0.062 in.) and the drill hole is 25 mils, the pad name would be 62R25. The copper ring around the hole

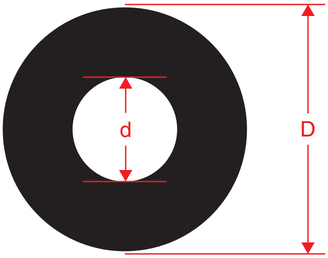


Figure 8-17 Inner and outer pad diameters.

is called the annular ring. The padstack.llb library contains many through-hole padstacks, but it does not contain surface-mount pads.

Accessing existing padstacks

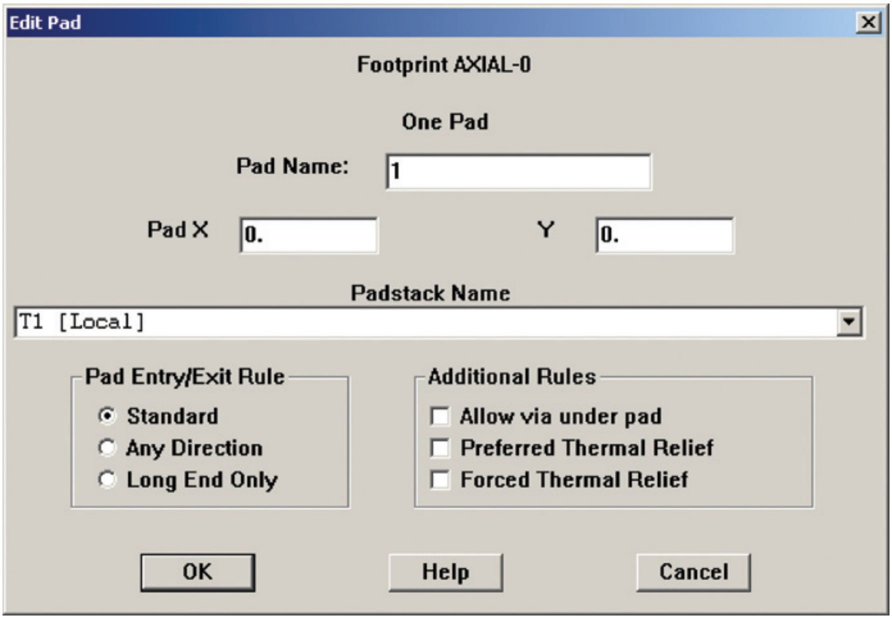
Padstack definitions can exist in three places: in a library (usually the padstack.llb), as local entities in saved footprints, or as local entities in a specific board layout (in a .MAX file). The padstack.llb is not included with the Demo version, so all padstacks are local entities that are contained within their respective footprints. There is no padstack manager (in either the Demo or the full version) as there is a library manager for footprints, so you cannot “open” a padstack and look at it the same way you can open a footprint with the Library Manager. However, using the Library Manager, you can access padstacks indirectly.

There are two ways to access padstacks using the Library Manager. The method you will use depends on what you are trying to do. You use the Edit Pad dialog box to replace one padstack with a preexisting padstack, and you use the Padstacks spreadsheet to make a new padstack or make detailed modifications to existing padstacks. With either method, you must first have the Library Manager open, and you need to have a footprint open in the Library—Pin Tool window. Instructions on how to display the two tools are given immediately below. Detailed instructions on how to use them are provided later in the design example.

The Edit Pad dialog box is shown in Fig. 8-18. **To display the Edit Pad dialog box:**

1. Activate the pin tool. ①
2. Select one of the padstacks displayed on the footprint in the Library—Pin Tool window by holding down the Ctrl key on your keyboard and left clicking on the padstack.
3. Right click with your mouse and select Properties from the pop-up menu.
4. The Edit Pad dialog box shown in Fig. 8-18 will be displayed.

The Edit Pad dialog box is used to replace the selected padstack with one of the padstacks that is displayed in the Padstack Name dropdown list. The only padstacks that are displayed in the list are ones that reside in the padstack library (if available), local copies of one of the seven template padstacks (T1–T7), and the local padstacks residing on the footprint that you



Edit Pad

Footprint AXIAL-0

One Pad

Pad Name: 1

Pad X 0. Y 0.

Padstack Name

T1 [Local]

Pad Entry/Exit Rule

● Standard
○ Any Direction
○ Long End Only

Additional Rules

☐ Allow via under pad
☐ Preferred Thermal Relief
☐ Forced Thermal Relief

*Figure 8-18 The **Edit Pad** dialog box.*

currently have open. The Edit Pad dialog box also allows you to specify certain board level parameters, such as how traces are allowed to enter or exit the pad, when routing a board.

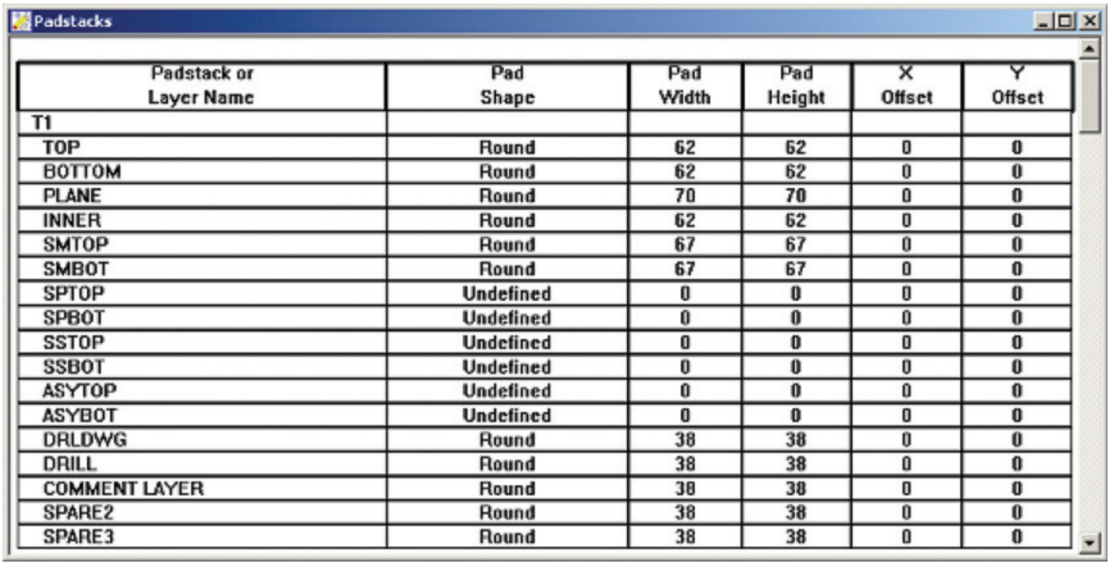
The Padstacks spreadsheet is shown in Fig. 8-19. **To display the Padstacks spreadsheet:**

1. With a footprint displayed in the editing window as described above, select the spreadsheet button, on the tool bar.
2. Select Padstacks from the menu.
3. A spreadsheet similar to the one shown in Fig. 8-19 will be displayed.

The padstacks that are included in the Padstacks spreadsheet are limited to the seven template padstacks and the padstacks of the footprint you have open. The Padstacks spreadsheet is used to make detailed changes to a padstack; it can be used to make new padstacks; and it can be used to save a padstack to a library (either the padstack library or any other library you chose). If you save a padstack to a library, it will become a public entity and will be visible in the Padstack Name selection list from within any board layout whenever the Edit Pad dialog box (see Fig. 8-18) is displayed.

Editing padstack properties from the spreadsheet

You can use the Padstacks spreadsheet to modify any aspect of any part of a padstack including the size or shape of any pad on any layer. You can make global changes to the entire



Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
T1					
TOP	Round	62	62	0	0
BOTTOM	Round	62	62	0	0
PLANE	Round	70	70	0	0
INNER	Round	62	62	0	0
SMTOP	Round	67	67	0	0
SMBOT	Round	67	67	0	0
SPTOP	Undefined	0	0	0	0
SPBOT	Undefined	0	0	0	0
SSTOP	Undefined	0	0	0	0
SSBOT	Undefined	0	0	0	0
ASYTOP	Undefined	0	0	0	0
ASYBOT	Undefined	0	0	0	0
DRLDWG	Round	38	38	0	0
DRILL	Round	38	38	0	0
COMMENT LAYER	Round	38	38	0	0
SPARE2	Round	38	38	0	0
SPARE3	Round	38	38	0	0

*Figure 8-19 The **Padstacks** spreadsheet.*

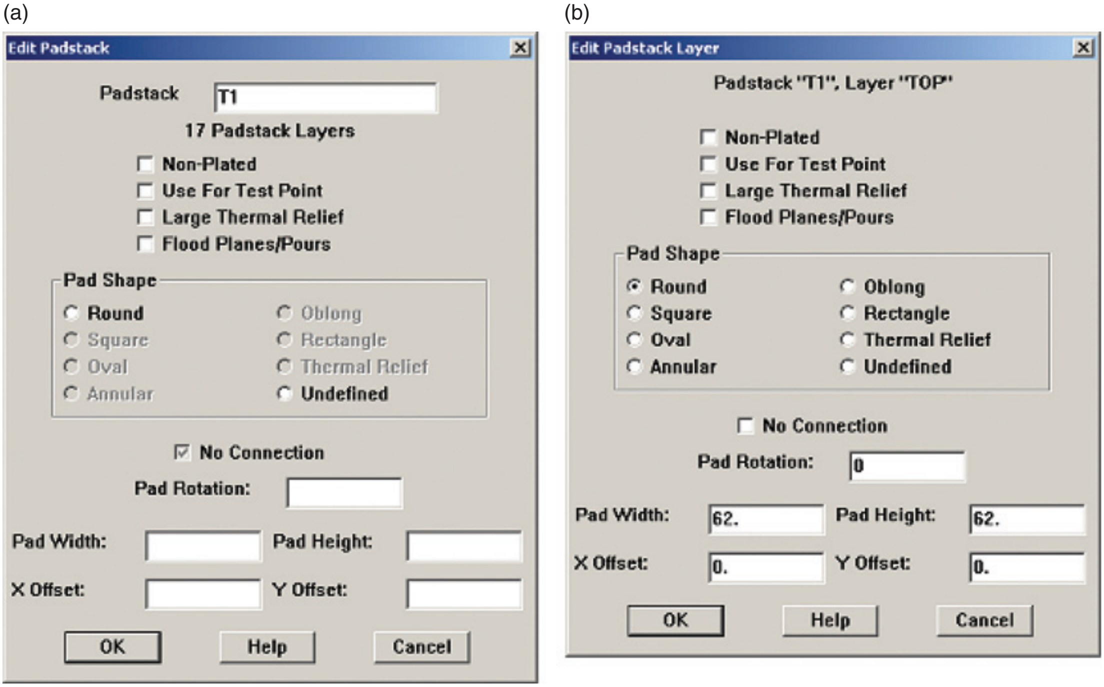
padstack, you can make changes that are limited to a single layer, or you can make changes that are limited to a particular cell.

To see how, display the Padstacks spreadsheet using the View Spreadsheets button. **To make global changes to a padstack**, select the entire padstack (e.g., T1) by clicking with the left mouse button on the cell with the padstack's name. Then right click on that cell and select Properties from the pop-up menu to display the Edit Padstack dialog box shown in Fig. 8-20(a). Any changes you make to the padstack from this dialog box will apply to all the layers of the padstack. From this dialog box you can also **change the name of a padstack.**

To edit a pad on a single layer, select the layer (row) on the spreadsheet by clicking on the layer name with the left mouse button. Then right click and select Properties from the pop-up to display the Edit Padstack Layer dialog box shown in Fig. 8-20(b). Any changes you make with this dialog box will be limited to the selected layer. You can also select a single cell on a layer and bring up an Edit Padstack Layer dialog box for just that cell. You can see from Figs. 8-20(a) and 8-20(b) that certain selections are not available depending on which selection method was used. In the design example below we will make a custom footprint with custom padstacks and obstacles, so you will see how and when to use each of the tools discussed so far.

Saving footprints and padstacks

After you make a new *footprint* or modify an existing one, there are three ways to save the footprint. You can save a footprint to a new library; you can save a footprint to an existing



(a)

Edit Padstack

Padstack: T1

17 Padstack Layers

☐ Non-Plated
☐ Use For Test Point
☐ Large Thermal Relief
☐ Flood Planes/Pours

Pad Shape
○ Round
○ Square
○ Oval
○ Annular
○ Oblong
○ Rectangle
○ Thermal Relief
○ Undefined

☑ No Connection

Pad Rotation:

Pad Width:

Pad Height:

X Offset:

Y Offset:

(b)

Edit Padstack Layer

Padstack "T1", Layer "TOP"

☐ Non-Plated
☐ Use For Test Point
☐ Large Thermal Relief
☐ Flood Planes/Pours

Pad Shape
● Round
○ Square
○ Oval
○ Annular
○ Oblong
○ Rectangle
○ Thermal Relief
○ Undefined

☐ No Connection

Pad Rotation: 0

Pad Width: 62.

Pad Height: 62.

X Offset: 0.

Y Offset: 0.

Figure 8-20 **Edit Padstack** dialog boxes. (a) Global layer editing. (b) Single layer editing.

library; or you can modify a footprint that has been placed on a board and save the footprint with the board.

After you make a new *padstack* or modify an existing one, there are two ways to save the padstack. You can save a padstack in a padstack library (either the default one or a user-defined one), or you can save a padstack with a footprint. If you save the padstack with a footprint, the padstack can be saved wherever the footprint is saved (i.e., to a library or a specific board) as described above. You will see how to do this in the examples below.

Where you decide to save your custom footprints and padstacks depends on your situation. One thing to consider is how often the new padstacks or footprints will be used in future designs. It is a good idea to save custom footprints to a new library to keep them separate from the footprints supplied by OrCAD and to allow you to easily find and back up your footprints to protect your work. Padstacks can be saved to a library if they will likely be used often and they are known good designs, otherwise it is a good idea to just save them with the new footprint. The reason for a conservative approach is that once you save a padstack to a library you cannot easily delete it (even the bad ones). And since there is no padstack "viewer," so to speak, the padstack library can quickly become cluttered and confusing as the library becomes larger and larger.

Footprint Design Examples

The following are simple examples of how to design padstacks and footprints for through-hole and surface-mounted devices. Once you understand these basic steps, you can apply the same principles to design new footprints or modify existing ones of any type. No matter what type of footprint you are trying to make, you can follow the design flow process shown in Fig. 8-21.

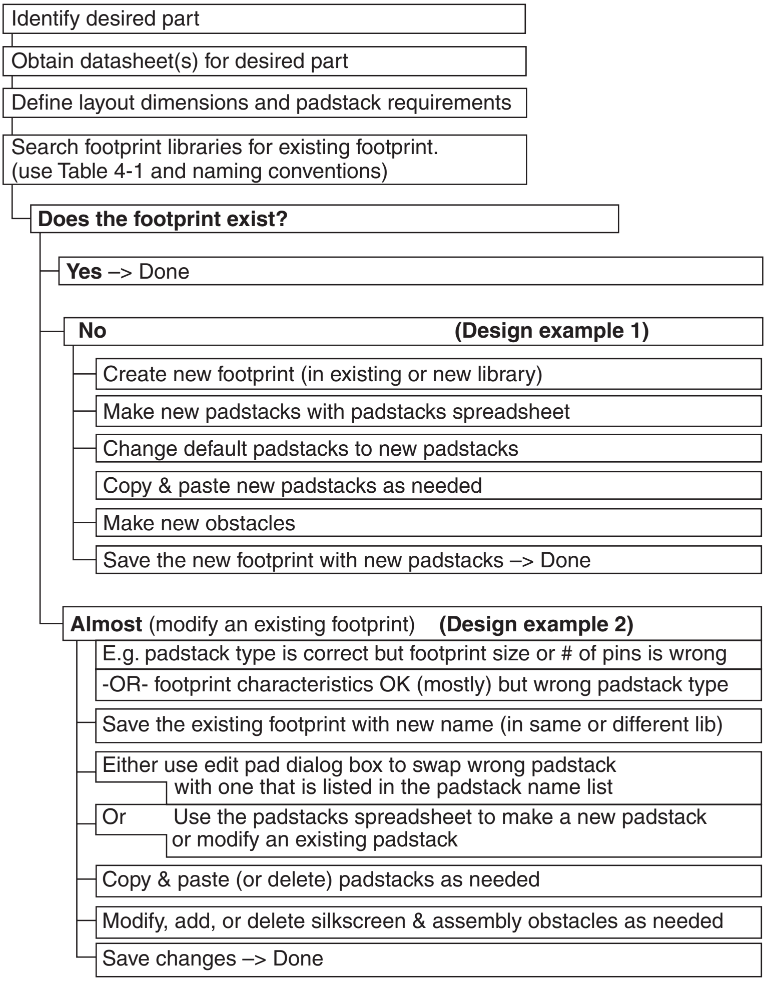

Identify desired part
Obtain datasheet(s) for desired part
Define layout dimensions and padstack requirements
Search footprint libraries for existing footprint. (use Table 4-1 and naming conventions)
Does the footprint exist?
Yes –> Done
No (Design example 1)
Create new footprint (in existing or new library)
Make new padstacks with padstacks spreadsheet
Change default padstacks to new padstacks
Copy & paste new padstacks as needed
Make new obstacles
Save the new footprint with new padstacks –> Done
Almost (modify an existing footprint) (Design example 2)
E.g. padstack type is correct but footprint size or # of pins is wrong
-OR- footprint characteristics OK (mostly) but wrong padstack type
Save the existing footprint with new name (in same or different lib)
Either use edit pad dialog box to swap wrong padstack with one that is listed in the padstack name list
Or Use the padstacks spreadsheet to make a new padstack or modify an existing padstack
Copy & paste (or delete) padstacks as needed
Modify, add, or delete silkscreen & assembly obstacles as needed
Save changes –> Done

Figure 8-21 Footprint design flow.

The design examples below demonstrate how to work with padstacks and footprints. The first design example shows how to create new padstacks and a new footprint from scratch. The second design example shows how to modify an existing footprint to meet the needs of a new part.

Design example 1: a surface-mount footprint design

The first example demonstrates how to make an SOT-523 small outline transistor package from scratch. The physical package is shown in Fig. 8-22(a) and a typical OEM suggested land pattern is shown in Fig. 8-22(b). If the manufacturer of the part does not provide a land pattern use the land pattern calculations described in Chap. 5 or use the IPC Land Pattern Viewer. Note that the OEM land pattern shown in Fig. 8-22(b) is different from the IPC suggested land pattern.

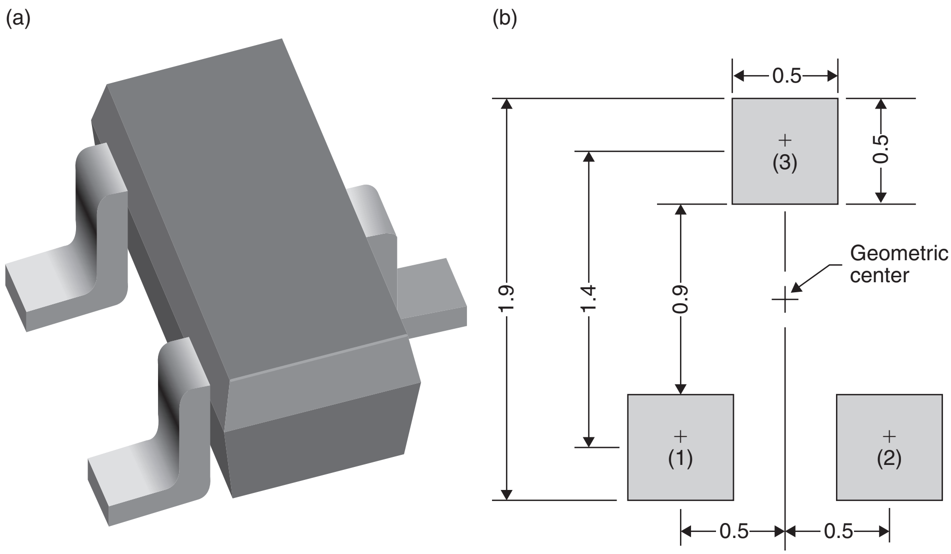
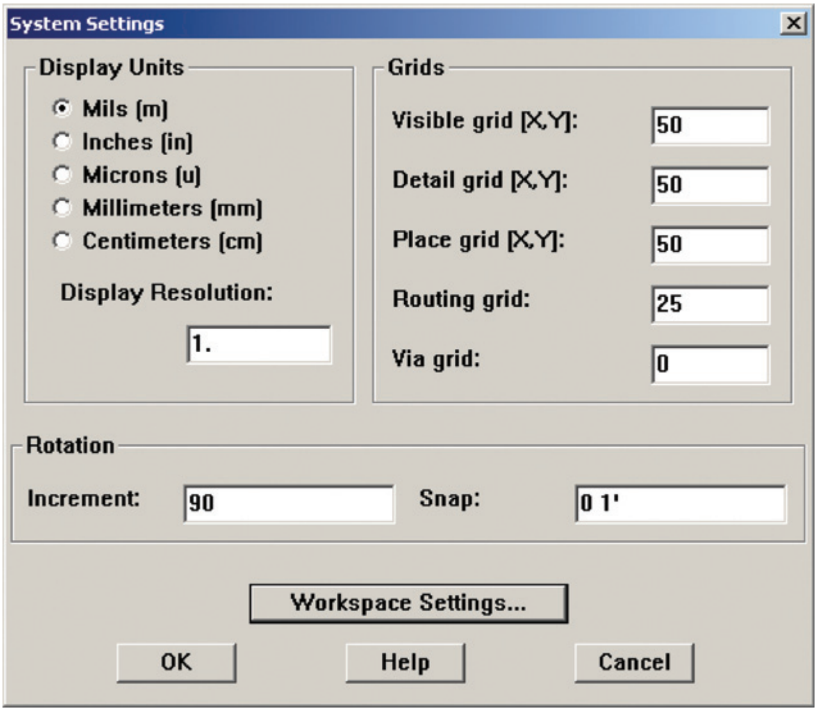


Figure 8-22 SOT-523 small outline transistor and land pattern. (a) Package. (b) Land pattern (units in mm).

Start Layout and select Library Manager from the Tools menu in the main session frame. Click the Create New Footprint button and enter SOT523_123 in the Name of Footprint: text box in the Create New Footprint dialog box. Click OK. You will again start with the default footprint template with the T1 padstack (see Fig. 8-11). From the Options menu, select System Settings (see Fig. 8-23). Select millimeters as the units. Change the visible grid and the place grid to 0.1 mm. Click OK.

To define a new surface-mount padstack open the Padstacks spreadsheet by clicking the Spreadsheets button ▦, and then select Padstacks from the pop-up (Fig. 8-24). Select the T1 padstack and then right click select New from the pop-up. A new padstack definition will be inserted at the bottom of the spreadsheet with a default name of T8 and default pad dimensions identical to those of T1. Select the



● Mils (m)
○ Inches (in)
○ Microns (u)
○ Millimeters (mm)
○ Centimeters (cm)

Display Resolution: 1.

Visible grid [X,Y]: 50
Detail grid [X,Y]: 50
Place grid [X,Y]: 50
Routing grid: 25
Via grid: 0

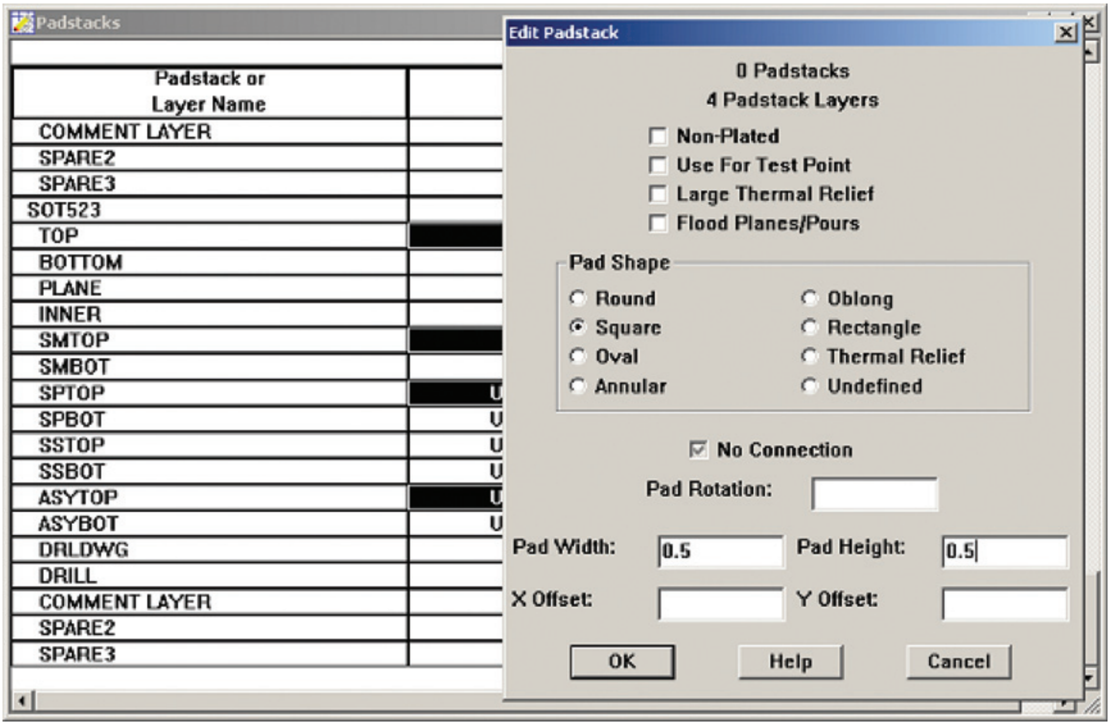
Increment: 90
Snap: 0 1'

Figure 8-23 ***System Settings*** *dialog box (from* ***Options*** *menu).*

T8 cell, right click, and select **Properties** from the pop-up. Type a name such as SOT523 or L.5xW.5 in the Padstack Name text box since all of the pads are the same size. If pad 1 was different from the others you could name it SOT523_1 or its dimension. You would then make another new pad and name it SOT523_2 or its dimension for the other pads. Click **OK.** Select the TOP row and then hold down the **Ctrl** key and select the SMTOP, SPTOP, and ASYTOP rows to select all four layers at once. Right click and select **Properties** from the pop-up. Check the radio button for a square pad and enter 0.5 in the pad width and height boxes. Click **OK.**

Note

- *This will make the soldermask openings the same size as the pads. In some cases the soldermask openings should have a clearance of 1 to 6 mils around the pad to allow for fabrication tolerances. Check the suggested land pattern dimensions specified by your board manufacturer and the manufacturer of the specific IC you are using for the proper soldermask opening size. See also IPC-7351 and Chap. 5 of this book.*



Padstack or Layer Name	
COMMENT LAYER	
SPARE2	
SPARE3	
SOT523	
TOP	■
BOTTOM	
PLANE	
INNER	
SMTOP	■
SMBOT	
SPTOP	■ U
SPBOT	U
SSTOP	U
SSBOT	U
ASYTOP	■ U
ASYBOT	U
DRLDWG	
DRILL	
COMMENT LAYER	
SPARE2	
SPARE3	

0 Padstacks
4 Padstack Layers

☐ Non-Plated
☐ Use For Test Point
☐ Large Thermal Relief
☐ Flood Planes/Pours

Pad Shape
○ Round
● Square
○ Oval
○ Annular
○ Oblong
○ Rectangle
○ Thermal Relief
○ Undefined

☑ No Connection

Pad Rotation:
Pad Width: 0.5
Pad Height: 0.5
X Offset:
Y Offset:

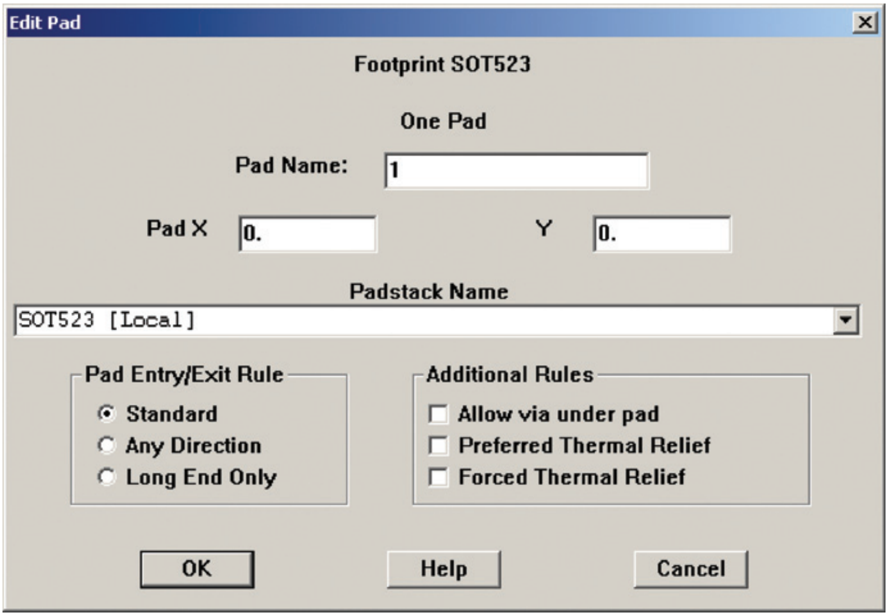
Figure 8-24 ***Padstacks*** *spreadsheet and* ***Edit*** *dialog box.*

Next select all of the other layers (BOTTOM, PLANE, INNER, SMBOT, SPBOT, SSTOP, SSBOT, and all of the drill and documentation layers). Right click and select Properties again to display the Edit Padstack dialog box for these layers. Select the Undefined radio button to disable these layers since they do not exist for a surface-mount pad.

After you have finished specifying the pad sizes, close the Padstacks spreadsheet. Select (Ctrl + left click) the default pad provided with the new footprint and then right click and select Properties from the pop-up to display the Edit Pad dialog box (Fig. 8-25). Pull down the Padstack Name list and select the SOT523 [Local] padstack you just made. Click OK. Right click and select End Command from the pop-up to complete the action. You should now have a small square pad where the large through-hole pad was.

To save the new footprint (as it is so far) click the Save button. In the Save Footprint As... dialog box you can use the SOT523_123 name you started with or give it a new name; select an existing library using the Browse... button or create a new library by clicking the Create New Library... button and choosing a name and location for the new library.

The SOT523 [Local] padstack is also saved with the footprint and exists only with this footprint. **To save the padstack to a library** (e.g., the PADSTACK library) locate the padstack in the Padstacks spreadsheet. Select the entire padstack by left clicking the cell with the



Edit Pad

Footprint SOT523

One Pad

Pad Name: 1

Pad X 0. Y 0.

Padstack Name: SOT523 [Local]

Pad Entry/Exit Rule
- ● Standard
- ○ Any Direction
- ○ Long End Only

Additional Rules
- ☐ Allow via under pad
- ☐ Preferred Thermal Relief
- ☐ Forced Thermal Relief

Figure 8-25 Assigning the new padstack.

padstack's name. Right click and select Save to Library... from the pop-up. Use the Create... or Browse... button to select the desired library.

Select the text tool button T. Move all of the text objects to an area above the padstacks so that your view of the padstack area is not obstructed. Zoom in so that the new pad fills up about ¼ of the work space and is located in the lower left corner of the work area. **To zoom in**, use the Zoom In tool 🔍, or hit the I key on your keyboard.

Select pad 1 (use Ctrl + left click) and copy it using Ctrl + C (or right click and select Copy from the pop-up). A new pad (pad 2) will be attached to the cursor. Move pad 2 to coordinate location [1.000, 0.000]. Press the Insert key on your keyboard to paste pad 2. Another pad (pad 3) will automatically be attached to the cursor. Move the cursor to coordinate [0.500, 1.400]. Paste pad 3 by pressing Ctrl + V on your keyboard (or right click and select Paste from the pop-up). Press the Esc key on the keyboard or right click and select End Command from the pop-up.

Next, make the silk screen, assembly, and place outline obstacles as shown in Fig. 8-26. First, change the detail and visible grid settings to 0.05 mm (Options → System Settings menu). **To make the component outline on the silk screen** make the silk-screen layer active and toggle the Obstacle tool. Right click in the work space and select New. Right click again and select Properties. Select Detail from the Obstacle type dropdown list, select SSTOP from the Obstacle Layer list, and enter 0.1 in the Width text box. Draw the silk-screen markings as shown in Fig. 8-26. Right click and select End Command from the pop-up when you are finished. Repeat this process for the top assembly layer.

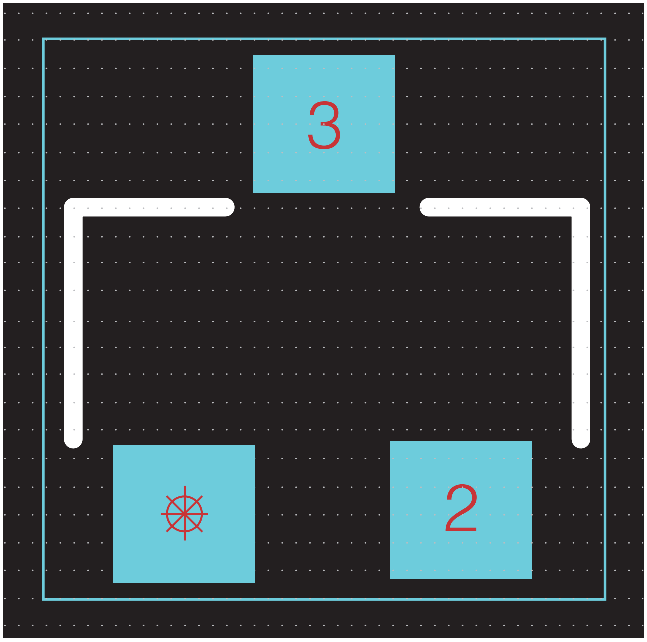


Figure 8-26 SOT-523 footprint with silk screen and place outline obstacles.

Next, draw the **place outline obstacle**. Right click in the work space and select New. Right click again and select Properties. Select Place outline from the Obstacle type dropdown list and select TOP from the Obstacle Layer list. Click OK. Draw the place outline box as shown in Fig. 8-26. If desired, you can also add an Insertion outline obstacle on the top layer using the same procedure.

Note 1

- *The place outline is set to Global for through-hole devices, but surface-mount devices can have the place outline obstacle as either Global or TOP. If you set it to TOP, then you are allowed to place other surface-mount components on the backside of the board underneath this component. Global place outline obstacles restrict other parts from being placed on any layer so that there is absolutely no overlap.*

Note 2

- *The place outline is what the DRC uses to determine if spacing rules are being followed. See Table 5-14 for spacing guidelines.*

Zoom out so that you can see the entire work space including all of the text objects. **To zoom out** press the O key on your keyboard or click the Zoom All tool, on the toolbar.

If you will primarily use this part on boards that use mils instead of millimeters use the System Settings dialog box **to change the units** back to mills and the resolution to 25 mils.

Select the Text tool and move the &Comp text objects (there are two—one on the silk-screen layer and one on the assembly layer) to below pin 1 and pin 2. This will make the reference designator closer to the component when it is placed on your PCB.

Finally, **move the insertion point to the geometric center of the footprint** outline. From the toolbar, select Tool → Dimension → Move Datum. The cross hair will become small. Do not click the left mouse button or the datum point will be moved—we want only the insertion point moved. Instead, right click and select Center Insertion Origin from the pop-up menu.

The completed SOT-523 footprint design is shown in Fig. 8-27. Save your new footprint by clicking the Save button in the lower left corner of the Library Manager.

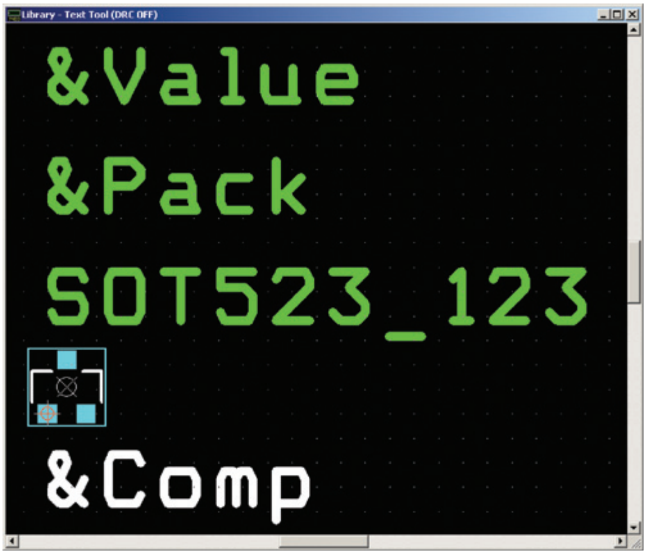


Figure 8-27 Completed SOT-523 footprint.

Design example 2: a modified through-hole footprint design

In this design example, a ¼-W, 20%, carbon film resistor will be made by modifying the simple axial footprint that was made at the beginning of this chapter. First, we will specify the padstack requirements. The diameter of a padstack is defined by the size of the drill hole plus the width of the annular ring (the copper trace around the drill hole—see Fig. 8-17). There are industry guidelines that define the sizes of the drill holes and the minimum annular ring width with respect to the size of the lead that will be soldered into the padstack (called the wire-to-hole ratio). There are also standards with respect to the bend radius of the lead, which, along with the length of the part, determines how far apart the padstacks should be placed. Chapter 5 provides guidelines and formulas for determining wire-to-hole ratios and pad diameters.

Figure 8-28 shows the dimensions of the resistor for this design example. In the simple footprint example above, default through-hole padstacks were used, and the pads were arbitrarily placed about 300 mils apart. The padstacks will need to be changed to accommodate the 25-mil-diameter leads, and the padstacks will need to be moved farther apart to accommodate the 250-mil body length and bend radius of the leads. The obstacles will also need to be resized to meet the 100-mil body width and the increased length.

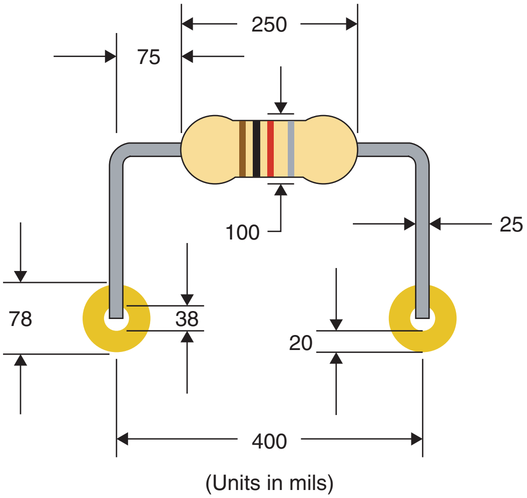


Figure 8-28 Footprint requirements for an axially leaded resistor.

Methods for "engineering" plated through-holes are described in detail in Chap. 5. For now we will keep things simple and set the drill hole for the lead to 1.5 times the diameter of the lead. The drill diameter is then $1.5 \times 25 = 38$ mils (Coombs, 42.2.2, p. 42.3). If we then decide that the annular ring should be 20 mils wide (a fairly robust annular ring), then the pad's outer diameter should be $20 + 38 + 20 = 78$ mils as shown in Fig. 8-28. The typical naming convention in Layout for a pad with these dimensions is 78R38.

A rule of thumb with regard to pad spacing (see IPC-2221A Section 8.1.11 and Chap. 5 for details) suggests that the distance from the end of the body to the center of the bent lead should be at least one lead diameter plus an allowance for the bend radius; we will use 75 mils as a conservative number in this example. The distance between the pads then will be

75 + 250 + 75 = 400 mils at the centers. The overall dimensions of the footprint then are 38-mil holes spaced 400 mils apart with a body width of 100 mils.

If we want to determine if this footprint already exists, we would search for a discrete, through-hole mounted component with axial leads. Using Table 8-1, the correct library would most likely be TM_AXIAL.LLB (**t**hrough-hole **m**ounted with **axial** leads). If you look through the TM_AXIAL.LLB library (full version only), you will find footprint AX/.400x.100/.034. This is close to what is needed, but the drill size is too small for our needs and the silk-screen obstacles are too short, so we will make a copy of this footprint, modify it, and save it with a new name. If you are using the Demo version of Layout, there are no axial footprints in the Ex_gui library so you can practice on the AXIAL-0 footprint example developed at the beginning of this chapter.

To modify a footprint, open Layout, bring up the Library Manager and open the TM_AXIAL.LLB (or your UserLibrary) and select the AX/.400x.100/.034 (or AXIAL-0) footprint. Click the Save As... button on the Library Manager. In the dialog box, enter the footprint's new name, AX/.400x.100/.038, in the Name of Footprint text box and select your UserLibrary in the Name of Library list box (use the Browse button if necessary). Click OK.

Select your UserLibrary in the Libraries pane of the Library Manager. The new AX/.400x.100/.038 footprint should be listed in the Footprints pane. Select the footprint to display it in the editing window.

The first editing task will be to make a new 78R38 padstack from the existing padstack. **To make a new padstack** select the Pin tool, ①, and select one of the footprint's padstacks (use Ctrl + left click to select the pad). Toggle the Spreadsheets button, ▦, and select Padstacks from the menu. The Padstacks spreadsheet will pop up with padstack TM_AXIAL.llb_pad1 in view (or T1 if you are using a copy of the AXIAL-0 footprint).

Note

- *You do not have to select a padstack prior to opening a Padstacks spreadsheet, but if you do not select the padstack you will have to search through the spreadsheet because the spreadsheet will display the first padstack in the spreadsheet (usually T1) by default.*

To make the new padstack based on the existing one, select the existing padstack (if not already selected), right click, and select New... from the pop-up menu. A new padstack (TM_AXIAL.llb_pad2 or T8) will automatically be generated with default properties and placed after the last padstack in the spreadsheet. Select the entire new padstack by left clicking in the cell with the padstack's name in it. All of the padstack property cells should be highlighted. Right click and select Properties from the pop-up menu to bring up the Edit Padstack dialog box. Replace the existing name with "78R38" in the Padstack Name text box. Do not do anything with any of the other options yet. Click OK to get back to the spreadsheet.

Change the pad diameters to 78 mils on the TOP, BOTTOM, INNER, SMTOP, SMBOT, ASYTOP, and ASYBOT layers. To change all of them simultaneously, select the TOP layer first, then hold the Ctrl key down and select the remaining six layers. With all seven layers selected, right click and select Properties from the pop-up. In the Edit Padstack Layer dialog box change the pad widths and heights to 78. Click OK. Make sure that the Round button is selected as well.

Note

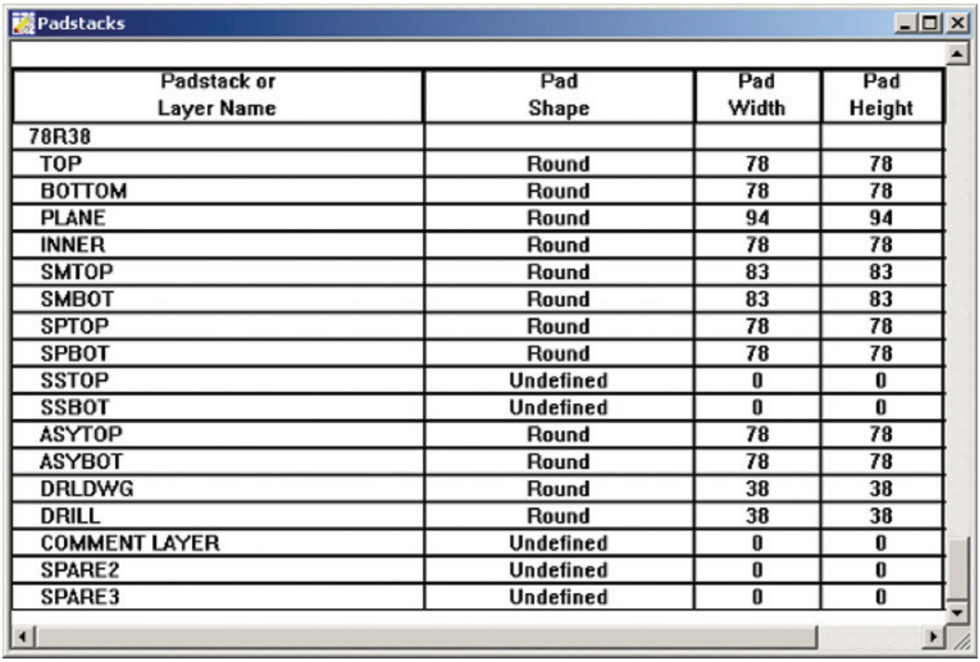
- *You could change the SMTOP and SMBOT to 83-mil-diameter openings (pad diameter + 5 mils) depending on your board manufacturer's requirements. See soldermask thumb rules and standards in Chap. 5.*

Change the drill holes on the DRLDWG and DRILL layers to 38-mil-diameter holes using the procedure just described.

The next step is to define the clearance area on the plane layers. The goals are to provide proper spacing clearance between the drill hole and the edge of the hole in the plane and to prevent any of the pads from overlapping the plane. So the diameter of the isolation area is typically 10 to 20 mils larger than the diameter of the external (TOP/BOTTOM) pads, which typically meets both requirements. (see Chap. 5 for design standards). In this example we will make the clearance 16 mils larger than the TOP pads. Select the PLANE row and change the pad width and height to 94 (78 + 16 = 94 mils) using the Edit Padstack Layer dialog box as described in the previous step. The completed padstack is shown in Fig. 8-29.

The 78R38 padstack is complete but is currently only a temporary, local padstack (i.e., if you were to close Layout without saving the footprint, 78R38 would be lost). In this example we will make the padstack a permanent, public padstack. To **save a new padstack to the Padstack library**, right click the cell in the spreadsheet with the padstack's name (78R38), right click, and select Save to Library... from the pop-up. From the Save padstacks—Select library dialog box you can save the padstack to one of the libraries in the Select Library list, save it to a new padstack library using the Create... button, or save it to any other library using the Browse button. Once you save the padstack to a library you will be able to access it easily and reuse it as long as the library you saved it to is listed in the Library Manager's library window.

Next, exchange the padstacks currently on the footprint for the 78R38 padstack you just saved. Close the Padstacks spreadsheet. **To exchange an existing padstack for a different**



Padstack or Layer Name	Pad Shape	Pad Width	Pad Height
78R38			
TOP	Round	78	78
BOTTOM	Round	78	78
PLANE	Round	94	94
INNER	Round	78	78
SMTOP	Round	83	83
SMBOT	Round	83	83
SPTOP	Round	78	78
SPBOT	Round	78	78
SSTOP	Undefined	0	0
SSBOT	Undefined	0	0
ASYTOP	Round	78	78
ASYBOT	Round	78	78
DRLDWG	Round	38	38
DRILL	Round	38	38
COMMENT LAYER	Undefined	0	0
SPARE2	Undefined	0	0
SPARE3	Undefined	0	0

Figure 8-29 Completed 78R38 padstack.

one (e.g., change pad 1 to the new 78R38 padstack), select pad 1 (Ctrl + left click), right click, and select Properties from the pop-up to display the Edit Pad dialog box. The 78R38 padstack will be listed in the Padstack Name dropdown list. Select 78R38 and click OK. Right click and select End Command from the pop-up to make the change take effect. Pin 1 is now a 78R38 padstack. Change pin 2 to 78R38 by repeating the process.

Move pin 2 to the correct location. Select pin 2 (without using the Ctrl key) and move it so that it is 400 mils to the right of pin 1. Use the X-Y coordinates indicator at the bottom left corner of the Library Manager to locate the point and left click to place the padstack.

The next step is to resize and move the component outline obstacles on the silk screen and assembly layers and the outline obstacle on the Global layer. Resizing and moving obstacles has a different “feel” to it compared to making new ones. **To move an obstacle**, select it by either pressing the Ctrl key while you click and release the obstacle with the left mouse button or pressing and holding the left mouse button while you drag a box across part of the obstacle. Once you select it, click and hold the obstacle with the left mouse button to grab and move the obstacle. Continue holding the left mouse button until the obstacle is located where you want it. Release the mouse button and deselect it by right clicking and selecting End command from the pop-up or by hitting the Esc key on your keyboard.

To resize a closed obstacle, you cannot grab the vertices by clicking on them. You have to grab a side next to the vertex you want to move. Which side to grab is determined by which vertex you are trying to move and in which direction you want to move it. Figure 8-30 shows the relationship. For all vertices except the first one that was placed (i.e., the start point) grab the vertical side next to the vertex to move the vertex horizontally (i.e., left or right). To move a vertex vertically (up or down), grab the horizontal side next to the vertex. In contrast, to move an object's start point horizontally (left or right) you have to grab the horizontal side next to the vertex, and if you want to move the start point vertically you have to grab the vertical side.

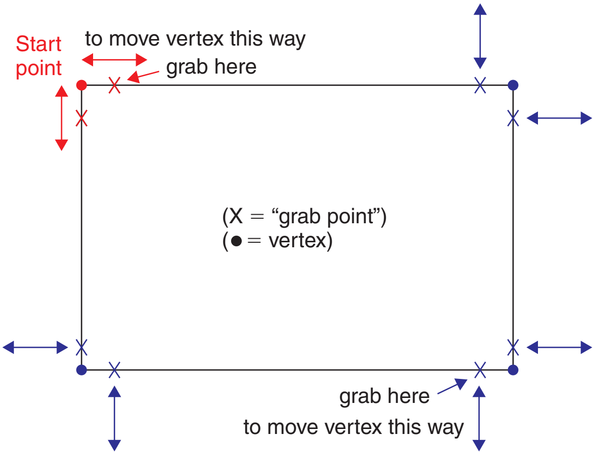


Figure 8-30 Grab locations for resizing obstacles.

You cannot tell which vertex was the starting point vertex by looking at it. The only way to find out is to pick a corner and try to move it. You have a 75% chance of selecting a vertex that moves "normally." If it seems to behave strangely then you found the starting point vertex. Hit the Esc key and grab the side adjacent to the one you just grabbed. If you grab a side in the middle, it will "snap" and you will insert another vertex where you grabbed it (more or less).

Next, modify the silk screen, assembly, and place outline layers to look like the final footprint as shown in Fig. 8-31. The silk screen and assembly component outlines should be 100 × 250 mils and centered between the padstacks. The place outline should be 110 × 500 mils to allow the padstacks and all other obstacles to reside completely inside the place outline. You will need to change the visible and detail grid settings to 5 mils to accomplish this. A note on place outline obstacles: If you use a round place outline obstacle instead of a square one (e.g. for a radially leaded electrolytic capacitor) the DRC will approximate the area as if it were a square and generate pad spacing errors if you place other components where the corners would be even when the place outlines are not touching.

You can review the final resistor design using the Footprints spreadsheet view as shown in Fig. 8-32, which shows the new footprint name and the new padstacks you designed. Once

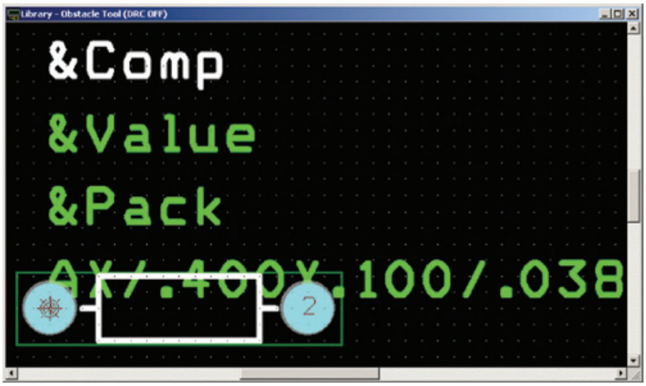
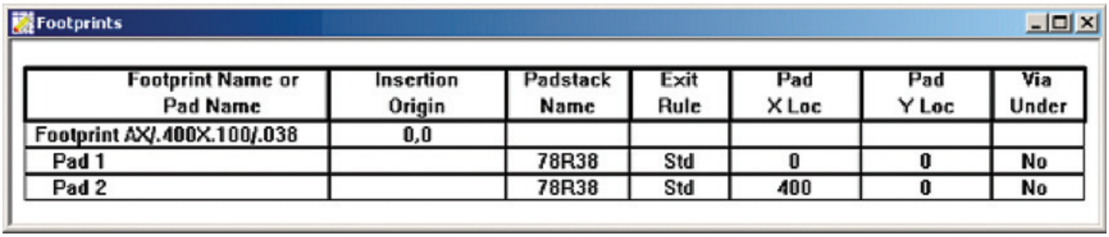


Figure 8-31 Final modified through-hole resistor footprint.



Footprint Name or Pad Name	Insertion Origin	Padstack Name	Exit Rule	Pad X Loc	Pad Y Loc	Via Under
Footprint AX/.400X.100/.038	0,0					
Pad 1		78R38	Std	0	0	No
Pad 2		78R38	Std	400	0	No

Figure 8-32 Final resistor footprint design.

it passes final inspection, save the new footprint by clicking the **Save** button on the Library Manager.

Using the Pad Array Generator

Introduction

The pad array generator is used to construct footprints for high-density pin packages such as pin grid arrays (shown in Fig. 8-33) and ball grid arrays. PGAs and BGAs are used for ICs that have large numbers of input and output ports such as field programmable gate arrays (FPGAs), memory chips, and microprocessors (CPUs), These types of ICs can have 1000 or more pins. In addition to ICs, the pad array generator can be used to make footprints for PCB mounted connectors. Making footprints with a large number of pins is made easier with the pad array generator because much of the work is done for you. The next two examples will demonstrate how to use the pad array generator to construct footprints for through-hole and surface-mounted devices.

Footprint design for PGAs

The pad array generator will be used in this first example to construct a footprint for the PGA shown in Fig. 8-33. The first step is to obtain a data sheet for the part. The dimensions for a

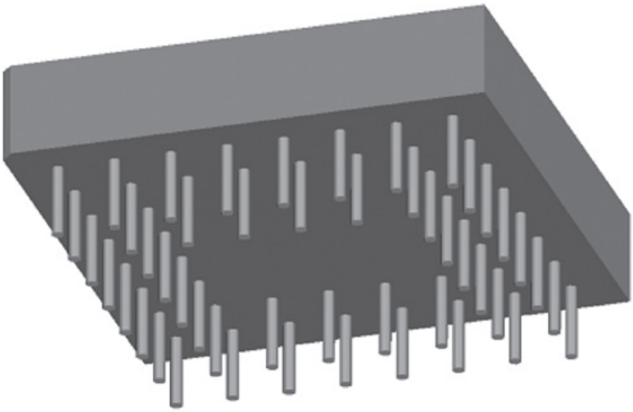


Figure 8-33 Bottom view of 48-pin, 8 × 8 pin grid array.

generic 48-pin, 8 × 8 PGA are shown in Fig. 8-34(a). Each pin has a 22-mil diameter and is spaced 100 mils from the others. A padstack with a 34-mil hole and 54-mil-diameter pads will suffice for the 22-mil pin (Fig. 8-34(b)).

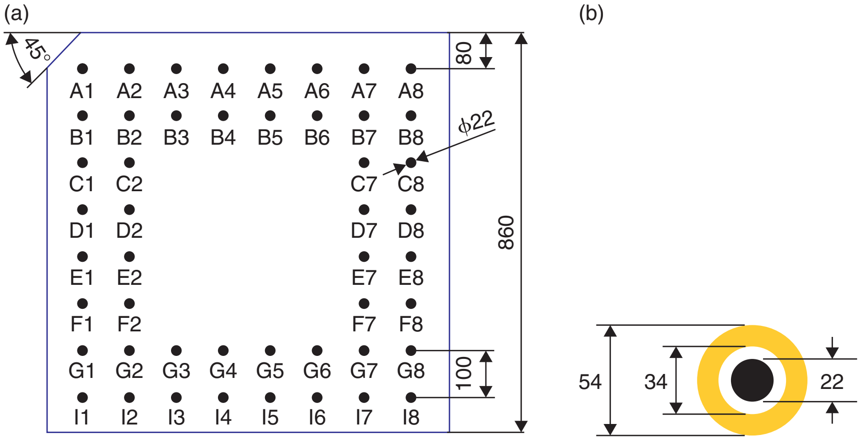
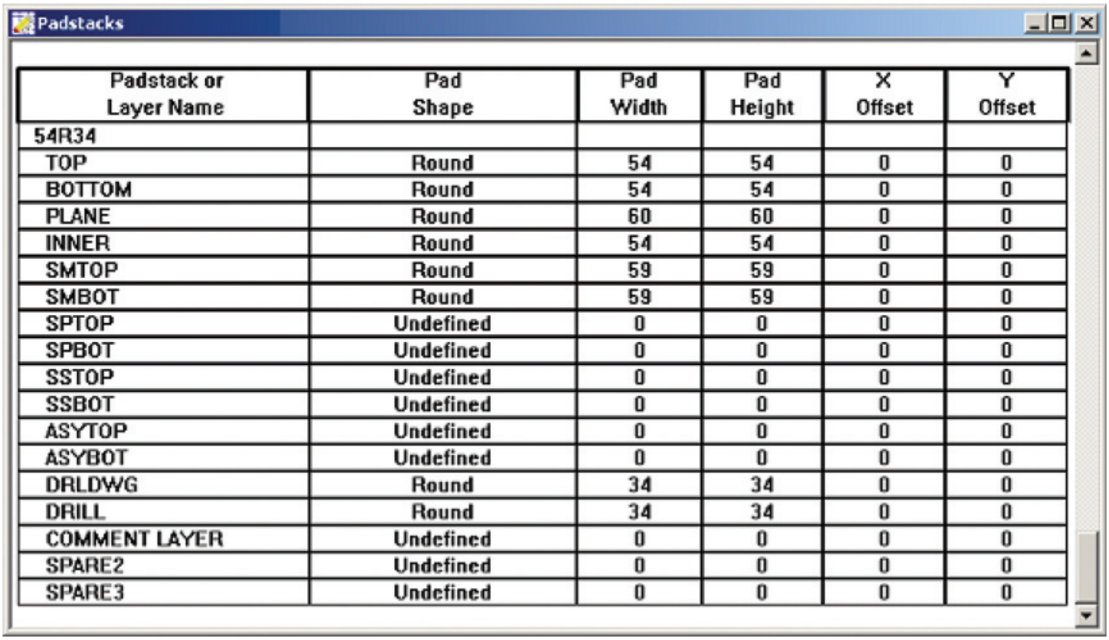

(a)
(b)
45°
80
860
100
ϕ22
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
C1 C2 C7 C8
D1 D2 D7 D8
E1 E2 E7 E8
F1 F2 F7 F8
G1 G2 G3 G4 G5 G6 G7 G8
I1 I2 I3 I4 I5 I6 I7 I8
54
34
22

Figure 8-34 Pin grid array design requirements (units in mils). (a) Package dimensions. (b) Padstack parameters.

Before using the pad array generator, you will need to have the correct padstack present in one of the padstack libraries. A 54R34 padstack is included with the padstack.llb library. If you are using the Demo version you will have to make the padstack and save it to your custom footprint library (UserLibrary.LLB). Use the procedure described above to construct the padstack as shown in Fig. 8-35. Once you have the padstack definitions finished, click the

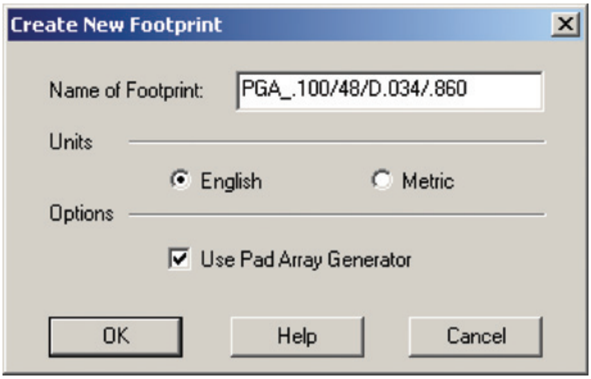


Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
54R34					
TOP	Round	54	54	0	0
BOTTOM	Round	54	54	0	0
PLANE	Round	60	60	0	0
INNER	Round	54	54	0	0
SMTOP	Round	59	59	0	0
SMBOT	Round	59	59	0	0
SPTOP	Undefined	0	0	0	0
SPBOT	Undefined	0	0	0	0
SSTOP	Undefined	0	0	0	0
SSBOT	Undefined	0	0	0	0
ASYTOP	Undefined	0	0	0	0
ASYBOT	Undefined	0	0	0	0
DRLDWG	Round	34	34	0	0
DRILL	Round	34	34	0	0
COMMENT LAYER	Undefined	0	0	0	0
SPARE2	Undefined	0	0	0	0
SPARE3	Undefined	0	0	0	0

Figure 8-35 PGA padstack properties.

54R34 cell in the spreadsheet to select the entire padstack and then right click and select Save to Library... from the pop-up. Save the padstack to your library, and close the spreadsheet.

Next, display the Create New Footprint dialog box by clicking the Create new footprint button in the Library Manager. Enter a name for the PGA footprint (e.g., PGA_.100/48/D.034/.860) as shown in Fig. 8-36. Also, select English units and make sure the Use Pad Array Generator box is checked. Click OK.



Name of Footprint: PGA_.100/48/D.034/.860

Units

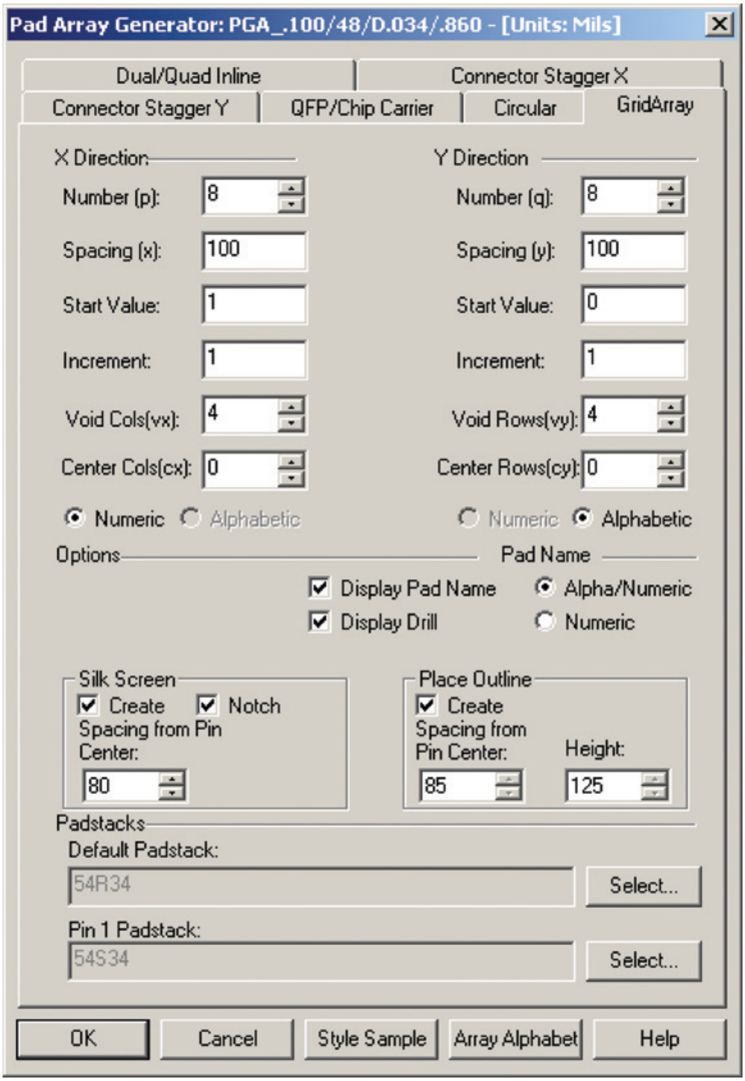
● English ○ Metric

Options

☑ Use Pad Array Generator

Figure 8-36 Using the pad array generator to create a new footprint.

The **Pad Array Generator** dialog box will be displayed; click the **GridArray** tab and enter the values as shown in Fig. 8-37. If the Array Preview window (Fig. 8-39(a)) is covering the dialog box, move it to the side so that it does not obstruct your view but so you can still see it. In the **Padstacks** section of the dialog box, click the **Select**... button to bring up the **Select Padstack** dialog box shown in Fig. 8-38 to select the **Default Padstack.** Scroll down to find the 54R34 padstack. If the **Padstack** library (or the library in which you saved your 54R34 padstack) is not listed, click the **Add** button and add the appropriate library. Repeat the process to select the 54S34 padstack to select a square padstack for the **Pad 1 Padstack.**


Dual/Quad Inline
Connector Stagger X
Connector Stagger Y
QFP/Chip Carrier
Circular
GridArray
Select...
Select...
OK
Cancel
Style Sample
Array Alphabet
Help

Pad Array Generator: PGA_.100/48/D.034/.860 - [Units: Mils]

X Direction
Number (p): 8
Spacing (x): 100
Start Value: 1
Increment: 1
Void Cols(vx): 4
Center Cols(cx): 0
● Numeric ○ Alphabetic

Y Direction
Number (q): 8
Spacing (y): 100
Start Value: 0
Increment: 1
Void Rows(vy): 4
Center Rows(cy): 0
○ Numeric ● Alphabetic

Options
☑ Display Pad Name
☑ Display Drill

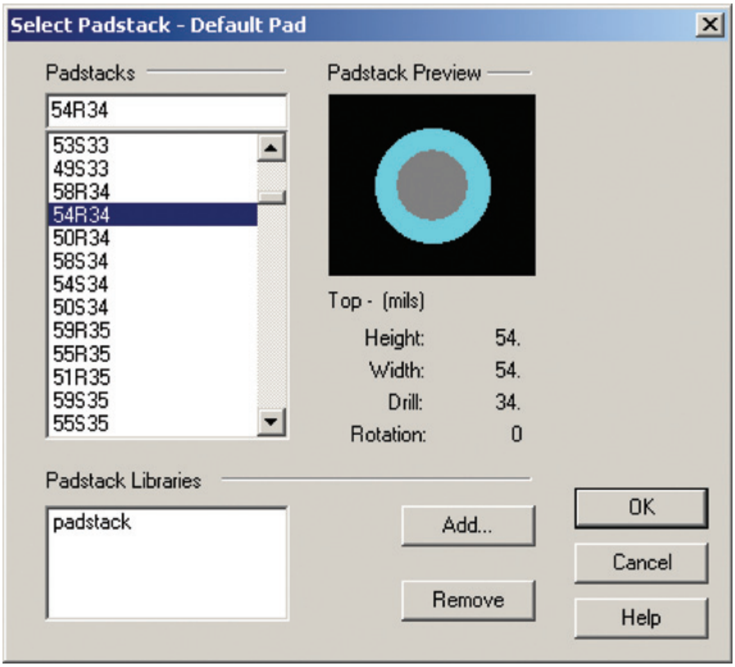
Pad Name
● Alpha/Numeric
○ Numeric

Silk Screen
☑ Create ☑ Notch
Spacing from Pin Center: 80

Place Outline
☑ Create
Spacing from Pin Center: 85
Height: 125

Padstacks
Default Padstack: 54R34
Pin 1 Padstack: 54S34

Figure 8-37 ***Pad Array Generator*** *dialog box.*



Select Padstack - Default Pad

Padstacks

54R34

53S33
49S33
58R34
54R34
50R34
58S34
54S34
50S34
59R35
55R35
51R35
59S35
55S35

Padstack Preview

Top - (mils)

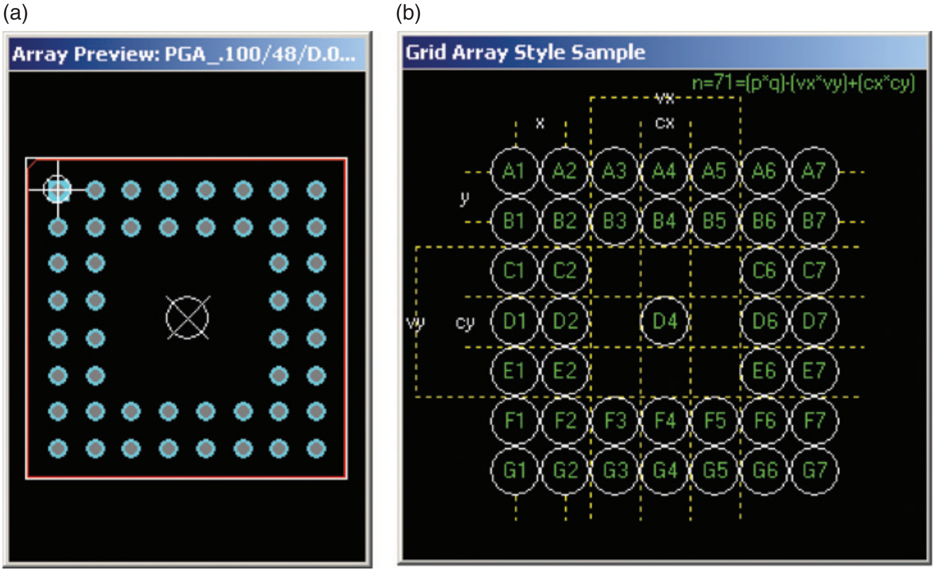
Height: 54.
Width: 54.
Drill: 34.
Rotation: 0

Padstack Libraries

padstack

Add...
Remove
OK
Cancel
Help

Figure 8-38 Padstack selection dialog box.



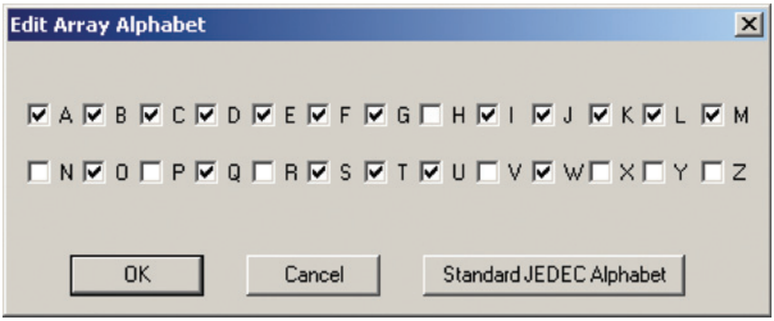
(a)
Array Preview: PGA_.100/48/D.0...
(b)
Grid Array Style Sample
n=71=(p*q)-(vx*vy)+(cx*cy)
vx
x
cx
y
vy
cy
A1
A2
A3
A4
A5
A6
A7
B1
B2
B3
B4
B5
B6
B7
C1
C2
C6
C7
D1
D2
D4
D6
D7
E1
E2
E6
E7
F1
F2
F3
F4
F5
F6
F7
G1
G2
G3
G4
G5
G6
G7

Figure 8-39 Pad array design aids. (a) Array preview. (b) Array style sample.

We want the middle 16 pins removed, so enter 4 in both the **Void Cols (vx):** and **Void Rows(vy):** boxes. You can have the generator create a silk screen and place outline obstacles automatically as well. To do so, enter the values shown in Fig. 8-37.

Toggle the **Style Sample** button at the bottom of the dialog box (Fig. 8-37) to get the Style Sample window shown in Fig. 8-39(b). It changes with each tab you select and displays the spacing parameters to assist you in generating the array.

Toggle the **Array Alphabet** button (bottom of the dialog box in Fig. 8-37) to bring up the **Edit Array Alphabet** dialog box shown in Fig. 8-40. This dialog box is used to set the naming convention for the pins. Notice in Fig. 8-34 that there is no "H" row. Not all letters of the alphabet are used. The JEDEC standard letters are checked in Fig. 8-40. Manufacturers occasionally use their own set of letters when labeling the pins. Make sure that you closely check the data sheet for the device you are using so that the pins on your footprint will match up with the pins on your Capture part in the schematic. Click **OK** to get back to the **Pad Array Generator** dialog box.



☑ A ☑ B ☑ C ☑ D ☑ E ☑ F ☑ G ☐ H ☑ I ☑ J ☑ K ☑ L ☑ M

☐ N ☑ O ☐ P ☑ Q ☐ R ☑ S ☑ T ☑ U ☐ V ☑ W ☐ X ☐ Y ☐ Z

Figure 8-40 ***Edit Array Alphabet*** *dialog box.*

After you have all of the settings as desired in the **Pad Array Generator** dialog box, click **OK.** The pad array generator will automatically construct an 8 × 8 array of 54R34-size padstacks. The finished 48-pin, 8 × 8 PGA footprint is shown in Fig. 8-41.

Finally, save the footprint (if you are not using the Demo version) in one of the existing libraries or a new library as discussed above. If you are using the Demo version, you will not be able to save the footprint because it has more than 14 pins.

Footprint design for BGAs

In this section we see how to construct a footprint for a BGA. Figure 8-42 shows a 15 × 15 BGA. BGAs have advantages over PGAs including higher lead (ball) density (i.e., more I/O pins for the same board real estate), smaller footprints, higher speed, improved heat dissipation, and self-alignment to the PCB during board assembly. But with these advantages come

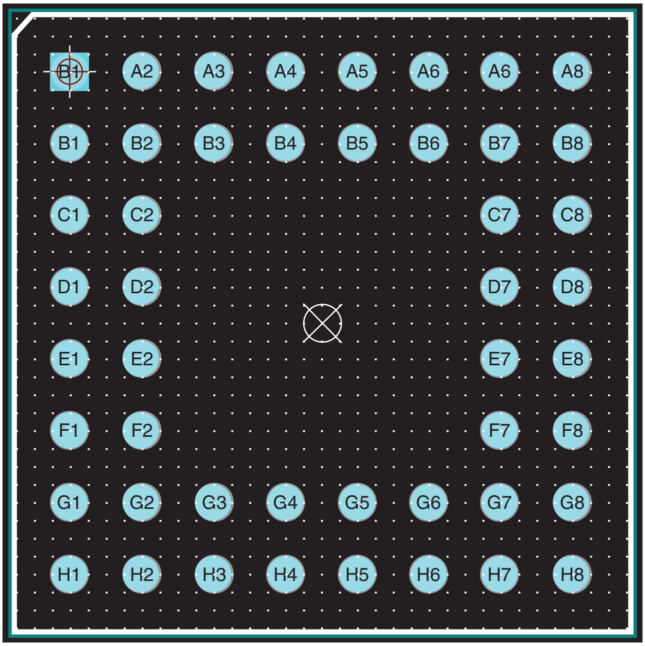

B1
A2
A3
A4
A5
A6
A6
A8
B1
B2
B3
B4
B5
B6
B7
B8
C1
C2
C7
C8
D1
D2
D7
D8
E1
E2
E7
E8
F1
F2
F7
F8
G1
G2
G3
G4
G5
G6
G7
G8
H1
H2
H3
H4
H5
H6
H7
H8

Figure 8-41 Completed 8 × 8 pin grid array with 48 pins.

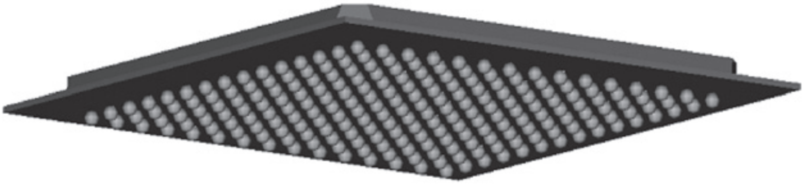


Figure 8-42 A 15 × 15 BGA as seen from the bottom.

greater footprint design and board layout challenges because of the greater interconnect density. The specific functions of the I/O pins and the locations of power and ground pins may also have a significant impact on footprint design details and on how the BGA will ultimately be routed.

The full version of OrCAD Layout includes about 80 BGA footprints. Footprint BGA10M_ 1.00/100/B.60/W11.00 is shown in Fig. 8-43. The padstacks are actually surface-mount pads (i.e., only TOP copper, top soldermask, top solder paste, and top assembly pads are defined). The pads are 24 mils in diameter (0.6 mm) and spaced 39 mils (1 mm) apart. That leaves only 16 mils from the edge of one pad to the edge of the next nearest pad. This spacing allows only one trace (two at the most) between pads. For example, if the width of a routing trace

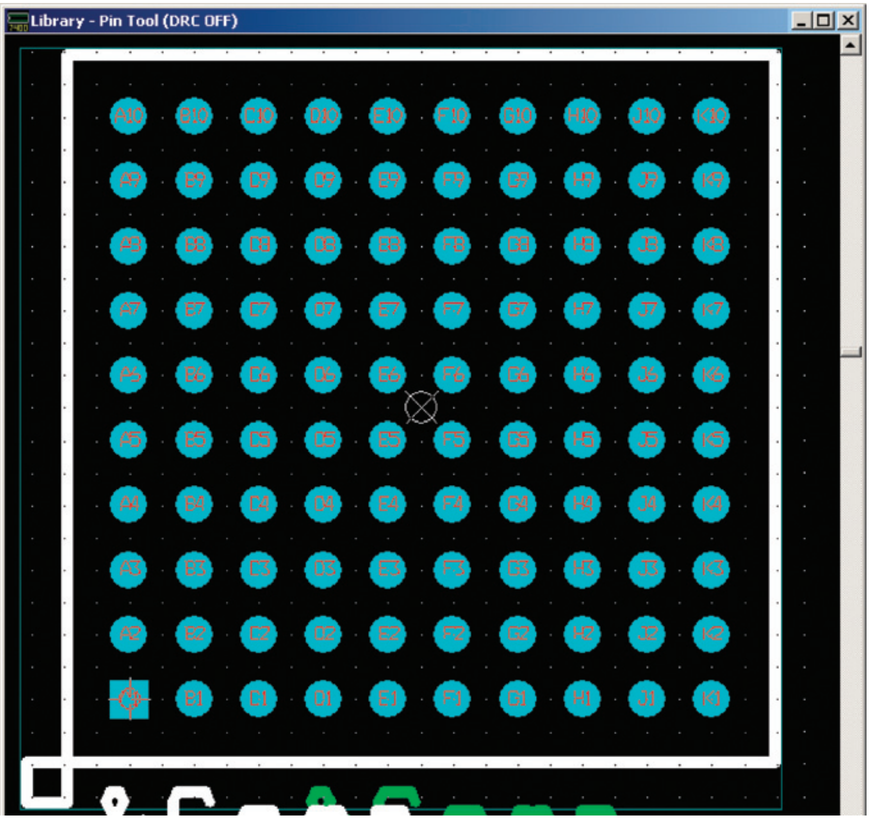


Figure 8-43 A 10 × 10 BGA footprint from the BGA library (viewed from top).

is 6 mils, then 5 mils remain for the spacing on each side of the trace, which uses up the full 16 mils. In order to get two traces and the associated spacing, the traces and spaces would have to be 3 mils wide. Depending on the capabilities of your board manufacturer, that may be risky. You can see that if you try to route the traces from the inner pads outward, you will quickly run out of available routing spaces after the first two rows.

The only solution is to insert fan-out vias for each of the inner pads so that traces to/from the inner pads can be immediately routed to different layers in order to avoid the pads on the outer rows. Figure 8-44 shows an 8 × 8 BGA fanout. Because of the tight tolerances and small dimensions, custom pads and vias must be employed. These vias along with their respective pads are commonly called “dogbones” (see Fig. 8-45). The vias typically have smaller features than the Layout’s default vias, and they are usually tented, i.e., they do not have a soldermask opening.

Another important detail of the dogbone is that the soldermask opening where the solder balls are attached usually is what is called a non-soldermask-defined (NSMD) pad. Figure 8-46 shows the difference between soldermask-defined pads and NSMD pads. NSMD pads

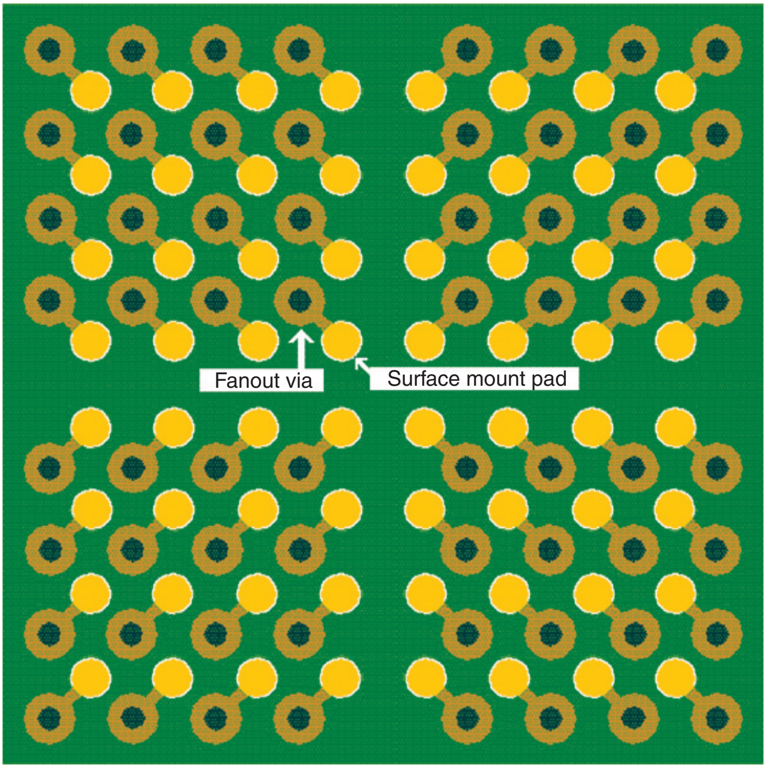

Fanout via
Surface mount pad

Figure 8-44 An 8 × 8 BGA fanned out with dogbones.

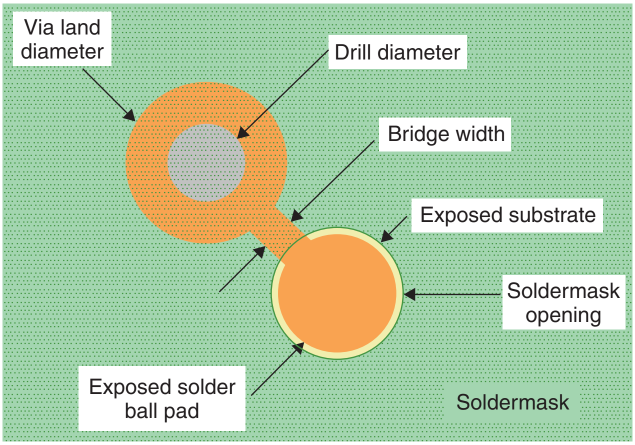

Via land diameter
Drill diameter
Bridge width
Exposed substrate
Soldermask opening
Exposed solder ball pad
Soldermask

Figure 8-45 Details of a "dogbone" fanout for a BGA.

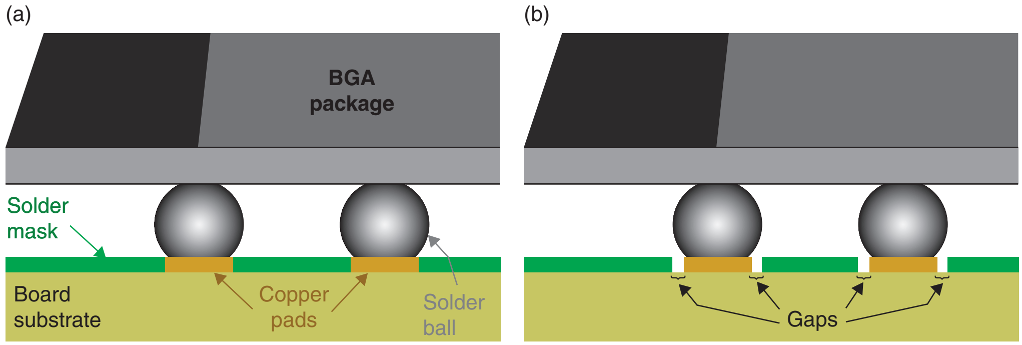


Figure 8-46 Soldermask definitions for BGAs. (a) Soldermask defined. (b) Non-soldermask defined—preferred.

are preferred because the larger openings prevent the pads from being significantly shadowed (covered) by the soldermask due to soldermask misregistration (misalignment). NSMD pads also provide greater surface area for the solder balls to cling to by using the sides of the pads in addition to the tops of the pads. This also helps with the self-alignment of the BGA to the PCB.

When using BGAs in your PCB design there are two approaches to designing and fanning out BGA footprints:

1. Use the pad array generator to array surface-mount pads and save the footprint to a library, then add the fanouts to the PCB later.
2. Use the pad array generator to array PTH vias instead of the surface-mount pads. Move the vias to the fanout locations and then add surface-mount pads and bridges to make the dogbones, then save the pre-fanned out footprint.

If you use a basic BGA footprint and perform the fanout on the board you can place the fanout vias exactly where you want them, but you will have to do that for each and every BGA footprint on every board. If you fan out the footprint ahead of time, much of the work is done up front and that work can be reused. However, the pad array generator will array only the surface-mount pads or the vias but not both. So, if you pre-fan out a BGA footprint, you will have to add one or the other manually to make a dogbone fanout even when using the pad array generator, and you may still have to rearrange the fanouts later on the board depending on the functions of specific BGA pins. Overall though, if you pre-fan out the BGA at the footprint level you can often save yourself a considerable amount of work in the long run.

In this example we will choose option 2, i.e., design a BGA footprint with dogbone fanouts using the pad array generator. The example will be a fictitious (but simple) 4 × 4 BGA. The dimensions are shown in Fig. 8-47. Using a (fictitious) data sheet as a guide, it is determined that the footprint parameters are:

Ball pitch (spacing):	50 mils (1.27 mm)
Ball diameter:	30 mils (0.75 mm)

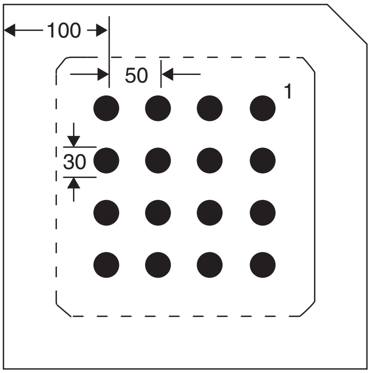


Figure 8-47 Dimensions for fictitious 16-pin BGA (units in mils).

Ball land diameter: 22 mils (0.55 mm)

Soldermask diameter: 26 mils (0.61 mm)

IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard,* provides guidelines on BGA footprints and fanout dimensions. Using IPC-7351 and Fig. 8-45 as a guide, we determine the fanout parameters to be:

Bridge width: 6 mils (0.152 mm)

Via hole diameter: 14 mils (0.0.36 mm)

Via land diameter: 28 mils (0.71 mm)

First, make the PTH via that will be used for the dogbones and save it to your UserLibrary. **To make a dogbone via** open the Layout Library Manager and open the Padstacks spreadsheet. Select one of the padstacks, right click, and select New from the pop-up. Double click the new padstack (or select it, right click, and select Properties... from the pop-up) to display the Edit Padstack dialog box. Rename the new padstack to something like BGA_VIA/28R14. Using Fig. 8-48 as guide, modify the padstack to meet the needs of the BGA fanout. Note that soldermask is undefined. This is done intentionally to produce a “tented” via, which helps prevent solder bridges and solder migration.

Once the via has been defined select the via, right click, and select Save to Library... from the pop-up. You can save the padstack in the padstack.llb or save it to your UserLibrary, and close the spreadsheet.

The next step is to **use the pad array generator to build a 4 ×4 BGA**. From the Library Manager click the Create New Footprint button. The Create New Footprint dialog box will be displayed. Enter a name for the footprint (since this is just practice, keep it simple, e.g., BGA/4x4). Select English units and check the Use Pad Array Generator box; click OK. Use the pad array generator to construct a 4 × 4 array as shown in Fig. 8-49. Remember to select the new VIA_BGA/28R14 as the pad to be arrayed. Click OK to display the array.

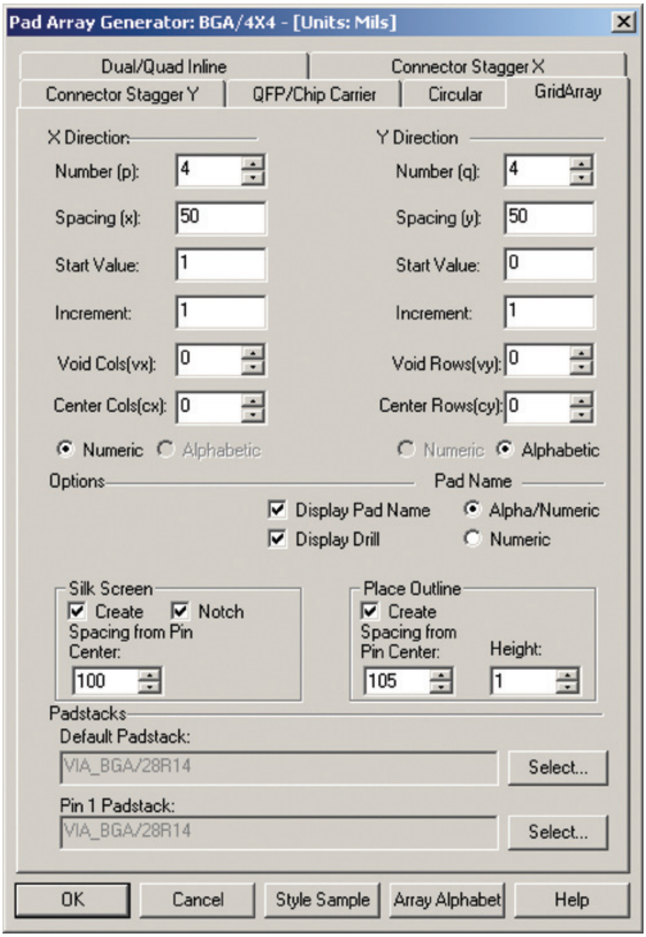
Padstack or Layer Name	Pad Shape	Pad Width	Pad Height
VIA_BGA/28R14			
TOP	Round	28	28
BOTTOM	Round	28	28
PLANE	Round	34	34
INNER	Round	28	28
SMTOP	Undefined	0	0
SMBOT	Undefined	0	0
SPTOP	Undefined	0	0
SPBOT	Undefined	0	0
SSTOP	Undefined	0	0
SSBOT	Undefined	0	0
ASYTOP	Undefined	0	0
ASYBOT	Undefined	0	0
DRLDWG	Round	14	14
DRILL	Round	14	14
COMMENT LAYER	Undefined	0	0
SPARE2	Undefined	0	0
SPARE3	Undefined	0	0

Figure 8-48 BGA fan-out via definitions.

Although we are using the array generator to place through-holes as the BGA “pads,” they will ultimately be the fanouts, and shortly we will add the pads to which the BGA is soldered. The reason for doing it this way is that the autorouter routes to the named pads of a footprint. The array generator places the correct number of vias for the device and names them, forcing the autorouter to route to these “pins” instead of the surface-mount pads. Also, Layout allows adding copper areas (the surface-mount pads) to a footprint and attaching them to the named footprint pins, but Layout does not allow adding free vias to a footprint and then attaching them to a named pin. Even if it did, the autorouter would typically ignore the via and try to route to the named pin anyway, and if it could not it might use the via or it might insert one of its own.

Figure 8-50 shows the initial view of the new BGA (you might have to move the text out of the way to get the same view). The next step is to place the surface-mount pads for the ball lands. Begin by changing the grid settings by selecting System Settings from the Options menu. Change the visible grid to 2 mils and change all of the other grids to 1 mil.

Select the Pin tool and move pad A1 up and to the left by 25 × 25 mils (see Fig. 8-51 for reference). Add a surface-mount pad to A1’s original place (0,0). **To add the surface-mount pad** select the Obstacle tool, right click and select New, right click again and select Arc,



Pad Array Generator: BGA/4X4 - [Units: Mils]

X Direction:
Number (p): 4
Spacing (x): 50
Start Value: 1
Increment: 1
Void Cols(vx): 0
Center Cols(cx): 0
● Numeric ○ Alphabetic

Y Direction
Number (q): 4
Spacing (y): 50
Start Value: 0
Increment: 1
Void Rows(vy): 0
Center Rows(cy): 0
○ Numeric ● Alphabetic

Options
☑ Display Pad Name
☑ Display Drill

Pad Name
● Alpha/Numeric
○ Numeric

Silk Screen
☑ Create ☑ Notch
Spacing from Pin Center: 100

Place Outline
☑ Create
Spacing from Pin Center: 105
Height: 1

Padstacks
Default Padstack: VIA_BGA/28R14
Pin 1 Padstack: VIA_BGA/28R14

Figure 8-49 Pad array generator setup for 4 × 4 practice BGA.

right click again and select Properties. Select Copper area, Top layer, and Width = 0 mils, and check the Do not fill beyond obstacle boundaries box. Select the Pin Attachment... button, select the Attach to pin radio button, and enter A1 in the Pin name text box. Click OK twice.

Click and release the left mouse button at location 0,0 to start the pad. Move the mouse 11 mils to the right to make a pad with a diameter of 22 mils. Click and release the mouse button again to complete the pad.

Next, place the bridge (a free track) from the pad to the via. Change all of the grid settings to 5 mils. Select the Obstacle tool, right click and select New, right click again and select Properties. Select Free track, Top layer, Width = 5 mils, and attach the obstacle to A1. Click OK. Draw a trace from the via to the copper pad by left clicking on the pad, move the

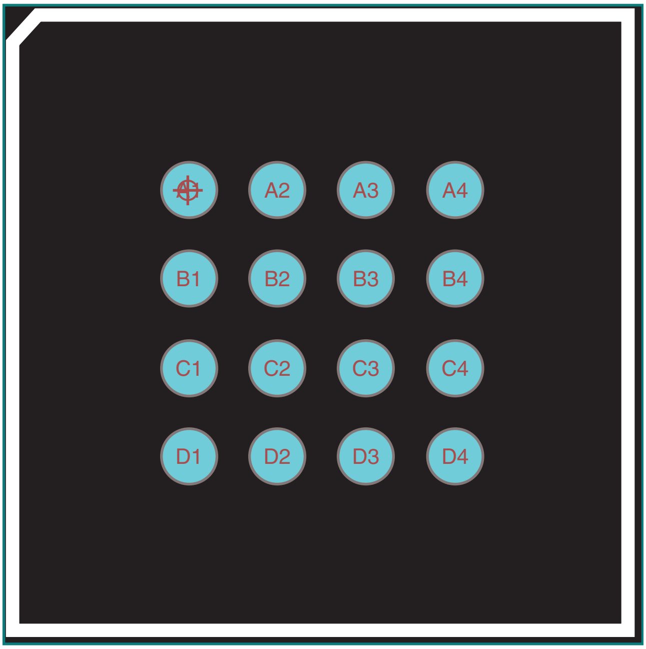


Figure 8-50 Initial view of the 16-pin practice BGA.

mouse to the via, and left click again to complete the segment. Right click and select End Command to end the segment. The bridge and the pad are now connected to the pin physically and by name.

Next make a soldermask opening over the pad. Copy the copper pad (Ctrl + left click, right click, and select Copy) and paste the copy in an open space off to the side. Ctrl + left click to select New Obstacle, right click, and select Properties. Change the layer to SMTOP and Width to 0. Click OK. Change the detail grid to 1 mil, grab the right edge of the new obstacle, and drag it 2 mils to the right to make the obstacle's diameter 4 mils bigger (26 mils total diameter). Left click the mouse to finish resizing it. Use Ctrl + left click and select the soldermask opening at its center. Move it so that it is centered over the copper pad and left click to place it. Right click and select End Command. The finished dogbone is shown in Fig. 8-51.

Using the Pin and Obstacle tools, move the remaining pins to their new locations and copy the copper pads, copper bridges, and soldermask openings for each pin as shown in Fig. 8-52. Select and rotate the bridges as necessary for each pin. Each copper area will have to be attached to its respective pin. **To change the pin attachments**, select the copper object, right click, and select Properties. Select the Pin Attachment... button, the Attach to pin radio button should already be selected. Enter the correct pin name in the Pin name text box.

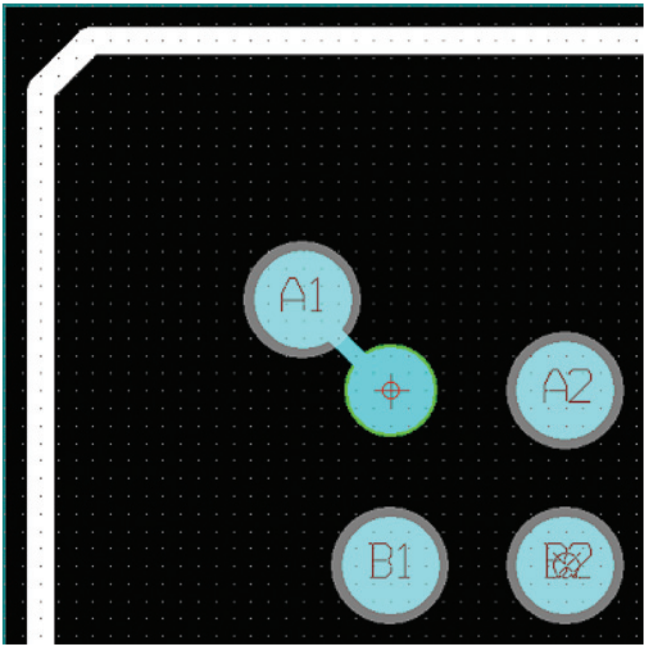


Figure 8-51 The completed "dogbone" fanout for pin A1.

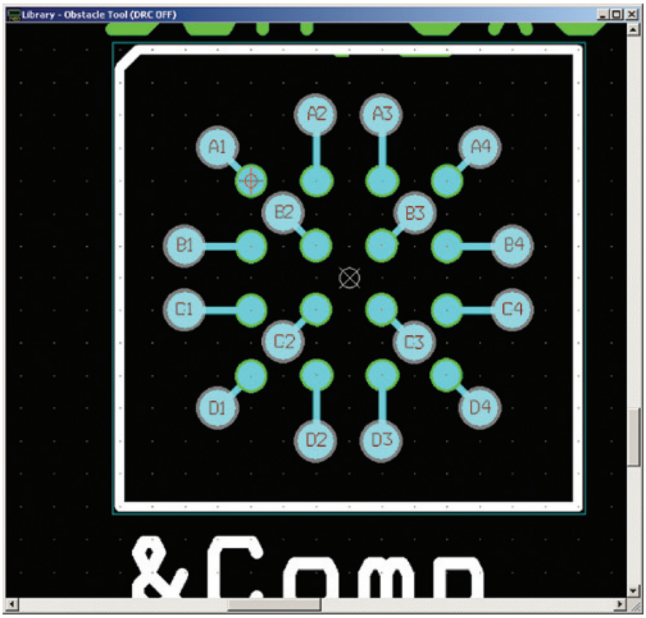

Library - Obstacle Tool (DRC OFF)
A1
A2
A3
A4
B1
B2
B3
B4
C1
C2
C3
C4
D1
D2
D3
D4
&Comp

Figure 8-52 The completed pre-fanned out BGA.

Blind, buried, and microvias

Blind and buried vias are not designed into footprints but are added to a PCB during the layout and routing process. An example of designing using blind vias is given in Chap. 9, but is discussed briefly here to show how they can be used with BGAs.

Figure 8-53 shows how microvias and blind and buried vias can help route high-density BGAs. In Fig. 8-53 a BGA is placed on the top of a board and another surface-mounted device is placed directly opposite the BGA on the bottom of the board. To accomplish this, through-hole vias cannot be used. Fanout and routing of the BGA are accomplished using blind and buried vias. Blind vias are visible only on one side of the PCB and connect traces on the one outer layer to inner traces only, while buried vias are not visible from either side of the board and connect traces only between inner layers.

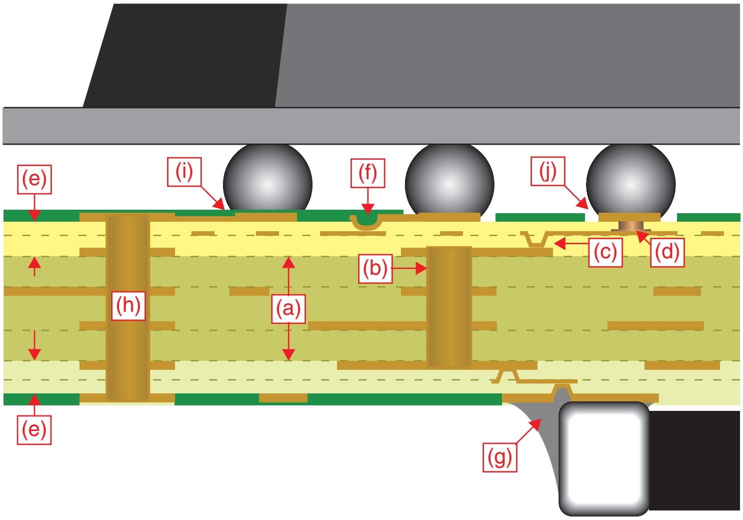


Figure 8-53 Various via technologies and their applications.

Blind and buried vias are realized on built-up PCBs. A built-up PCB often has a standard layer stack-up core (section (a) in Fig. 8-53) and additional layers are sequentially added to the board (the two (e) sections in Fig. 8-53). Plated through-hole vias in the standard core become buried vias ((b) in Fig. 8-53). As the outer layers are built up on top of the base core, buried microvias ((c) in Fig. 8-53) and blind microvias ((d) in Fig. 8-53) can be embedded into the outer layers. During the build-up process resistors or capacitors can also be buried in the layers. After all of the layers have been built up, additional microvias ((f) and (g) in Fig. 8-53) and standard plated through-holes ((h) in Fig. 8-53, tented on the top end) can be added to the entire assembly.

Figure 8-53 shows three types of microvias: (c) and (g) are laser-drilled, plated vias; (d) is a laser-drilled, paste-filled via; and (f) is a plasma-etched, plated via. To learn more about designing built-up boards and microvias see *Coombs' Printed Circuits Handbook*.

Mounting holes

Mounting holes can be used for attaching the PCB to mounting hardware (such as stand-offs) or for attaching hardware to the PCB (such as heat sinks). Mounting holes are considered component footprints but are not part of the schematic. The four basic hole types are shown in Table 8-2; in them holes can be made with or without lands (pads), with or without plating, or with any combination of the two. Mounting holes that are plated can be attached to any net, or they can be isolated from all nets. When mounting holes are attached to a net that is assigned to a plane layer the hole can be connected to the plane through thermal reliefs or flood planes/pours just like any other plated through-hole.

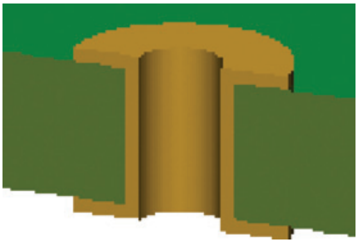
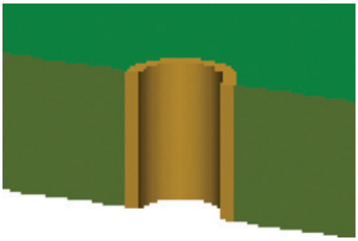
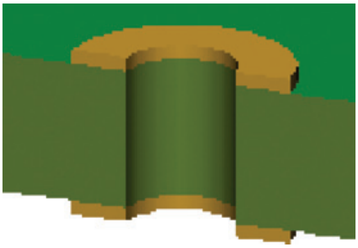
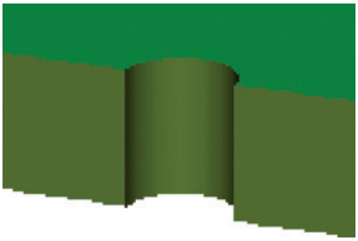
	Plated	Nonplated
With pads	2a 	2c 
Without pads	2b 	2d 

Table 8-2 Basic hole types

The full version of Layout contains the Layout.LLB footprint library, which contains three mounting-hole templates (MTHOLE1 through MTHOLE3), which are all plated holes with no pads. However, they or any other padstack can be modified to construct any one of the hole types in Table 8-2. A reference table of drill and screw sizes is provided in Appendix E as an aid to designing mounting holes for standard screw sizes.

The pad and plating definitions are set independently. Table 8-3 shows the pad, clearance, and drill parameters for the padstack. **To make a hole with pads** (regardless of whether or not it will be plated) select the Padstack spreadsheet and select an existing padstack or right click and select New from the pop-up. Set up the padstack pads as you would any other padstack per Table 8-3. Save the padstack in a library as described above.

Layer	With pads, plated	With pads, nonplated	No pads, plated	No pads, nonplated
TOP/BOTTOM	As required	As required	1	1
INNER	As Required	As required	1	1
SM	Optional	Optional	1	1
PLANE	DRILL + 15 mils (min)	DRILL + 15 mils (min)	DRILL + 15 15 mils (min)	DRILL + 15 mils (min)
DRILL	As required	As required	As required	As required

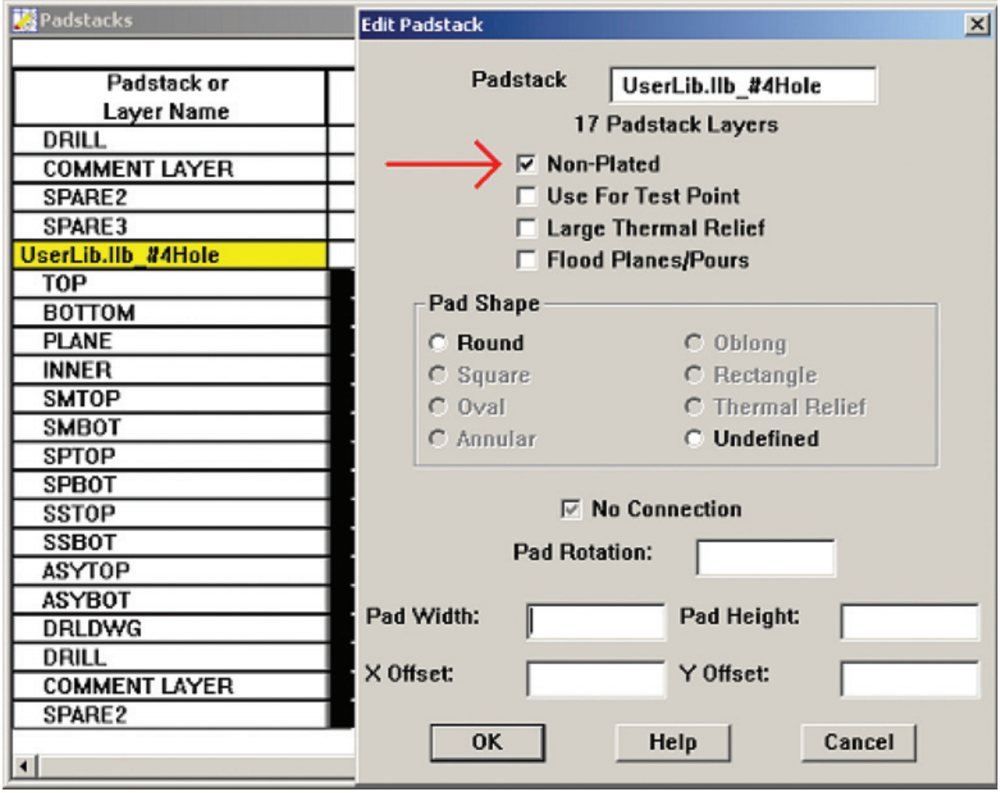
Table 8-3 Padstack definitions for various hole types

To make a padless mounting hole (regardless of whether or not it will be plated) select the Padstack spreadsheet and select an existing padstack or right click and select New from the pop-up. Set up the padstack pads as indicated in Table 8-3. When you set the pad diameters to 1 the router knows to ignore them and they will be drilled out during the manufacturing process. If you set the pads to 0 the pad will be undefined and Layout will interpret the padstack as a blind or buried via. The holes of some footprints that come with the software have pad diameters that are equal to the drill diameter. Ideally this accomplishes the same thing as setting the pad size to 1 and the pads will be drilled out. However, because a certain amount of misregistration occurs during board fabrication a thin ring of copper may be left behind during the drilling process. It is generally harmless but is an imperfection. Setting the pad size to 1 ensures that all the copper is removed.

To make a nonplated mounting hole (regardless of whether or not it has pads) select the Padstack spreadsheet and select an existing padstack or right click and select New from the pop-up. Set up the padstack pads per Table 8-3 depending on whether or not you want pads. Double click the padstack name to display the Edit Padstack dialog box as shown in Fig. 8-54. Place a check mark in the Non-Plated box and click OK.

When the board is postprocessed a second drill file (in addition to the standard thruhole.tap file) that will have a .NPT extension will be generated. A second drill file is needed because nonplated holes are drilled after all plating processes are complete, whereas plated through-holes are drilled before the plating process; therefore a completely separate set of instructions is required.

Examples of how to place a mounting hole on a board and connect it to a net are given in Chap. 9, Example 2. A brief description is provided here for convenience. **To place a mounting hole on a board** choose the Component Tool, right click, and select New from the pop-up. Click the Footprint... button and select a mounting hole from one of the libraries. Place a check mark in the Not in Netlist box and click OK (this prevents the holes from being removed during AutoECO operations). Left click to place the mounting hole. **To connect a mounting hole to a net** choose the Pin Tool, select the hole using Ctrl + left click, right click, and select Properties... from the pop-up. In the Modify Connections dialog box select the desired net from the Net Name list. Click OK.



Padstack or Layer Name
DRILL
COMMENT LAYER
SPARE2
SPARE3
UserLib.llb_#4Hole
TOP
BOTTOM
PLANE
INNER
SMTOP
SMBOT
SPTOP
SPBOT
SSTOP
SSBOT
ASYTOP
ASYBOT
DRLDWG
DRILL
COMMENT LAYER
SPARE2

Padstack: UserLib.llb_#4Hole

17 Padstack Layers

☑ Non-Plated
☐ Use For Test Point
☐ Large Thermal Relief
☐ Flood Planes/Pours

Pad Shape
○ Round
○ Square
○ Oval
○ Annular
○ Oblong
○ Rectangle
○ Thermal Relief
○ Undefined

☑ No Connection

Pad Rotation:

Pad Width:

Pad Height:

X Offset:

Y Offset:

Figure 8-54 Defining a nonplated mounting hole.

Printing a catalog of a footprint library

You can print out a catalog of an entire footprint library, which you can use as a reference. You can also create a PDF file of a footprint library. The directions are provided in Chap. 15 of the *Layout User's Guide* (search for Catalog Tool). The directions are very straightforward, so they will not be duplicated here.

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CHAPTER 9

PCB Design Examples

In Chap. 2 the basic PCB design flow was demonstrated starting from schematic entry with Capture to board routing with Layout, but no attention was given to board design issues such as component placement and spacing rules, layer stack-up, or trace routing and spacing rules.

Design examples will be used in this chapter to illustrate the various PCB design considerations described in Chaps. 5 and 6 and how to use the Layout tools to accomplish the design goals. The part count in each example is kept to a minimum (all designs have fewer than 10 parts and 14 pins/part) so as not to be cumbersome and not to distract the reader from understanding how to route and set up layers and so that the Demo version can be used. In-depth discussion on PCB design manufacturability is covered in Chap. 5 and signal integrity and routing are covered in Chap. 6.

The following examples use parts that may not be included with your version of OrCAD. You can make the parts yourself using the procedures discussed in the previous chapters, or you can copy the parts and footprints provided in the example libraries located on the CD-ROM included with the book.

The first example is a simple analog design using a single op-amp. The design shows how to set up multiple plane layers for positive and negative power supplies and ground. The design also demonstrates several key concepts in Capture, such as how to connect global nets, how to assign footprints, how to perform design rule checks, how to use the Capture part libraries, how to generate a bill of materials (BOM), and how to use the BOM as an aid in the design process in Capture and Layout. The design also shows how to perform important tasks in Layout such as loading board technology files, finding and selecting specific parts, and modifying padstacks. Intertool communication (such as annotation and back annotation) between Capture and Layout is also demonstrated.

The second example is a mixed, digital/analog circuit. In addition to the tasks demonstrated in the first example, the design also demonstrates how to set up split planes to isolate analog and digital power supplies and grounds. Other tasks include using copper pours on routing layers to make partial ground planes, using copper pours on plane layers to make nested power and ground planes, and defining anti-copper areas on plane and routing layers.

The third example uses the same mixed, digital/analog circuit from the second example but demonstrates how to use multiple-page schematics and off-page connectors to organize and simplify large circuit designs and to incorporate PSpice simulations into a PCB layer design. It also demonstrates how to construct multiple, separated power and ground planes and a shield plane to completely isolate analog from digital circuitry. The use of guard rings and guard traces is also demonstrated.

The fourth example is a high-speed digital design that demonstrates how to design transmission lines, stitch multilayer ground planes, perform pin/gate swapping, place moated ground areas for clock circuitry, and design a heat spreader.

Overview of the Design Flow

Regardless of which type of board will be made, certain steps must be executed in the design flow process. The following is an outline of the process.

(I) Initial design concept and preparation.
    (A) Generate initial drawings.
    (B) Collect data sheets.
    (C) Take inventory of packaging/footprint needs.
    (D) Search through the Capture libraries to find the parts. For any parts that are not available, construct the parts using the Capture Part Editor or the PSpice Model Editor.

(II) Set up the design project in Capture.
    (A) Draw the schematic (placing and connecting parts).
    (B) Perform an annotation to clean up numbering.
    (C) Make sure multipart packages are properly utilized.
    (D) Make sure that global power nets are properly connected.
    (E) Assign related components to groups to aid in part placement in Layout.
    (F) Perform a Capture design rule check (DRC) to verify that the circuit schematic has no issues. Correct any errors and repeat DRCs as needed.
    (G) Generate a bill of materials to identify PCB assigned/missing footprints.
    (H) Search through the Layout libraries to find and assign footprints. For any footprints that are not available, obtain the data sheets for recommended land patterns and design the footprints using Layout Library Manager.
    (I) Generate netlist (.MNL) for Layout.

(III) Define the board requirements.
    (A) Board dimensions and mounting hole locations.
    (B) Part placement considerations (height restrictions, assembly method).
    (C) Noise and shielding requirements.
    (D) Component mounting technology (SMT, THT).
    (E) Trace width and trace spacing requirements.
    (F) Required vias and fanouts (size and tenting, etc.).
    (G) Number of power/ground planes and signal layers.

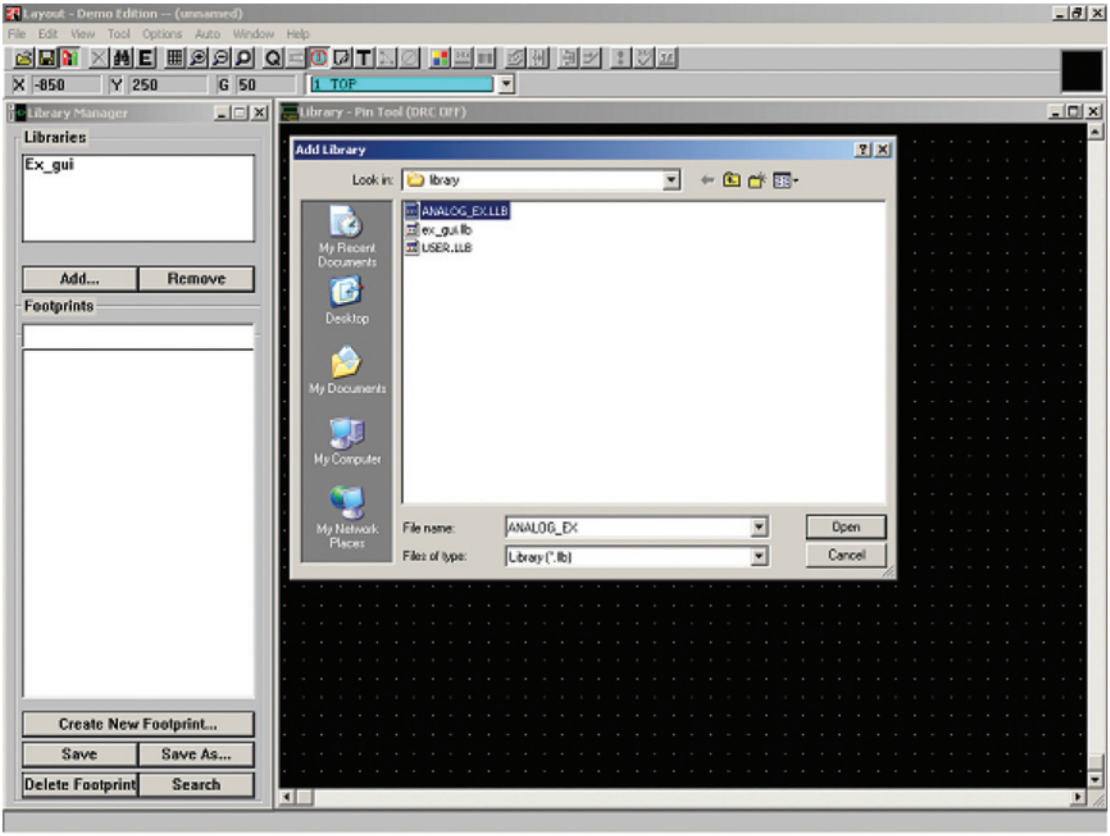
- (IV) Import the design into Layout and using AutoECO tool.
  - (A) Assign the technology file (.TCH).
  - (B) Load the Capture netlist file (.MNL).
  - (C) Save the design as board file (.MAX).
- (V) Basic board setup.
  - (A) Physical.
    - (1) Create the board outline using Obstacle tool.
    - (2) Place mounting holes.
    - (3) Define part and routing restriction areas.
    - (4) Add dimension documentation (optional).
  - (B) Preliminary parts placement.
    - (1) Use search/place tools to place selected parts and groups.
    - (2) Perform a board DRC to check for footprint and placement problems.
  - (C) Layer setup.
    - (1) Set up power and ground planes.
    - (2) Set up routing layers.
    - (3) Assign ground and power nets to plane layers.
    - (4) Define thermal relief parameters.
    - (5) Set which vias to use for fanouts, free vias, jumpers, etc.
    - (6) Perform a DRC to check for layer problems.
  - (D) Final parts placement.
    - (1) Make sure spacing rules are not violated.
    - (2) If using split or moated plane layers, make sure parts are placed accordingly.
    - (3) Check orientation of polarized components (caps, diodes, etc.).
- (VI) Preroute specific nets using manual and restricted autorouting.
  - (A) Perform power and ground fanouts.
  - (B) Preroute critical nets manually.
  - (C) Perform DRC to make sure that no errors have occurred. Fix errors.
- (VII) Autorouting.
  - (A) Set up the autorouter.
  - (B) Run the autorouter.
  - (C) Perform DRC to make sure that no errors have occurred. Fix errors.
- (VIII) Finalizing the design.
  - (A) Postrouting inspection.
    - (1) Sharp (acute) angles.
    - (2) Long parallel traces (cross-talk issues).
    - (3) Via locations.
    - (4) Silk-screen markings.
  - (B) Board cleanup.
    - (1) Unroute and then reroute problem traces.
    - (2) Perform a final DRC.
  - (C) Synchronization with Capture (back annotation).

A detailed example of how to postprocess a design and submit it to a board house is included in Chap. 10.

Example 1: Dual Power Supply, Analog Design

The first example will demonstrate the basics of schematic entry in Capture, including finding and placing parts, connecting parts and using global power nets, and generating a bill of materials to assist in the design process. The example continues with PCB design in Layout and demonstrates how to specify board requirements such as trace width and spacing and figuring out how to determine which technology file to use. Finally, the example outlines a process for setting up the overall board design, how to define layers, and how to perform manual and automatic routing.

To follow the example exactly as it is presented here you will need to copy the footprint library for this example from the CD included with this book. Copy the ANALOG_EX.LLB file located in the Projects/Analog_Ex folder on the CD into the OrCAD/OrCAD_10.5_Demo/Tools/



X -850 Y 250 G 50 1 TOP

Libraries: Ex_gui

Look in: library

ANALOG_EX.LLB
ex_gui.llb
USER.LLB

File name: ANALOG_EX

Files of type: Library (*.llb)

Layout - Demo Edition -- (unnamed)
File
Edit
View
Tool
Options
Auto
Window
Help
Library Manager
Footprints
Add...
Remove
Create New Footprint...
Save
Save As...
Delete Footprint
Search
Library - Pin Tool (DRC OFF)
Add Library
My Recent Documents
Desktop
My Documents
My Computer
My Network Places
Open
Cancel

Figure 9-1 Adding the analog example footprint library.

Layout/Library folder. After you copy it into the folder you will have to let Layout know that it is there by adding it to the library list. To do so, open Layout and, from the session frame, select Library Manager from the Tools menu. In the Library Manager click the Add... button located under the Libraries list box. From the Add Library dialog box select the ANALOG_EX.LLB library, and click the Open button. ANALOG_EX should now be displayed in the Libraries list box. You can now close the Layout Library Manager window (Fig. 9-1).

Although all of the schematic and design files for this example are also included on the CD, you do not have to copy them because all of the Capture parts in the example are already included with the OrCAD software. However, if you choose to copy the design files simply copy the entire ANALOG_EX folder into your project folder. If you do not have a project folder set up, now would be a good time to set one up. You can set it up anywhere your computer has access to and OrCAD should have no problem with it.

Initial design concept and preparation

Before you start a PCB design process, you will likely have some sort of preliminary design concept jotted down. Perhaps PSpice simulations of sections of the design have even been performed. The design concept for this example is shown in Fig. 9-2. The circuit is very simple, but it contains enough parts that it encompasses the same steps required for larger, more complicated designs. The circuit is a basic amplifier that consists of an active component (the op-amp) and several passive components (resistors and capacitors). The circuit also contains an off-board connector that supplies dual rail power to the board and provides connections for input and output signals. Through-hole components include the connector and power supply filter capacitors; surface-mounted devices include the op-amp, its bypass caps, and the signal conditioning and gain resistors.

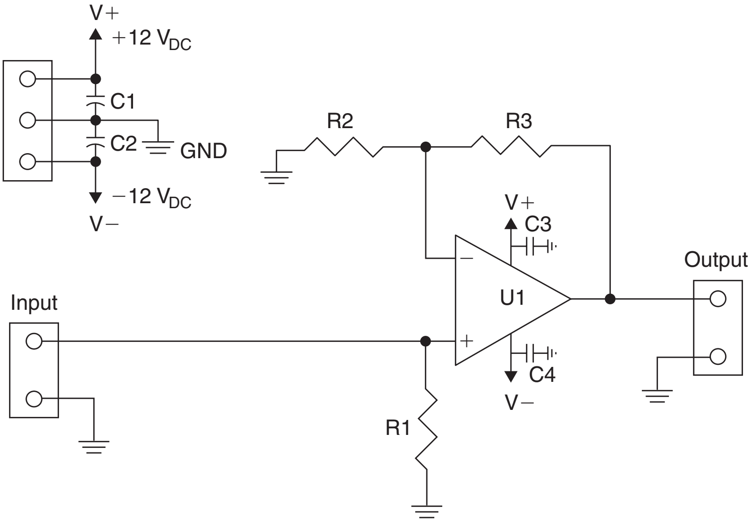


Figure 9-2 Analog circuit for design Example 1.

Once you have the basic design down, you will need to make a list of all the parts needed to build the circuit, including the off-board connector. Search through your favorite parts catalog to find the parts and download the data sheets from the manufacturers. It is helpful to make a spreadsheet that details the parts and footprints to keep track of the design details throughout the design flow so that once you receive the board from the manufacturer, the parts fit properly. An example spreadsheet is given in Table 9-1. During the entire design process you can continually add information to the spreadsheet to document and organize all aspects of the design process. If a problem does occur, the documentation can help identify where the fault occurred.

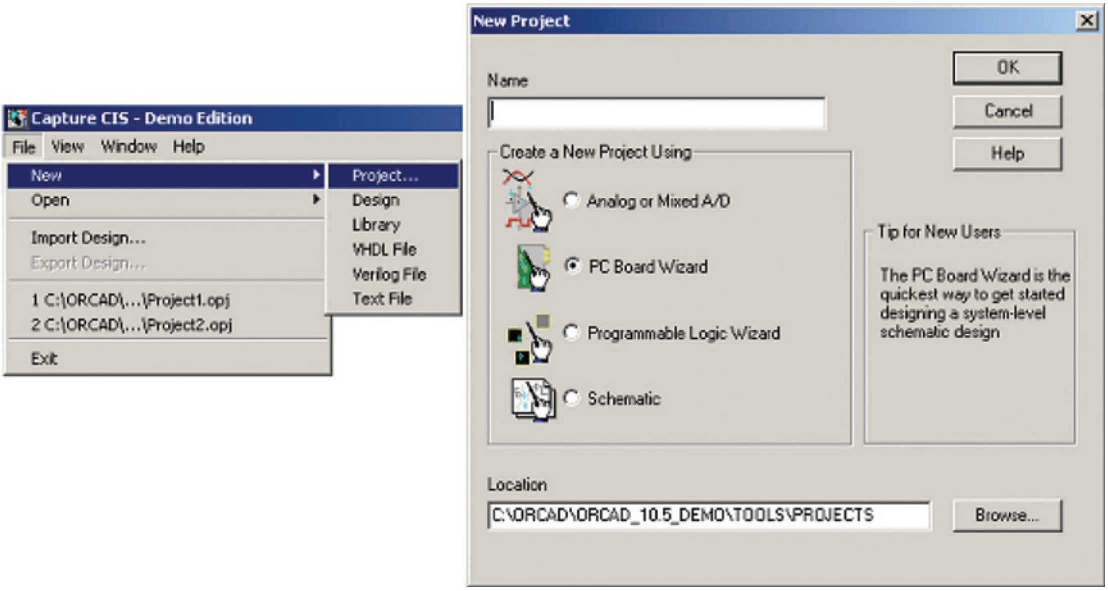
Reference	Value	Mounting/packaging	MFR	MFR P/N
J1	5-pin	Through-hole, 0–100-in. pin spacing	AMP/Tyco Electronics	3-643816-5
C1, C2	10uF	Through-hole, radial lead	Panasonic–ECG	ECS-F1VE106K
C3, C4	0.1uF	SMD, size 1206	Panasonic–ECG	ECJ-3YB2A104K
U1	LM741	SOIC-8	Texas Instruments	UA741CD
R1–R4	1k	SMD, size 1210 (¼ W)	Panasonic–ECG	ERJ-14NF xxxxU

Table 9-1 Basic parts list and mounting requirements

Project setup and design in Capture

Setting up the project

To begin a new design project start Capture and from the session window's File menu choose New → Project. At the New Project dialog box (Fig. 9-3) enter a name for the project.


Capture CIS - Demo Edition
File
View
Window
Help
New
Open
Import Design...
Export Design...
1 C:\ORCAD\...\Project1.opj
2 C:\ORCAD\...\Project2.opj
Exit
Project...
Design
Library
VHDL File
Verilog File
Text File
New Project
Name
OK
Cancel
Help
Create a New Project Using
○ Analog or Mixed A/D
● PC Board Wizard
○ Programmable Logic Wizard
○ Schematic
Tip for New Users
Location
Browse...

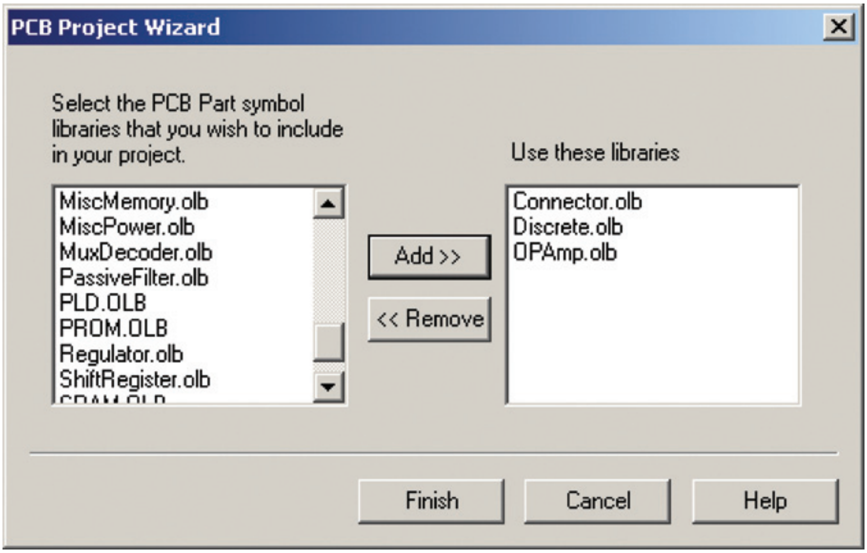
The PC Board Wizard is the quickest way to get started designing a system-level schematic design

Location: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS

Figure 9-3 Setting up a new project with the Project Wizard.

Select the PC Board Wizard radio button. You can also make PCB designs if you select the Analog or Mixed A/D button, which sets up PSpice simulation templates for the project. Since we will not be performing PSpice simulations in this example, PC Board Wizard will be used. Select the desired location for your project and then click OK.

At the next Project Wizard dialog box, do not enable project simulation, click Next. At the next dialog box add the Connector, Discrete, and OPAmp part libraries as shown in Fig. 9-4. To add a library select it (by clicking on it) in the left box and press the Add>> button. After you have added the libraries you want, click the Finish button.


PCB Project Wizard

Select the PCB Part symbol libraries that you wish to include in your project.

MiscMemory.olb
MiscPower.olb
MuxDecoder.olb
PassiveFilter.olb
PLD.OLB
PROM.OLB
Regulator.olb
ShiftRegister.olb

Use these libraries

Connector.olb
Discrete.olb
OPAmp.olb

Figure 9-4 Adding parts libraries to the project.

If you are using the Demo edition you will be shown an information box that says, “The Demo Edition does not support saving to a library with more than 15 parts....” Click OK each time it asks (you will need to click once for each library that you added to the project).

Drawing the schematic with Capture

Figure 9-5 shows the design goal. You can use it as a reference through the design example or modify it to your liking. If you are using the Demo version, remember that you cannot save a design in Layout that has more than 10 parts or parts with more than 14 pins. This design example meets these requirements so that you can save your work.

If a schematic page does not automatically open, expand the Design icon and the schematic folder in the Project Manager window, then double click the Page1 icon.

Placing parts

Before placing any parts onto the schematic page, make sure that the place grid is enabled. If parts are placed off-grid you will not be able to connect wires to the part’s pins. Use the

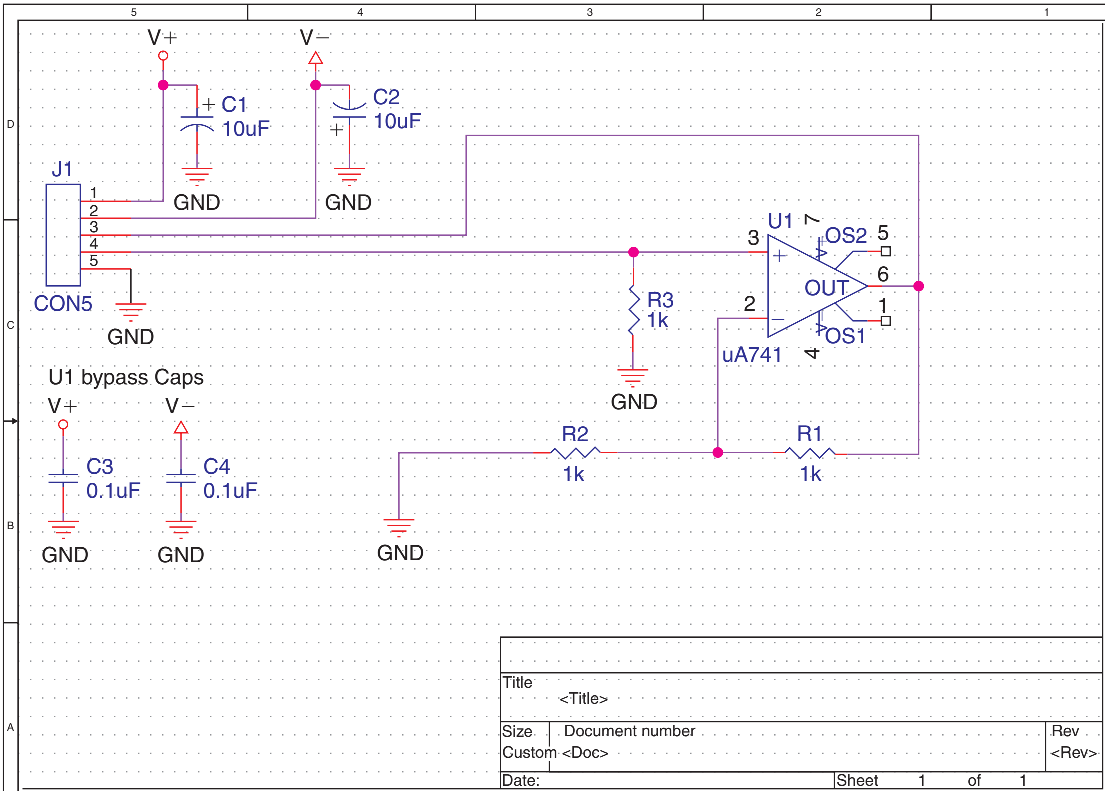

5
4
3
2
1
D
C
B
A
V+
V−
C1
10uF
C2
10uF
GND
GND
J1
1
2
3
4
5
CON5
GND
U1
7
3
OS2
5
6
OUT
2
1
OS1
uA741
4
R3
1k
GND
U1 bypass Caps
V+
V−
C3
0.1uF
C4
0.1uF
GND
GND
R2
1k
R1
1k
GND
Title
<Title>
Size
Custom
Document number
<Doc>
Rev
<Rev>
Date:
Sheet
1
of
1

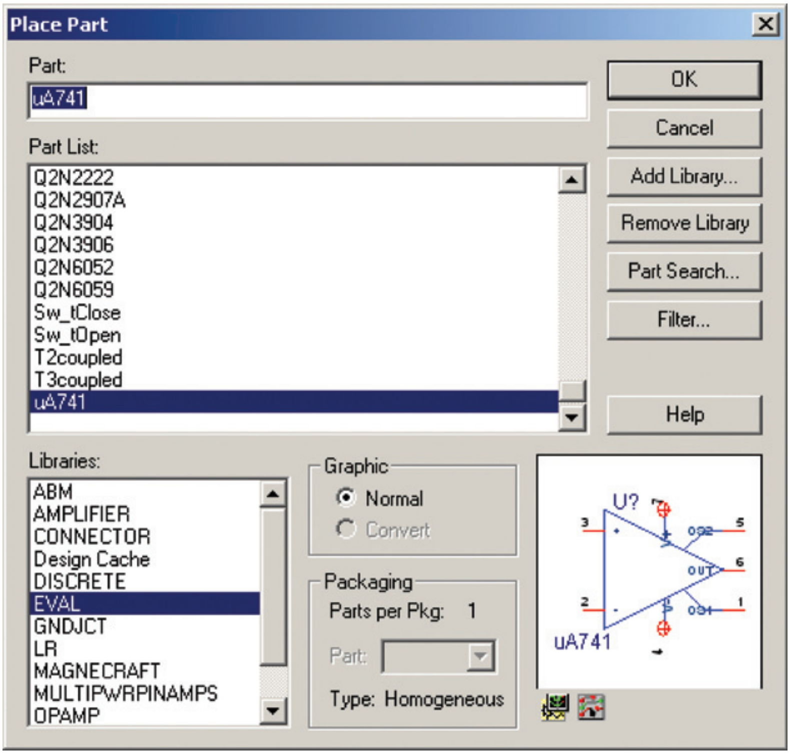
Figure 9-5 Analog circuit schematic design in Capture.

search tools described above to locate and place parts on the schematic page. Table 9-2 lists the parts used in this project and the libraries in which they are located.

Reference	Capture part	Capture library
J1	CON5	CAPTURE \ LIBRARY \ CONNECTOR.OLB
C1, C2	CAP POL	CAPTURE \ LIBRARY \ DISCRETE.OLB
C3, C4	CAP NP	CAPTURE \ LIBRARY \ DISCRETE.OLB
U1	uA741	CAPTURE \ LIBRARY \ PSPICE \ EVAL.OLB
	LM741	CAPTURE \ LIBRARY \ OPAMP.OLB
R1–R3	R	CAPTURE \ LIBRARY \ DISCRETE.OLB

Table 9-2 Capture library parts list

To place parts click the Place Part tool button, or select Part from the Place menu, or hit the P key on your keyboard. In the Place Part dialog box (see Fig. 9-6), select the OPAMP library or the EVAL library (your choice), and scroll down until you find the LM741 or the uA741 op-amp, respectively. Either one will work; it is just a matter of which one you



Place Part

Part: uA741

Part List:

Q2N2222
Q2N2907A
Q2N3904
Q2N3906
Q2N6052
Q2N6059
Sw_tClose
Sw_tOpen
T2coupled
T3coupled
uA741

Libraries:

ABM
AMPLIFIER
CONNECTOR
Design Cache
DISCRETE
EVAL
GNDJCT
LR
MAGNECRAFT
MULTIPWRPINAMPS
OPAMP

Graphic

● Normal
○ Convert

Packaging

Parts per Pkg: 1

Part:

Type: Homogeneous

*Figure 9-6 Choosing parts from the **Place Part** dialog box.*

prefer. You can place one of each, compare them, and then delete the one you do not like. If a library is not shown in the Libraries: box you can add it to the list as explained below. Once you find and select the part, click OK.

If a library is not displayed in the Libraries: window you will need to add it to the list. **To add a library to the Libraries: list in the Place Part dialog box**, click the Add Library... button on the Place Part dialog box (Fig. 9-6). Use the Browse File dialog box to locate the desired OLB library. For building schematics and PCB layouts you can use parts from either the main Capture library folder or the PSpice subfolder. If you are performing PSpice simulations, select parts only from the PSpice folder.

From the DISCRETE library place two polarized capacitors (CAP POL), two nonpolarized capacitors (CAP NP), and three resistors (R). From the CONNECTOR library, place a five-pin connector (CON5).

Connect parts with wires (signal nets)

To wire the circuit use the Place Wire tool, or select Wire from the Place menu, or hit W on your keyboard to activate the Wire tool. To attach wires between pins click once to start a wire, move the pointer to the next pin and click once to attach the wire and continue routing or double click to end the wire. Connect the circuit as shown in Fig. 9-5.

Making power and ground connections

There are three ways of adding power connections to active parts depending on what type of power supply pins the part has. A part's power supply pin can be a power-type pin and nonvisible, or a power-type pin and visible, or a nonpower-type pin (such as a passive or an input pin), which is always visible. The term "visible" specifically refers to whether the pin is visible to the Wire tool. However, in the general case, a nonvisible pin is also invisible from the user's perspective. Digital parts typically have nonvisible power pins, while analog parts—particularly op-amps—commonly use either visible power pins or one of the nonpower-type pins (which are always visible).

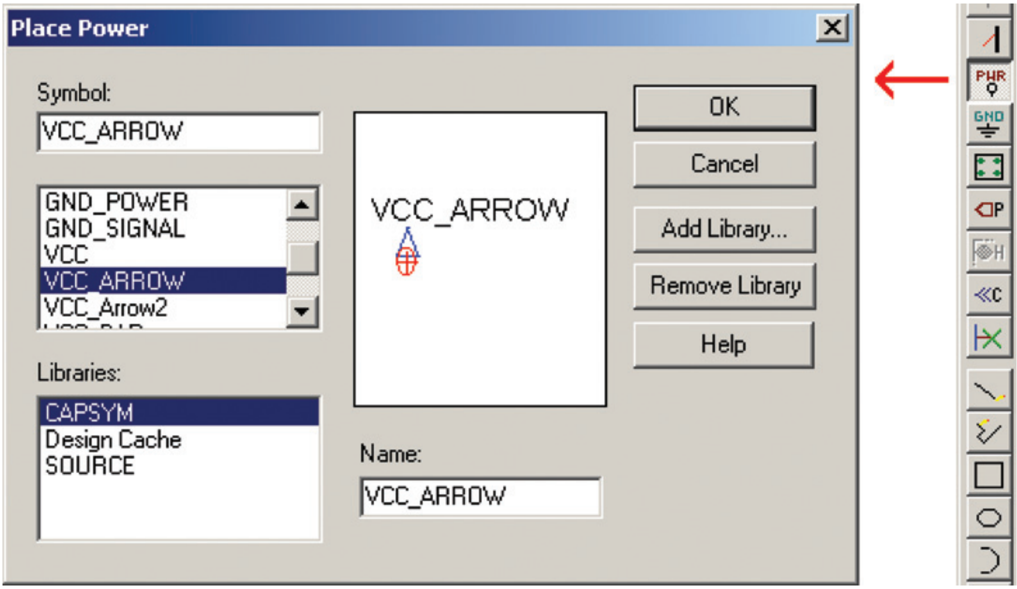
If a part's power supply pin is a power pin and is *not* visible you cannot connect a wire (a net) to it directly. A nonvisible power pin *is* a net and it is global. You connect a part's power pin to a power symbol by giving the pin and the power symbol the same name. To make the connection, you will need to place a power symbol, which is also global, somewhere on the schematic. Power symbols are always visible and are wired to either an off-board connector or a PSpice power supply. To make the names the same you can change the name of the power symbol, or the power pin, or both. An example of how to do this is given below.

If a power supply pin is a power pin, and it is visible, you can either take advantage of the power pin's global properties using power symbols or make direct connections to it with wires. If you use the pin's global nature, the pin name and the power symbol name must be the same as described above. If you make a direct connection to the power pin with a wire you do not have consider the naming convention. If you have a multipart package (e.g., a quad op-amp with shared power pins) all of the parts within the package that are placed on a schematic must have their power supply pins connected in the same way. So either they must all be global or they must all have wires connected to them.

If a part's power supply pin is a not a power pin, you must use a wire to connect the pin to some other object such as a power symbol or an off-board connector. If you place more than one part from a multipart package that has nonpower-type power pins, connections need to be made to only one of the part's power supply pins (although you can make connections to all of them if you want). See Chap. 7 for more information on pin types.

The 741 op-amp used in this example has visible power supply pins, so we will make use of their global properties by using power supply symbols to make connections to the off-board connector. Whether you used the LM741 from the OPAMP library or the uA741 from the EVAL library, the power supply pins are both visible power pins. The difference in their appearances is that the uA741 has zero-length power pins and the LM741 has line-length power pins. A zero-length pin is still "visible" to the Wire tool, but not to the user.

To place power symbols click the Place Power tool button and select one of the power supply symbols (VCC in this example) from the Place Power dialog box as shown in Fig. 9-7. Click OK and place the symbol onto the schematic.



Place Power

Symbol: VCC_ARROW

Libraries: CAPSYM

Name: VCC_ARROW

Figure 9-7 Placing global power symbols.

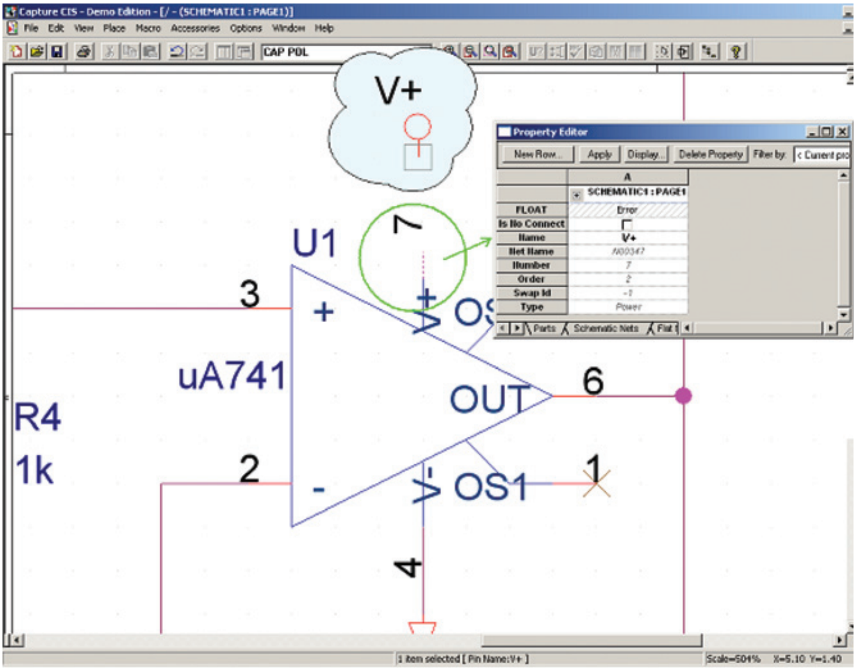
The names of the power pins on the op-amp and the names of the power symbols must be the same. You can change the name of the symbol or the pin or both. Some parts do not have visible labels for their power pins. **To check a pin's name and type** select the pin (if it is visible), right click, and select properties at the pop-up to get a Property Editor dialog box for the pin (see Fig. 9-8).

To change the name or type of a nonvisible power pin, select the part on the schematic, right click, and select Edit Part from the pop-up. You will be given a Capture Part Editor window (see Fig. 9-9). Double click the pin you want to change the name of to bring up the Pin Properties dialog box as shown in Fig. 9-9. Enter the new name in the Name: text box and click OK. Repeat the process for the other power supply pin.

Close the Part Editing window. Click Update Current when Capture asks you, "Would you like to update only the part instance being currently edited, or all part instances in the design?" In this case, since there is only one uA741, it does not matter if you click Update Current or Update All. But if you had several uA741's and you did not want all of them to have their power pin names changed you would click Update Current.

Note

- *When you change a part on the schematic the link between the design cache and the part library is broken. See the section at the end of the chapter for details on managing the design cache.*


Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PAGE1)]
File
Edit
View
Place
Macro
Accessories
Options
Window
Help
CAP POL
V+
U1
7
3
+
+
V
OS
uA741
OUT
6
R4
1k
2
-
V-
OS1
1
4
Property Editor
New Row...
Apply
Display...
Delete Property
Filter by:
< Current pro
Parts
Schematic Nets
Flat

	A
	SCHEMATIC1 : PAGE1
FLOAT	Error
Is No Connect	☐
Name	V+
Net Name	N00347
Number	7
Order	2
Swap Id	-1
Type	Power

1 item selected [Pin Name:V+]

Scale=504%   X=5.10 Y=1.40

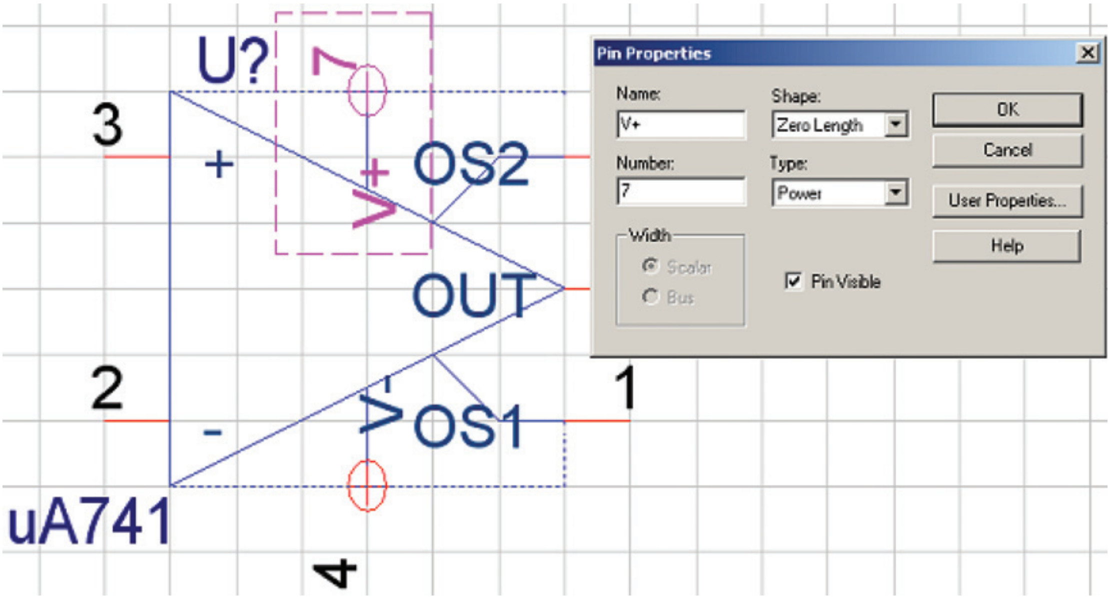
Figure 9-8 Determining a power pin's type and name.

Instead of changing the name of the power pin on the part you can change the name of the power supply symbol. **To change the name of the** power supply **symbol**, double click the symbol's name on the schematic. The Display Properties dialog box will pop up as shown in Fig. 9-10. The op-amp's positive power supply pin name is V+, so enter V+ in the Value: text box and then click OK. Place another power supply symbol and change its name to V− using the same procedure. Copy, place, and connect the V+ and V− power symbols as shown in Fig. 9-5.

Next, add a ground symbol. **To place a ground symbol** click the Place Ground tool button, GND and select one of the ground symbols from the Place Ground dialog box. Click OK and place the symbol onto the schematic. Place and connect ground symbols as shown in Fig. 9-5.

Note

- *For designs that will be simulated with PSpice you must use a GND symbol named "0" for the circuit to simulate correctly. You can use any of the symbols as long as they have the name "0". For PCB designs that will not be simulated you can use any of the GND symbols and name them whatever you want. A separate net will be instantiated for each distinct GND name. See Examples 2 and 3 for techniques on how to establish multiple GND systems.*


U?
7
3
+
V+
OS2
OUT
2
-
V-
OS1
1
uA741
4
Pin Properties
OK
Cancel
User Properties...
Help

Name: V+

Number: 7

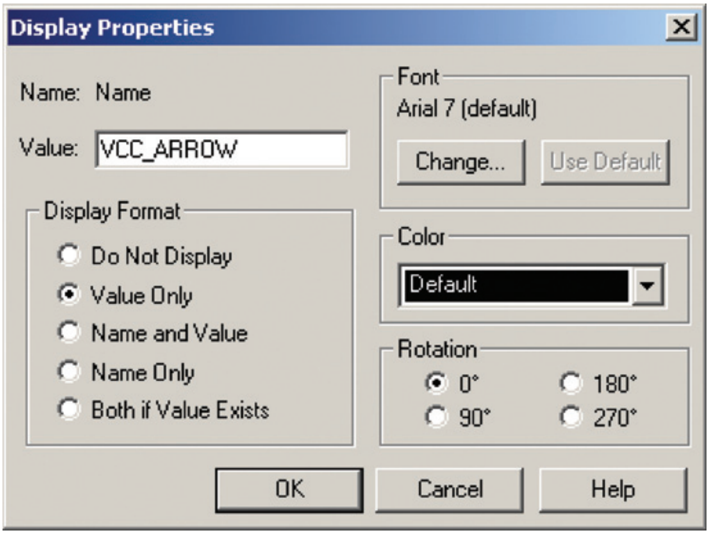
Shape: Zero Length

Type: Power

Width
● Scalar
○ Bus

☑ Pin Visible

Figure 9-9 Use the Part Editor to change a pin's name or type.


Display Properties
Change...
Use Default
OK
Cancel
Help

Name: Name

Value: VCC_ARROW

Display Format
○ Do Not Display
● Value Only
○ Name and Value
○ Name Only
○ Both if Value Exists

Font
Arial 7 (default)

Color
Default

Rotation
● 0°
○ 90°
○ 180°
○ 270°

*Figure 9-10 Use the **Display Properties** dialog box to change a power symbol's name.*

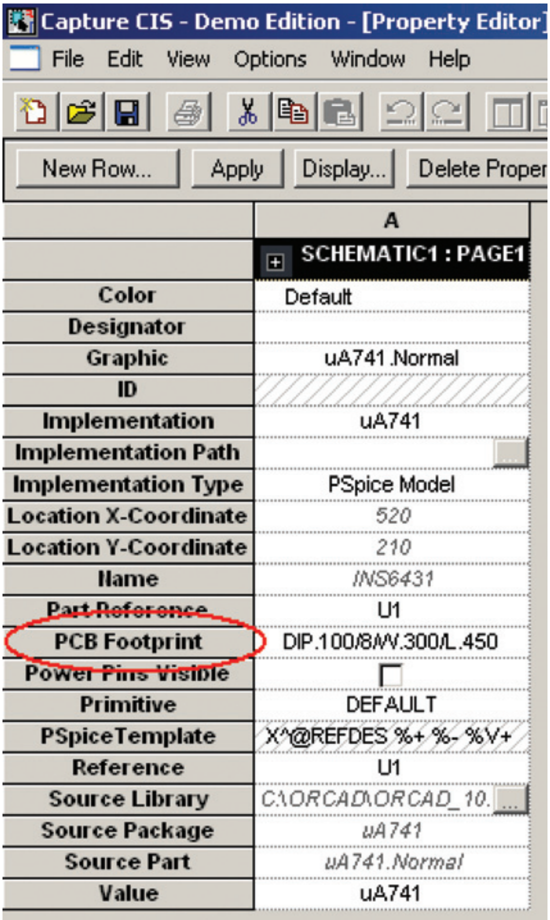
Preparing the design for Layout

Once all of the connections have been made, the next step is to prepare the design for making a Layout netlist.

Things to do:

- Make sure all of the footprints are assigned.
- Assign parts to groups.
- Perform an annotation.
- Clean up the design cache.
- Perform a DRC in Capture.

There are several ways to find out which (if any) parts have footprints assigned to them and if they are the right ones. You can check each part one at a time by double clicking a part to bring up the properties spreadsheet and look at the PCB Footprint cell as shown in Fig. 9-11.



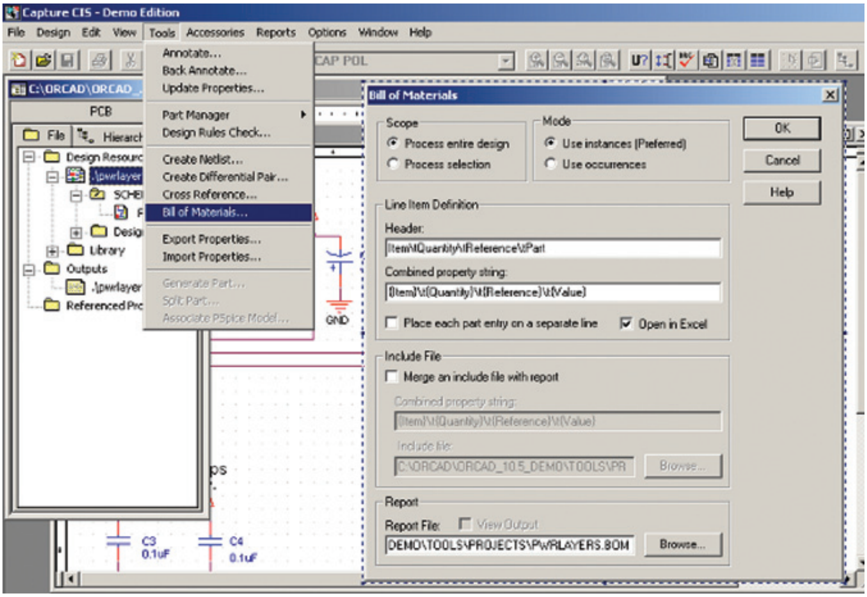
	A
	SCHEMATIC1 : PAGE1
Color	Default
Designator	
Graphic	uA741.Normal
ID	
Implementation	uA741
Implementation Path	
Implementation Type	PSpice Model
Location X-Coordinate	520
Location Y-Coordinate	210
Name	INS6431
Part Reference	U1
PCB Footprint	DIP.100/8/W.300/L.450
Power Pins Visible	☐
Primitive	DEFAULT
PSpiceTemplate	X^@REFDES %+ %- %V+
Reference	U1
Source Library	C:\ORCAD\ORCAD_10.
Source Package	uA741
Source Part	uA741.Normal
Value	uA741

Figure 9-11 Part properties spreadsheet.

Or you can check all of the parts at the same time by selecting all of the parts in the schematic (drag a box across the schematic using the left mouse button), then right click and select Edit Properties... from the pop-up. The spreadsheet will show the properties of all the parts that were selected. To toggle the spreadsheet view between the column and row organization right click the upper left corner or the spreadsheet and select Pivot from the pop-up.

The spreadsheet method is fast and easy for small circuit designs, but it may be impractical for large circuits. An alternative is to generate a customized BOM that lists all of the footprints in an Excel spreadsheet. The spreadsheet can be printed and used as a reference while you are searching through Layout's footprint libraries for the right footprints.

To generate the custom BOM go to the Project Manager, select the Design icon, and then select Bill of Materials... from the Tools menu (see Fig. 9-12). At the Bill of Materials dialog box add the text "\tFootprint" in the text box labeled Header:, and add the text "\t{PCB Footprint}" in the text box labeled Combined property string:. Put a check mark in the Open in Excel box. You can specify the location and name of the BOM using the Browse... button at the bottom. Click OK when you have finished the setup. For additional information on using Excel with a BOM see Chap. 11.


Capture CIS - Demo Edition
File
Design
Edit
View
Tools
Accessories
Reports
Options
Window
Help
Annotate...
Back Annotate...
Update Properties...
Part Manager
Design Rules Check...
Create Netlist...
Create Differential Pair...
Cross Reference...
Bill of Materials...
Export Properties...
Import Properties...
Generate Part...
Split Part...
Associate PSpice Model...
CAP POL
C:\ORCAD\ORCAD_
PCB
File
Hierarch
Design Resourc
.\pwrlayer
SCHE
Desig
Library
Outputs
.\pwrlayer
Referenced Pro
GND
C3
0.1uF
C4
0.1uF
Bill of Materials
OK
Cancel
Help
Browse...
Browse...

Scope
● Process entire design
○ Process selection

Mode
● Use instances (Preferred)
○ Use occurences

Line Item Definition

Header: Item\tQuantity\tReference\tPart

Combined property string: {Item}\t{Quantity}\t{Reference}\t{Value}

☐ Place each part entry on a separate line ☑ Open in Excel

Include File

☐ Merge an include file with report

Combined property string: {Item}\t{Quantity}\t{Reference}\t{Value}

Include file: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PR

Report

Report File: ☐ View Output

DEMO\TOOLS\PROJECTS\PWRLAYERS.BOM

Figure 9-12 Generating a bill of materials to include PCB footprints.

The left side of Table 9-3 shows a BOM. The BOM shows that none of the parts have the correct footprint assigned to them. The column on the right of Table 9-3 shows the correct Layout footprints and their libraries (compare with Table 9-1). Note that the right column was not produced by the BOM, but it is shown next to it for ease of identifying which footprints belong with which part.

Bill of materials				
Reference	**Value**	**Capture part**	**Default footprint**	**Layout library: footprint**
J1	3-pin	CON5		BCON100T: BLKCON.100/VH/TM1SQS/W.100/5
C1, C2	0.1uF	CAP POL		TM_RAD: RAD/.100X.100/LS.100/.031
C3, C4	0.1uF	CAP NP		SM.LLB: SMIC_1206
U1	x741	uA741	DIP.100/8/W.300/L.450	SOG.LLB: SOG.050/8/WG.244/L200
R1–R4	1k	R		SM.LLB: SM/R_1210

Table 9-3 Bill of materials spreadsheet and available layout footprints

The next step then is to assign footprints to the components. The easiest way to find the desired footprint is by using the Footprint Library Manager in Layout.

To find footprints in Layout's footprint libraries open Layout and, from the session frame, select Library Manager from the Tools menu. Once you find the footprint in the Library Manager, select it so that it is visible in the editing/viewing window, then copy (using Ctrl + C) its name from the Footprints text box as shown in Fig. 9-13. See Table 8-1 and Fig. 8-2 for naming conventions to make it easier to find footprints.

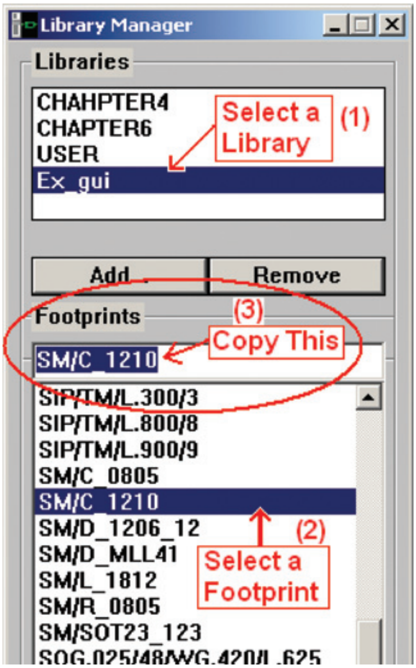
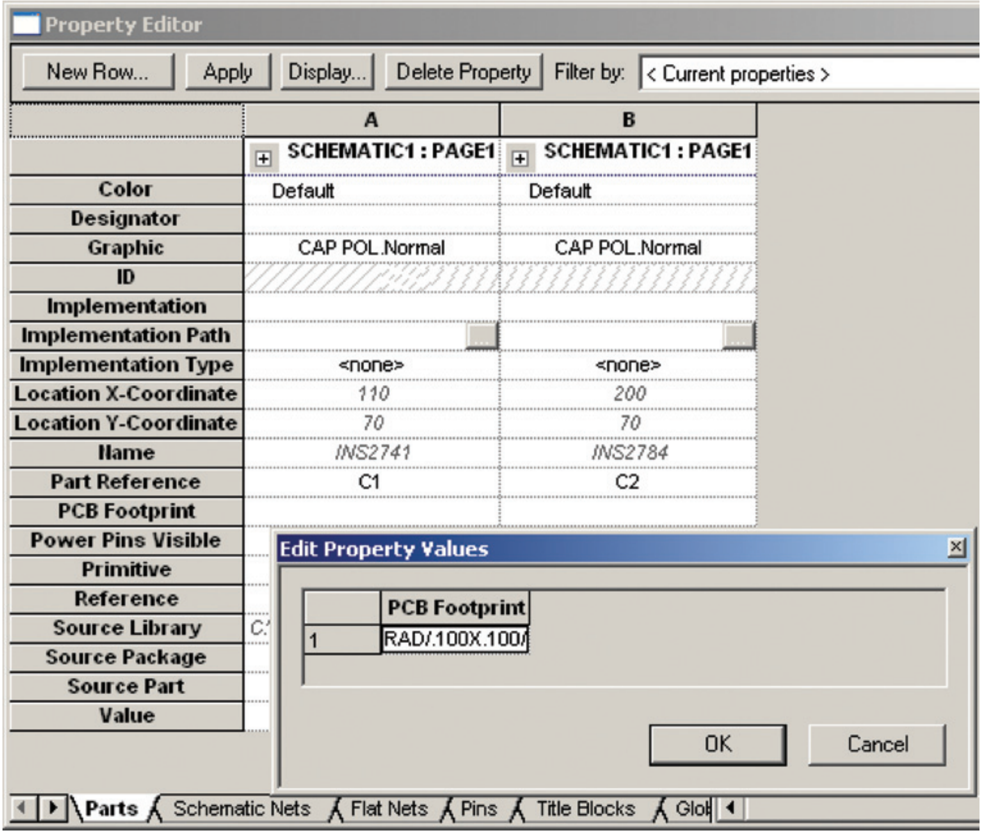

Library Manager
Libraries
CHAHPTER4
CHAPTER6
USER
Ex_gui
Select a Library
(1)
Add...
Remove
Footprints
(3)
Copy This
SM/C_1210
SIP/TM/L.300/3
SIP/TM/L.800/8
SIP/TM/L.900/9
SM/C_0805
SM/C_1210
SM/D_1206_12
SM/D_MLL41
SM/L_1812
SM/R_0805
SM/SOT23_123
SOG.025/48/WG.420/L.625
(2)
Select a Footprint

Figure 9-13 Find and copy the name of the footprint in Layout.

Go back to Capture. **To assign the footprint to a part** display the properties spreadsheet for the part to which you want to assign the footprint (double click the part to display its properties spreadsheet). Paste the footprint name into the PCB Footprint cell in the properties spreadsheet (see Fig. 9-11).

If there are several parts that have the same footprint (the capacitors and resistors, for example) you can change all of them at the same time. **To assign a footprint to multiple parts simultaneously**, hold down the Ctrl key on your keyboard while you select each component, right click, and select Edit Properties... from the pop-up. Select the PCB Footprint column (or row if the spreadsheet is pivoted) to select all of the PCB footprint cells and then right click and select Edit... from the pop-up to display the Edit Property Values minispreadsheet shown in Fig. 9-14. Paste the footprint name that you copied from Layout into the PCB Footprint cell and then click OK. Once you have all of the footprints assigned you can generate another bill of materials so that you can see all of the footprints at the same time to make sure you have not missed any. Figure 9-15 shows the final BOM listing with all of the footprints assigned.

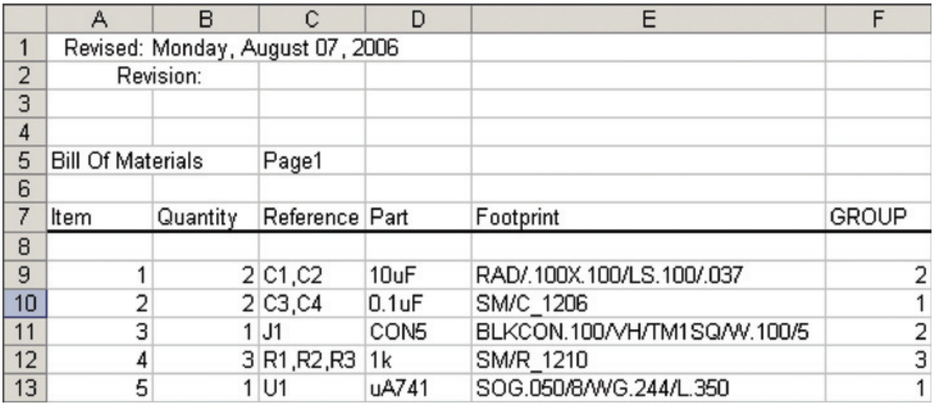


Filter by: < Current properties >

	A	B
	SCHEMATIC1 : PAGE1	SCHEMATIC1 : PAGE1
Color	Default	Default
Designator		
Graphic	CAP POL.Normal	CAP POL.Normal
ID		
Implementation		
Implementation Path		
Implementation Type	<none>	<none>
Location X-Coordinate	110	200
Location Y-Coordinate	70	70
Name	INS2741	INS2784
Part Reference	C1	C2
PCB Footprint		
Power Pins Visible		
Primitive		
Reference		
Source Library	C:	
Source Package		
Source Part		
Value		

	PCB Footprint
1	RAD/.100X.100/

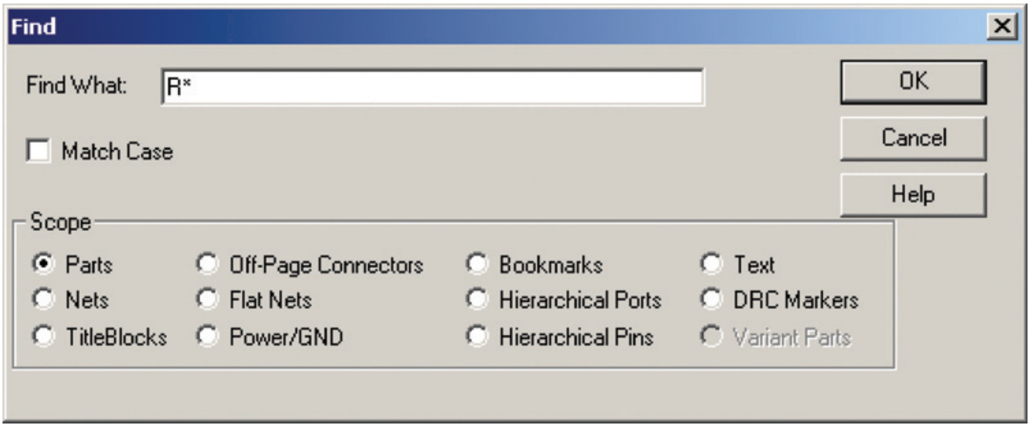
Figure 9-14 Assigning footprints to multiple parts with the Property Editor.



	A	B	C	D	E	F
1	Revised: Monday, August 07, 2006					
2	Revision:					
3						
4						
5	Bill Of Materials		Page1			
6						
7	Item	Quantity	Reference	Part	Footprint	GROUP
8						
9	1	2	C1,C2	10uF	RAD/.100X.100/LS.100/.037	2
10	2	2	C3,C4	0.1uF	SM/C_1206	1
11	3	1	J1	CON5	BLKCON.100/VH/TM1SQ/W.100/5	2
12	4	3	R1,R2,R3	1k	SM/R_1210	3
13	5	1	U1	uA741	SOG.050/8/WG.244/L.350	1

Figure 9-15 Final BOM listing with all footprints assigned.

You can also use the Find tool to automatically select a part or parts of a certain type. To use the Find tool select Find from the Edit menu; the Find dialog box will be displayed as shown in Fig. 9-16. If you enter R1 in the Find What: text box R1 will be highlighted on the schematic and centered on the screen. If you enter R* then all resistors will be selected. You can use the Find tool to look for other things, such as text and nets, as indicated in Fig. 9-16.



Find What: R*

☐ Match Case

Scope

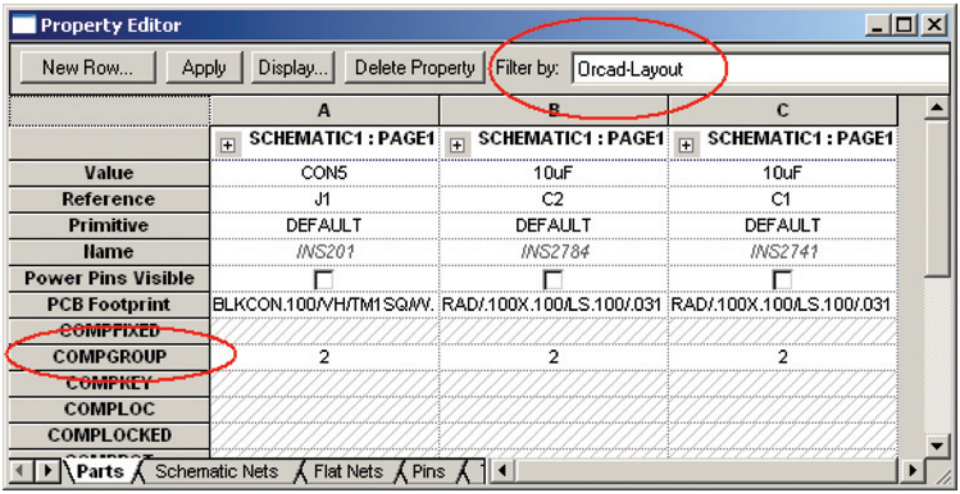
● Parts ○ Off-Page Connectors ○ Bookmarks ○ Text
○ Nets ○ Flat Nets ○ Hierarchical Ports ○ DRC Markers
○ TitleBlocks ○ Power/GND ○ Hierarchical Pins ○ Variant Parts

Figure 9-16 Using the Find tool to locate parts.

Grouping related components

Grouping related components in the schematic can make placing the parts easier in Layout. Parts are assigned a group number in Capture, and the grouping information is exported to Layout through the .MNL file during the AutoECO process. **To add parts to a group** select the related parts (e.g., J1 and the two filter caps) on the schematic. Right click and select Edit

Properties from the pop-up to display the Property Editor spreadsheet (see Fig. 9-17). In the Filter by: dropdown list select OrCAD-Layout. Select the COMPGROUP cell to select that property for all of the components and then right click and select Edit from the pop-up. In the Edit Property Values dialog box assign an integer number for the group (this will be the Group # that Layout uses). Click OK to close the dialog box. The integer value will be assigned to all of the parts you selected. Close the spreadsheet.

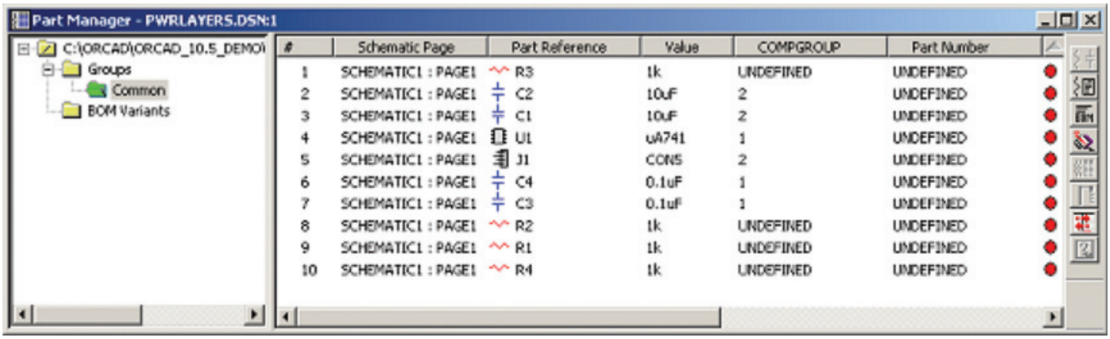


Filter by: Orcad-Layout

	A	B	C
	SCHEMATIC1 : PAGE1	SCHEMATIC1 : PAGE1	SCHEMATIC1 : PAGE1
Value	CON5	10uF	10uF
Reference	J1	C2	C1
Primitive	DEFAULT	DEFAULT	DEFAULT
Name	INS201	INS2784	INS2741
Power Pins Visible	☐	☐	☐
PCB Footprint	BLKCON.100/VH/TM1SQ/W.	RAD/.100X.100/LS.100/.031	RAD/.100X.100/LS.100/.031
COMPFIXED			
COMPGROUP	2	2	2
COMPKEY			
COMPLOC			
COMPLOCKED			

Figure 9-17 Using the Property Editor to assign components to groups.

To view group information for the entire design go to the Project Manager and select the Design icon. Right click and select Part Manager from the pop-up (or select Part Manager → Open from the Tools menu). The Part Manager is shown in Fig. 9-18.



#	Schematic Page	Part Reference	Value	COMPGROUP	Part Number
1	SCHEMATIC1 : PAGE1	R3	1k	UNDEFINED	UNDEFINED
2	SCHEMATIC1 : PAGE1	C2	10uF	2	UNDEFINED
3	SCHEMATIC1 : PAGE1	C1	10uF	2	UNDEFINED
4	SCHEMATIC1 : PAGE1	U1	uA741	1	UNDEFINED
5	SCHEMATIC1 : PAGE1	J1	CON5	2	UNDEFINED
6	SCHEMATIC1 : PAGE1	C4	0.1uF	1	UNDEFINED
7	SCHEMATIC1 : PAGE1	C3	0.1uF	1	UNDEFINED
8	SCHEMATIC1 : PAGE1	R2	1k	UNDEFINED	UNDEFINED
9	SCHEMATIC1 : PAGE1	R1	1k	UNDEFINED	UNDEFINED
10	SCHEMATIC1 : PAGE1	R4	1k	UNDEFINED	UNDEFINED

Figure 9-18 Using the Part Manager to view all groups.

If you do not see the COMPGROUP properties in the Part Manager, you can add it by selecting the Configure Part Properties Display option from the View menu. Select the COMPGROUP property icon and click the Add → button as shown in Fig. 9-19. You can use the ↑ and ↓ buttons on the right side of the dialog box to specify what order the properties are displayed in the Part Manager. Once you have added the properties you want to see, click OK. The parts should now be displayed in the Part Manager (Fig. 9-18).

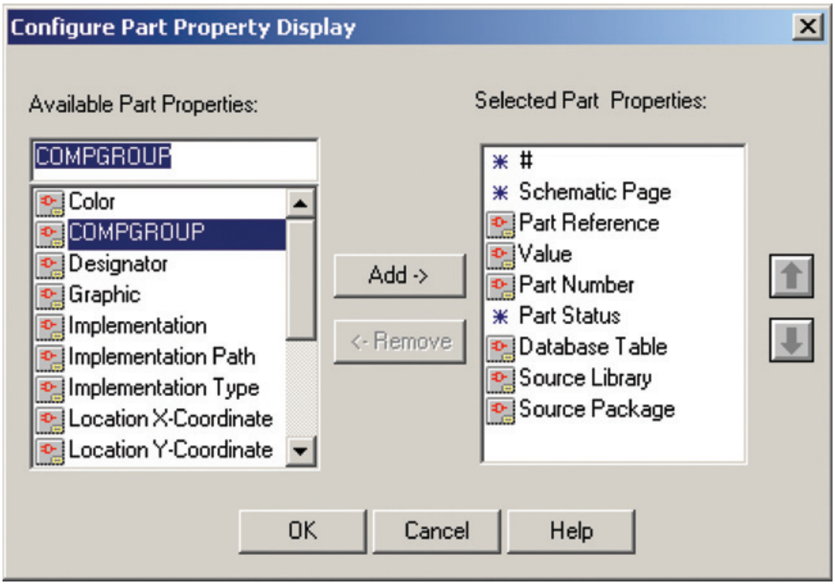

Configure Part Property Display
Available Part Properties:
COMPGROUP
Color
COMPGROUP
Designator
Graphic
Implementation
Implementation Path
Implementation Type
Location X-Coordinate
Location Y-Coordinate
Add ->
<- Remove
Selected Part Properties:
#
Schematic Page
Part Reference
Value
Part Number
Part Status
Database Table
Source Library
Source Package
OK
Cancel
Help

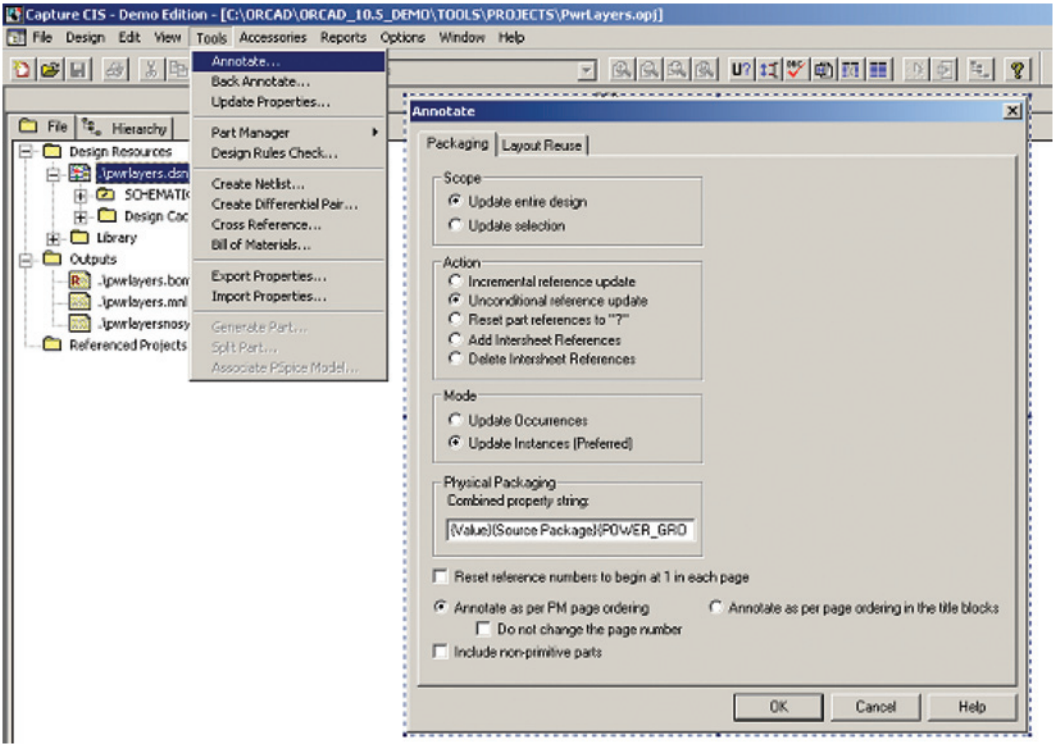
*Figure 9-19 The **Configure Part Property Display** dialog box.*

You can also add the COMPGROUP property to the bill of materials listing by adding "\tCOMPGROUP" to the Header: list and "\t{COMPGROUP}" to the Combined Property String list (see Chap. 11 for details).

Before making the netlist you should tidy up the design by performing an annotation, cleaning up the design cache, and performing a DRC.

Annotation

Performing an annotation chronologically renumbers the part references in your schematic design from top to bottom. **To perform an annotation**, go to the Project Manager and select Annotate from the Tools menu. The Annotate dialog box shown in Fig. 9-20 is displayed. Select the items you want updated and then click OK. Be sure to check multi part components (hex inverters for example) to make sure that they are annotated correctly.


Capture CIS - Demo Edition - [C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\PwrLayers.opj]
File
Design
Edit
View
Tools
Accessories
Reports
Options
Window
Help
Annotate...
Back Annotate...
Update Properties...
Part Manager
Design Rules Check...
Create Netlist...
Create Differential Pair...
Cross Reference...
Bill of Materials...
Export Properties...
Import Properties...
Generate Part...
Split Part...
Associate PSpice Model...
File
Hierarchy
Design Resources
.\pwrlayers.dsn
SCHEMATIC
Design Cac
Library
Outputs
.\pwrlayers.bom
.\pwrlayers.mnl
.\pwrlayersnosy
Referenced Projects
Annotate
Packaging
Layout Reuse
OK
Cancel
Help

Scope
● Update entire design
○ Update selection

Action
○ Incremental reference update
● Unconditional reference update
○ Reset part references to "?"
○ Add Intersheet References
○ Delete Intersheet References

Mode
○ Update Occurrences
● Update Instances (Preferred)

Physical Packaging
Combined property string:
{Value}{Source Package}{POWER_GRD

☐ Reset reference numbers to begin at 1 in each page

● Annotate as per PM page ordering
○ Annotate as per page ordering in the title blocks
☐ Do not change the page number
☐ Include non-primitive parts

Figure 9-20 Performing a design annotation.

Warning!

- *Do not perform another annotation after you have generated a Layout netlist or performed a back annotation from Layout (especially if you had Layout renumber the parts), because the project can become unsynchronized and produce very peculiar, irreversible results! To read more about the annotation function, search for "Annotate dialog box" in the Capture User's Guide.*

Cleanup Cache removes unused parts from the design cache. Unused parts pile up in the design cache when you place parts in the design but then later delete them. **To clean up the design cache** select the Design Cache folder in the Project Manager, right click, and select Cleanup Cache from the pop-up or select Cleanup Cache from the Design menu (see Design cache—cleanup, replace, update at the end of the chapter for information on the Update and Replace Cache commands).

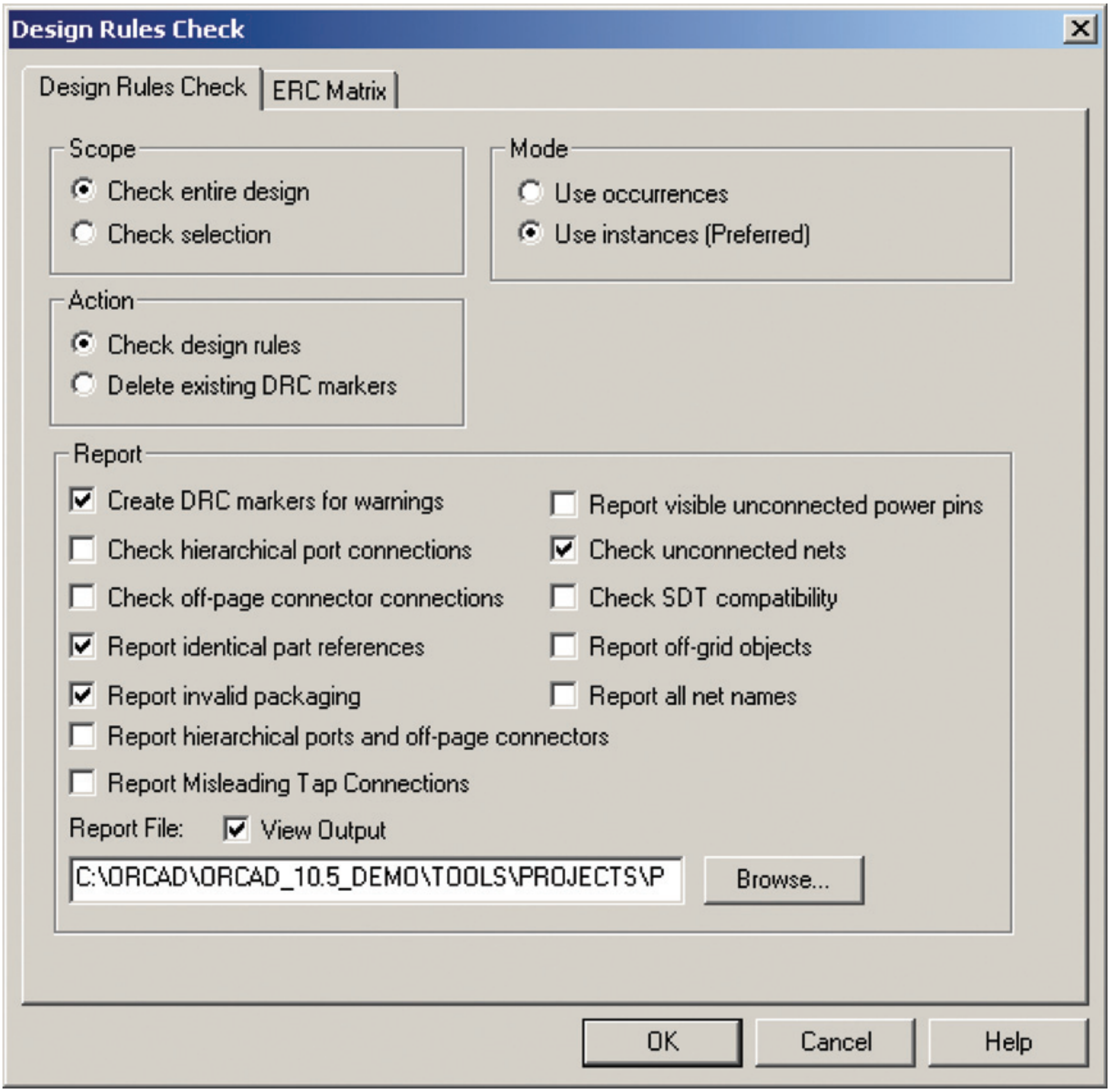
Performing a schematic DRC in Capture

It is a good idea to run a DRC before generating a netlist. The DRC checks your design for design rule violations and places error markers on the schematic page. **To perform a DRC**

in a Capture project make the Project Manager window active. From the Tools menu select Design Rules Check.... The Design Rules Check dialog box is displayed as shown in Fig. 9-21. Select the items you want to check and click OK. If you have errors you can search for the markers by using the Browse DRC Markers command from the Project Manager's Edit menu or from the Find option on the schematic's Edit menu.

Generating the Layout netlist (.MNL)

Once you have all of your connections finished and footprints and groups assigned, etc., you can create the .MNL netlist for Layout. **To create a netlist for Layout**, select the Design



Scope
● Check entire design
○ Check selection

Mode
○ Use occurrences
● Use instances (Preferred)

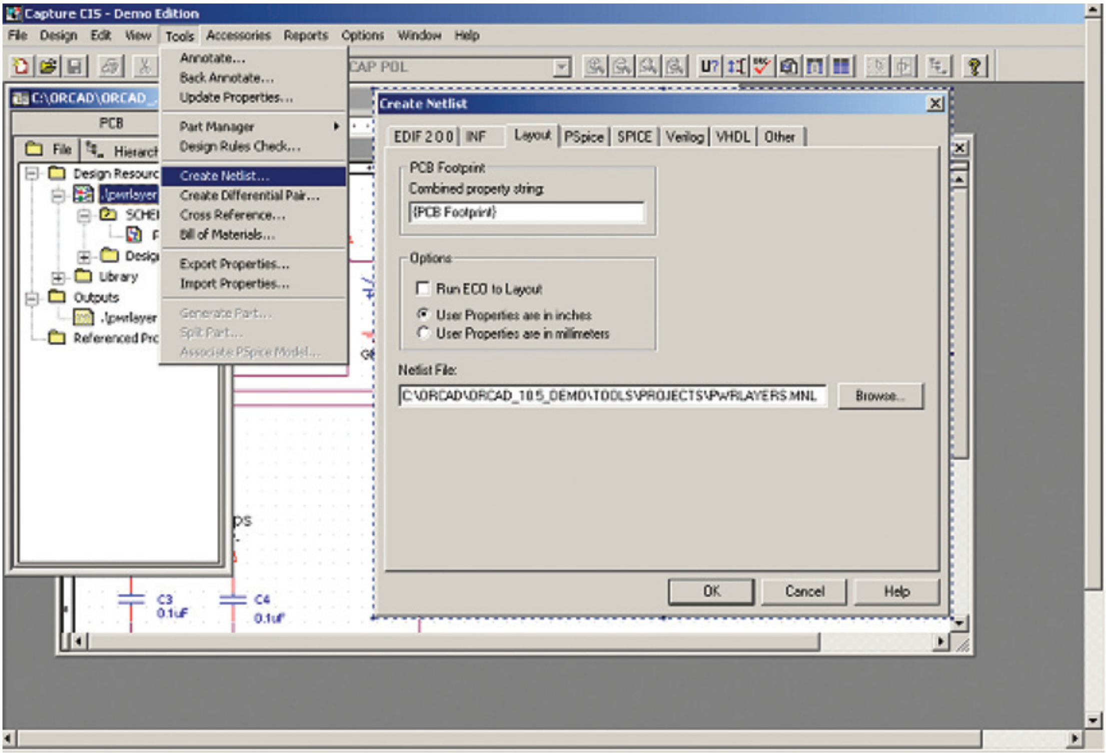
Action
● Check design rules
○ Delete existing DRC markers

Report
☑ Create DRC markers for warnings
☐ Report visible unconnected power pins
☐ Check hierarchical port connections
☑ Check unconnected nets
☐ Check off-page connector connections
☐ Check SDT compatibility
☑ Report identical part references
☐ Report off-grid objects
☑ Report invalid packaging
☐ Report all net names
☐ Report hierarchical ports and off-page connectors
☐ Report Misleading Tap Connections

Report File: ☑ View Output
C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\P

Figure 9-21 The Capture *Design Rules Check* dialog box.

icon in the Project Manager and select Create Netlist... from the Tools menu. In the Create Netlist dialog box (see Fig. 9-22) select the Layout tab and specify a netlist name or accept the default .MNL name. For new designs you can leave the Run ECO to Layout box unchecked (this is used to update an existing board design with new information from Capture). Click OK. For the time being, that completes your work in Capture. It is best to leave the Capture Project open while you work in Layout because Capture and Layout communicate with each other in real time (referred to as intertool communication). This will be demonstrated below.


Capture CIS - Demo Edition
File Design Edit View Tools Accessories Reports Options Window Help
Annotate...
Back Annotate...
Update Properties...
Part Manager
Design Rules Check...
Create Netlist...
Create Differential Pair...
Cross Reference...
Bill of Materials...
Export Properties...
Import Properties...
Generate Part...
Split Part...
Associate PSpice Model...
CAP PDL
C:\ORCAD\ORCAD_
PCB
File
Hierarch
Design Resourc
.\pwrlayer
SCHE
Desig
Library
Outputs
.\pwrlayer
Referenced Pro
C3
0.1uF
C4
0.1uF
Create Netlist
EDIF 2 0 0
INF
Layout
PSpice
SPICE
Verilog
VHDL
Other
Browse...
OK
Cancel
Help

PCB Footprint

Combined property string: {PCB Footprint}

Options

☐ Run ECO to Layout

● User Properties are in inches

○ User Properties are in millimeters

Netlist File: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\PWRLAYERS.MNL

Figure 9-22 Creating a circuit netlist for Layout from Capture.

Defining the board requirements

One of the first steps in setting up a new board in Layout is to select a technology file, which requires deciding on a couple of design requirements up front. Choosing a technology file requires knowing what types of parts will be used in the design (packaging and assembly requirements), the number and type of layers required, and the trace width and spacing requirements. These considerations for the analog design example are discussed in the following sections.

Specifying packaging and assembly requirements

Table 9-1 lists the parts that will be used in this design. As indicated both surface-mount and through-hole components will be used, and the eight-pin SOIC has the smallest lead pitch.

This design constraint is annotated in Table 9-5 and will be considered with the other design constraints when choosing the technology file.

Defining the layer stack-up

The op-amp used in this example requires a dual rail supply and at least one ground plane. At least two routing layers will also be needed (unless jumpers are used). Therefore a minimum of five layers is required. Since most multilayer boards are made up of double-sided cores (and therefore usually have an even number of layers) we will use the extra layer as an additional ground plane. There are several different ways the layers could be stacked up (see Chap. 6 for other examples). The stack-up shown Fig. 9-23 will be used in this example because it will provide the opportunity to demonstrate two different methods for defining plane layers.

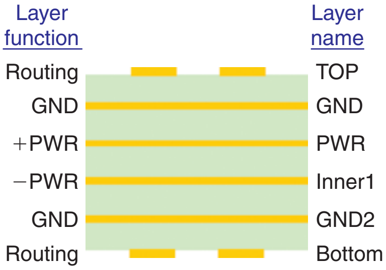


Figure 9-23 Layer stack-up for Example 1.

Determining trace width

Trace width depends on two design considerations. The first consideration is the required current handling capability and the second is the impedance. According to the data sheet, the short circuit output current for the uA741 op-amp is ±40mA. If we use a safety margin of, say, 100 mA and we are using a board with 1 oz copper, then per Eq. (17) in Chap. 6 (or graph from Fig. 6-38), the minimum trace width is 1.3 mils for inner layers and 0.5 mils for outer layers. Since all of the technology files shown in Table 9-4 have trace widths 6 mils or wider, we can use any of the standard technologies as far as trace width is concerned. From Table 6-8

Technology files (*.TCH)	Design complexity level/class	Trace width (mils)	Route spacing (mils)	Default layers	
				Route	Plane
default	A	12	12	12	2
1 bet_ any	A	12	12	12	2
metric	B	10	10	12	2
2bet_thr	B	10	8	12	2
2bet_smt	B	8	8	12	2
3bet_any	C	6	6	12	2

Table 9-4 Commonly used technology files and their properties

in Chap. 6 you can see that with 6-mil traces you can run up to about 300 mA on inner traces and about 600 mA on the outer traces. So you can usually use any of the standard technology files for most small signal applications.

For this example we specify that all signals will be very low frequency (<20 kHz) so that trace impedance is not a concern. An example of designing controlled impedance transmission lines is given in the digital design example later in the chapter.

Determining trace spacing requirements

The op-amp used in this example requires a dual rail supply, which can be up to ±15 V (and the input and output voltages must be between the rails). The greatest voltage difference possible between any two traces then is $30\,V_{P\text{-}P}$, so the spacing between the traces must be able to support this. If we decide to play it safe and use the 31–50 V range and we plan on using a soldermask then, using Table 6-8 in Chap. 6, the route spacing should be 4 mils on internal layers and 5 mils on external layers.

Choosing a technology file (.TCH)

When you first open Layout and start a new design, Layout will ask what technology file you want to use. The technology file defines the board layer structure and sets default values for trace width and route spacing (e.g., trace-to-trace and trace-to pad-spacing), default grids, padstack descriptions, default colors, etc. Table 9-4 lists the most commonly used technology files with some of their default values. A complete listing of all the technology files and their characteristics is given in Appendix A.

Table 9-5 shows a summary of the board requirements for this design example and lists the technology files that meet the requirements. All of the technology files listed in

Component and board requirements		Supporting technology files
Component mounting	Mixed (SMT and THT)	*bet_any.tch
No. sides w/parts	1	All
No. plane layers	2	All
No. routing layers	2	All
Total No. layers (minimum)	4	All
Smallest leads	SOIC-8	All
Pad spacing (minimum)	50 mils	All
Pad width (maximum)	25 mils	All
Max current	0.1 A	All
INNER trace width (min)	1.3 mils	All
OUTER trace width (min)	0.5 mils	All
Max voltage	10 V	All
Trace Spacing (INNER)	4 mils	All
Trace spacing (OUTER)	5 mils	All

Table 9-5 Analog design constraints and applicable technology files

Table 9-4 meet all design requirements except that none of them have the required number of plane layers, so no matter which one is chosen, additional plane layers will have to be added to the design. Whenever possible it is best to use the least design complexity; therefore either the default or 1bet_any technology files will work for this design; we will use 1bet_any.tch. Once a technology file has been selected in Layout you can modify any of the parameters as needed to meet the design requirements. See Miscellaneous Items at the end of this chapter to find out how to set up your own technology and template files.

Choosing a strategy file (.SF)

Layout has 25 routing strategy files (.SF). This design example requires no special routing, so we will use the standard strategy file (STD.SF), which is assigned by Layout by default. For further information on strategy files see the *Layout User's Guide*, Chap. 9.

Importing the design into Layout

Once the .MNL file is made in Capture, and you have copied the footprint library ANALOG_EX.LLB into the Layout library folder, and you know which technology file to use, you can import the design into Layout and begin building your board.

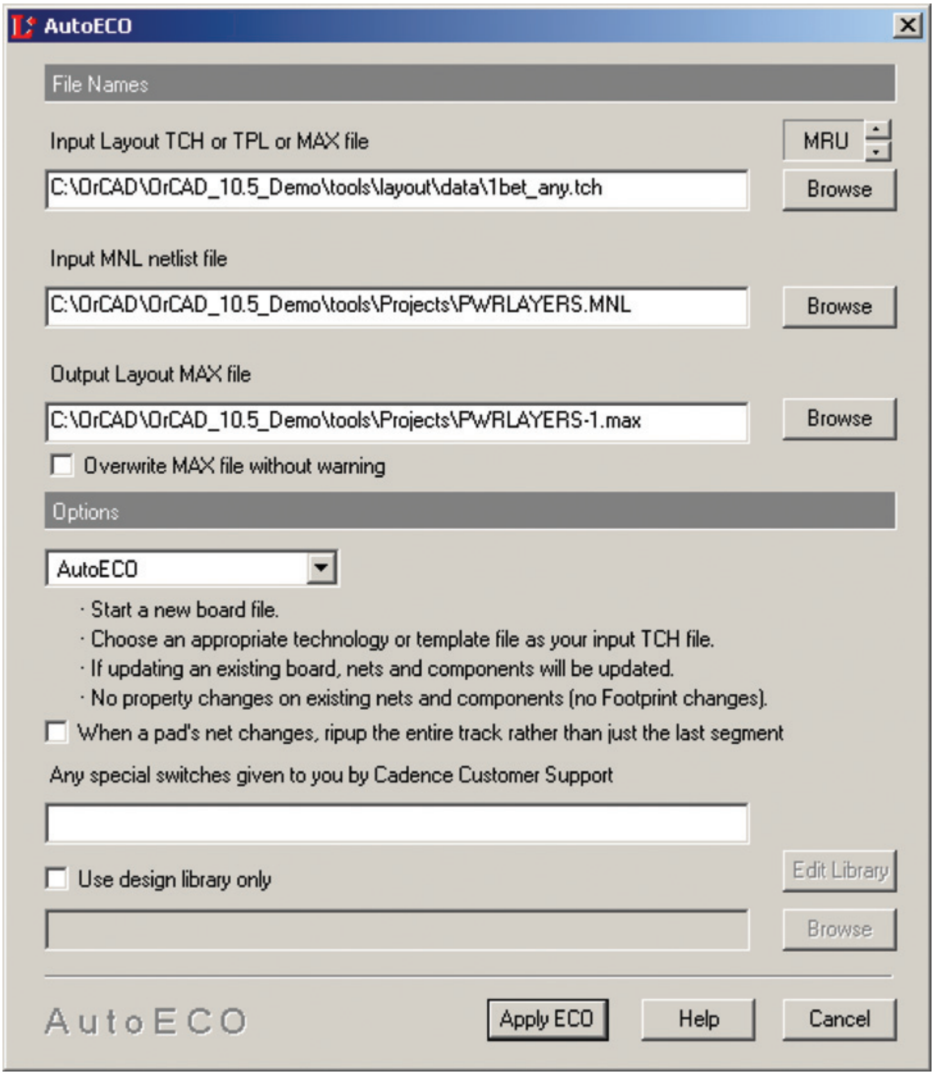
To import the .MNL file into Layout start Layout and from the session frame select File → New to bring up the AutoECO dialog box (see Fig. 9-24). Use the top Browse button to find and select the 1bet_any.tch technology file (located in the Data folder). Use the second Browse button to find and select the .MNL file from your design. The Output Layout MAX file text box should automatically be filled in for you once you specify the .MNL file. Under the Options section, make sure that AutoECO is selected (see Types of AutoECOs at the end of this chapter for more info on the various types of ECOs). Click Apply ECO.

If everything goes OK, you should get the ECO list report. But probably it won't.

If you encounter an error (for example the one shown in Fig. 9-25), the most likely cause will be that a part does not have a footprint assigned to it or one that was assigned is not present in one of the Layout libraries, or the AutoECO tool does not know about the library yet. If you followed the procedure at the beginning of the example then it should just be a simple manner to add the library to the AutoECO tool.

To add the ANALOG_EX footprint library to the AutoECO tool's library list, click the Link existing footprint to component... button. The dialog box shown in Fig. 9-26 should be displayed. Click the Add... button; an Add Library dialog box will be displayed. Navigate to the ANALOG_EX footprint library, select it, and click Open.

Once the new library has been added to the list, select it. The footprints that are contained in the library will be displayed in the Footprints list box. Select the desired footprint; it will be displayed in the preview window. Click OK to select it. The AutoECO report should then be displayed. Click Accept this ECO.



AutoECO

File Names

Input Layout TCH or TPL or MAX file

C:\OrCAD\OrCAD_10.5_Demo\tools\layout\data\1bet_any.tch

Input MNL netlist file

C:\OrCAD\OrCAD_10.5_Demo\tools\Projects\PWRLAYERS.MNL

Output Layout MAX file

C:\OrCAD\OrCAD_10.5_Demo\tools\Projects\PWRLAYERS-1.max

☐ Overwrite MAX file without warning

Options

AutoECO

- Start a new board file.
- Choose an appropriate technology or template file as your input TCH file.
- If updating an existing board, nets and components will be updated.
- No property changes on existing nets and components (no Footprint changes).

☐ When a pad's net changes, ripup the entire track rather than just the last segment

Any special switches given to you by Cadence Customer Support

☐ Use design library only

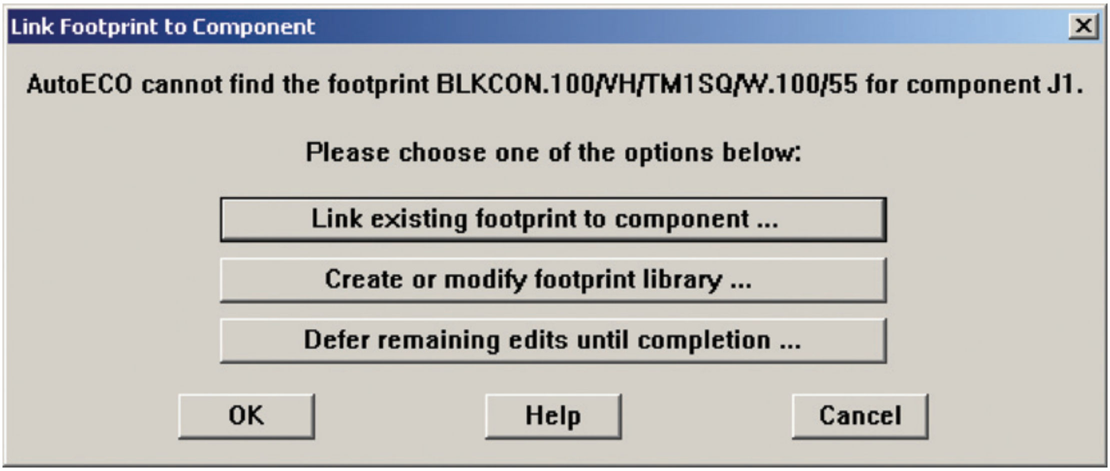
Figure 9-24 Using the AutoECO to begin a new PCB design in layout.

The first view you have of your new board will probably be a black background and part of a red square. Click the Zoom All button, 🔍 so that you can see the entire design. You should see something similar to Fig. 9-27.

Setting up the board

Making a board outline

The first step in laying out the board is to make the board outline and add mounting holes so that the boundaries of the board are known. First turn off the DRC box by toggling the



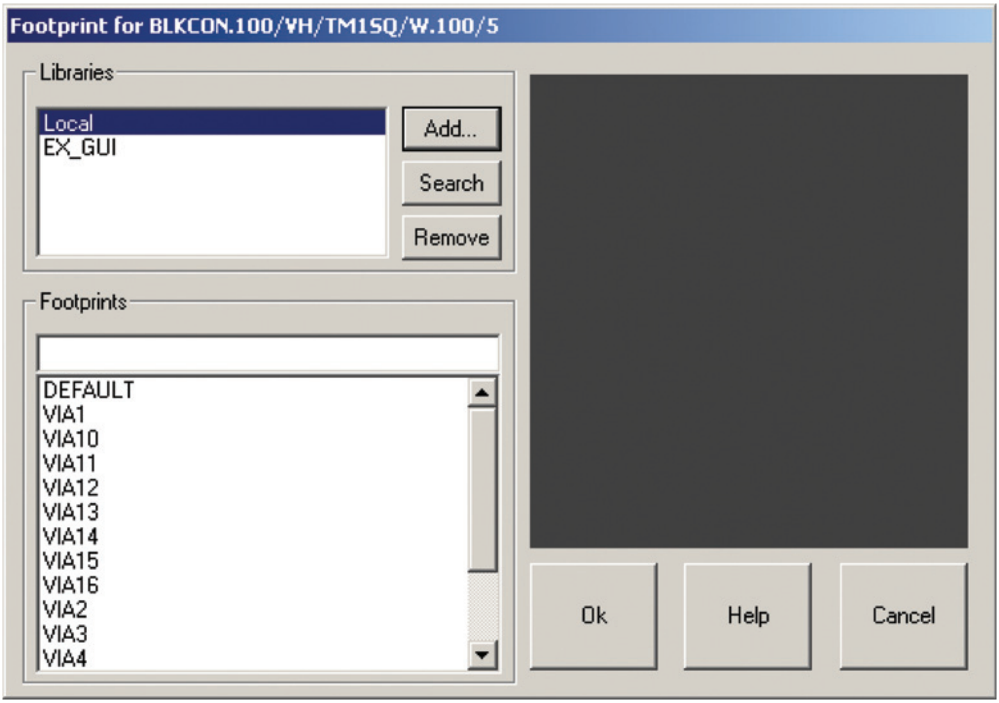
Link Footprint to Component

AutoECO cannot find the footprint BLKCON.100/VH/TM1SQ/W.100/55 for component J1.

Please choose one of the options below:

Link existing footprint to component ...
Create or modify footprint library ...
Defer remaining edits until completion ...
OK
Help
Cancel

*Figure 9-25 Example of the AutoECO **Link Footprint** error.*



Footprint for BLKCON.100/VH/TM1SQ/W.100/5

Libraries
Local
EX_GUI
Add...
Search
Remove
Footprints
DEFAULT
VIA1
VIA10
VIA11
VIA12
VIA13
VIA14
VIA15
VIA16
VIA2
VIA3
VIA4
Ok
Help
Cancel

Figure 9-26 Adding a footprint library to the AutoECO tool's library list.

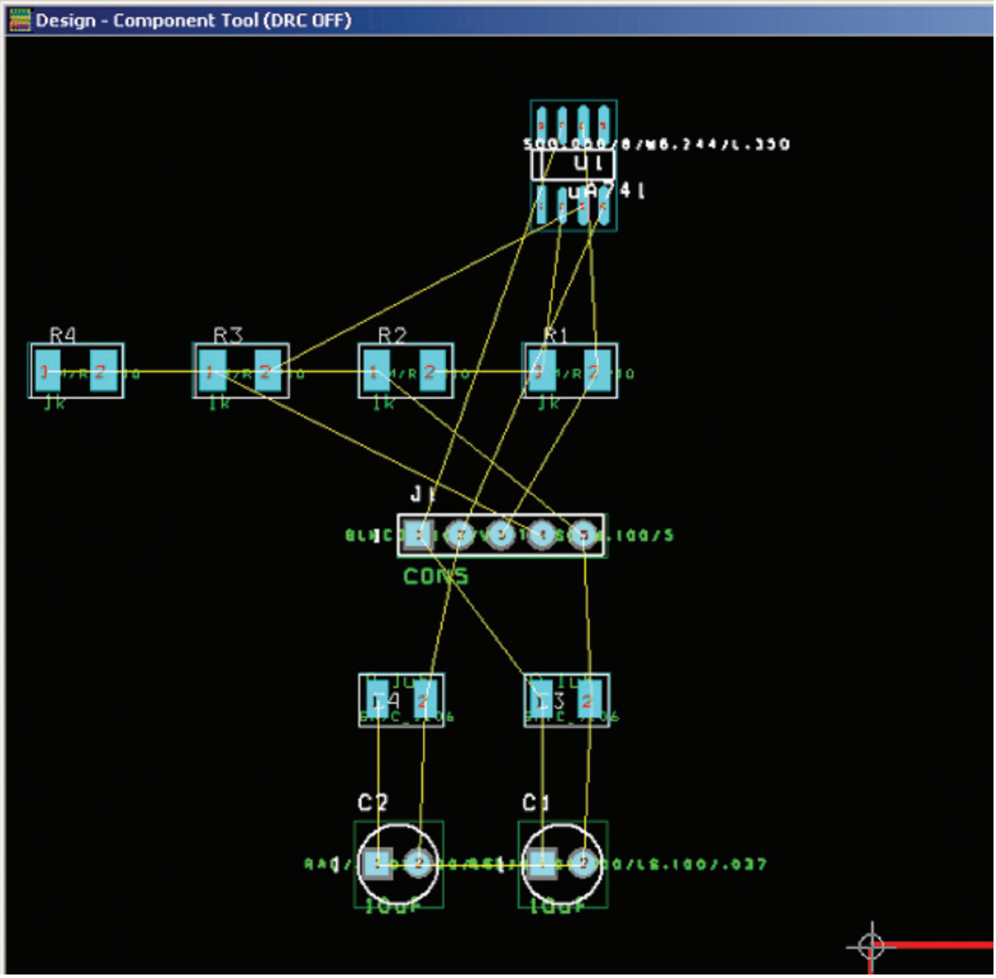


Figure 9-27 Initial view of the analog design.

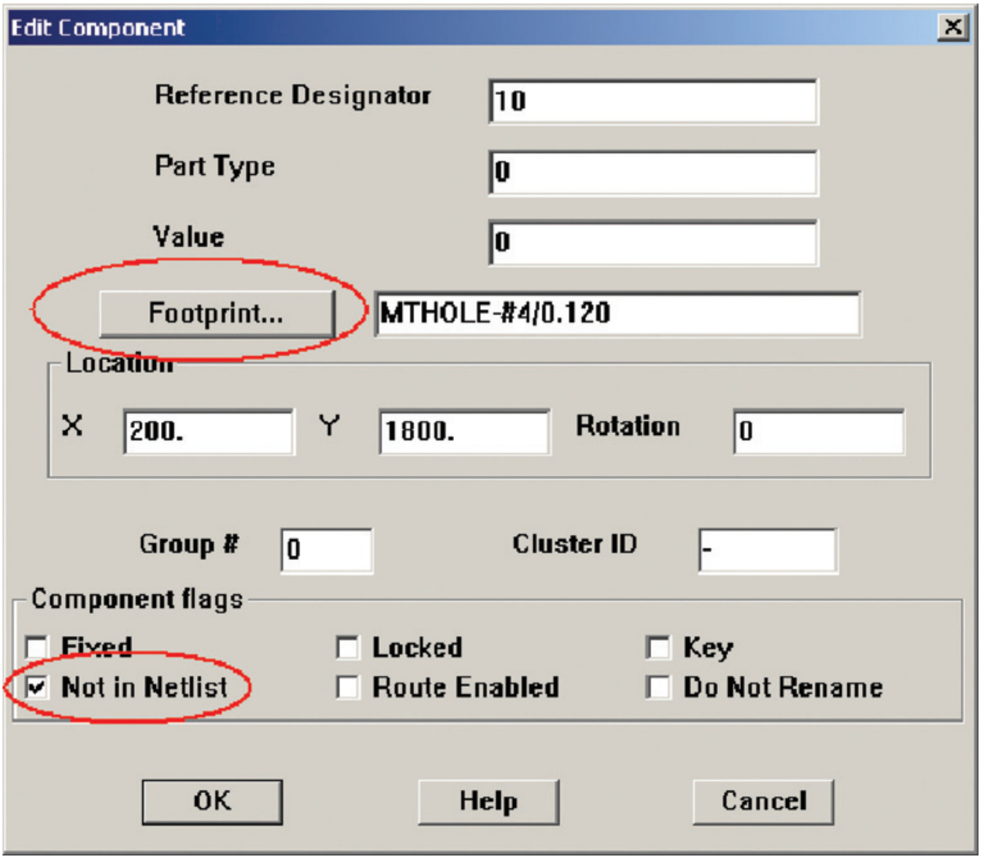
Online DRC button, DRC located on the toolbar. Then, **draw a board outline**: select the Obstacle tool, ✎. Right click in the work space and select New from the pop-up, right click again, and select Properties to invoke the Edit Obstacle dialog box. Make sure the obstacle is a Board outline on the Global layer. Click OK.

Left click at point 0,0 to place the first vertex. Left click to place each vertex of the board outline. Make the board outline about 2.0 × 2.5 in. (2000 × 2500 mils). Right click and select Finish from the pop-up after you have placed the fourth vertex.

The board outline possesses properties of several types of obstacles, including place outlines, route keep-outs, and anti-copper. The board outline can therefore alert you (through DRC errors) when parts or traces are too close to the board edge. It also removes copper from plane layers so that the conductors are not exposed at the board edges. The amount of copper that is removed is determined by the width of the outline.

Adding mounting holes

Next, place mounting holes on the board. This should be done before moving any parts into the board outline. **To place mounting holes** select the Component tool, right click, and select New... from the pop-up to display the Add Component dialog box shown in Fig. 9-28. Select the Footprint... button, navigate (or Add) to the Layout footprint library (or the ANALOG_EX library), and select the MTHOLE-#4/0.120 footprint to accommodate a #4-40 machine screw. Click OK. At the Edit Component dialog box check the Not in Netlist box to prevent the mounting hole from being removed the next time you run AutoECO. Click OK and place the mounting hole in the desired location. You can add more mounting holes by repeating the above procedure or by copying and pasting them.



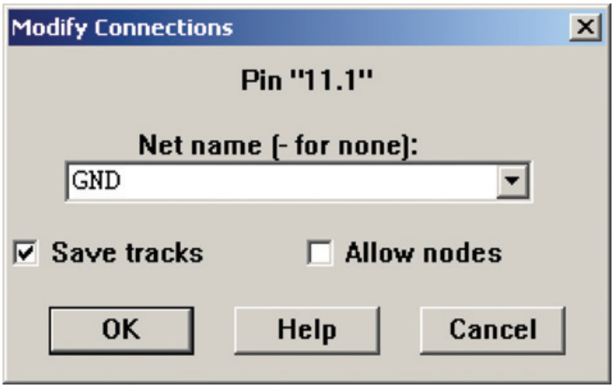
Reference Designator: 10
Part Type: 0
Value: 0
Footprint: MTHOLE-#4/0.120
X: 200.
Y: 1800.
Rotation: 0
Group #: 0
Cluster ID: -
☐ Fixed
☑ Not in Netlist
☐ Locked
☐ Route Enabled
☐ Key
☐ Do Not Rename

Figure 9-28 Using **Edit Component** dialog box to add mounting holes.

Note

- *If you are using the Demo version of Layout, you can have only 10 components in the design. If you already have 10 components, Layout will not allow you to add mounting holes.*

You can leave a mounting hole isolated from the copper on all layers, or if it is a plated mounting hole you can connect it to a net (e.g., the ground plane). **To connect a plated mounting hole to a net**, select the Pin tool, Ctrl + left click the mounting hole (padstack), right click, and select Properties from the pop-up to display the Modify Connections dialog box shown in Fig. 9-29. Select the net or plane you want to attach the mounting hole's plating to and click OK.


Modify Connections

Pin "11.1"

Net name (- for none): GND

☑ Save tracks

☐ Allow nodes

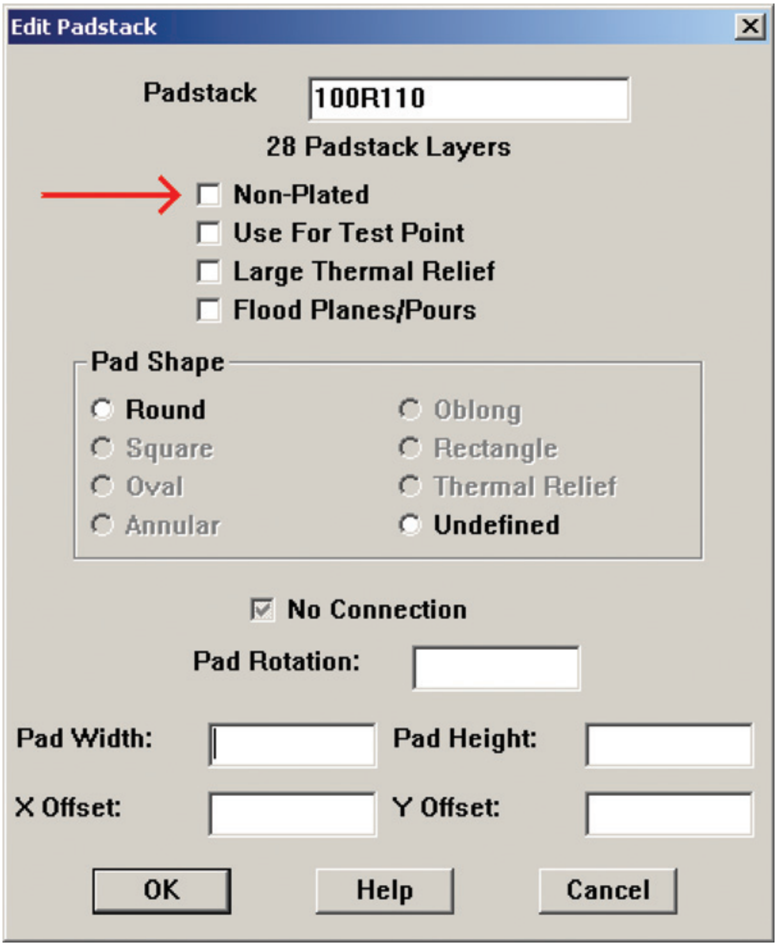
Figure 9-29 Adding a mounting hole to a net.

The mounting holes supplied with Layout are plated by default. **To make mounting holes nonplated**, toggle the Pin tool and select the mounting hole's padstack (use Ctrl + left-click). Toggle the View Spreadsheet button on the toolbar and select Padstacks from the pop-up. When the padstack spreadsheet is displayed the mounting hole's padstack should be highlighted. Right click and select Properties... from the pop-up. Select the Non-Plated option in the Edit Padstack dialog box as shown in Fig. 9-30.

Specifying a nonplated via instructs the postprocessor to create a separate drill file called thruhole.npt (recall that the drill file for plated through-holes is thruhole.tap). Nonplated holes are drilled separately as one of the very last steps of the board fabrication and no plating processes occur after the final drilling. See Chap. 8 for other ways of designing mounting holes and Appendix E for standard machine screw and drill hole sizes.

Adding dimension measurements

You can add dimension lines and measurements to your board for documentation purposes. You can also add temporary dimensions as guides to mark locations for mounting holes and



Edit Padstack

Padstack: 100R110

28 Padstack Layers

☐ Non-Plated
☐ Use For Test Point
☐ Large Thermal Relief
☐ Flood Planes/Pours

Pad Shape

○ Round
○ Square
○ Oval
○ Annular
○ Oblong
○ Rectangle
○ Thermal Relief
○ Undefined

☑ No Connection

Pad Rotation:

Pad Width:

Pad Height:

X Offset:

Y Offset:

*Figure 9-30 Use the **Edit Padstack** dialog box to make a padstack nonplated.*

connectors, etc. Dimensions can be placed on assembly or comment layers (e.g., the Notes layer). Once you are satisfied with the board layout, you can turn off documentation layers and/or delete temporary dimension lines.

Adding dimensions and measurements is a three-step process. Each step is accomplished from the Tools → Dimension menu (see Fig. 9-31) and is used to (1) specify the snap settings, (2) specify the type of dimension, and finally (3) place the dimension.

Figure 9-32 shows examples of relative and absolute dimensions. **Relative dimensions** show the distance between a starting point and an ending point. **Absolute dimensions** indicate *x* or *y* distances from the origin. A relative dimension line requires two click points—the beginning point and the endpoint. The measurement located in the center of the dimension is the distance between the two click points. An absolute dimension requires only one click point and the indicated measurement is the horizontal or vertical distance from the origin.

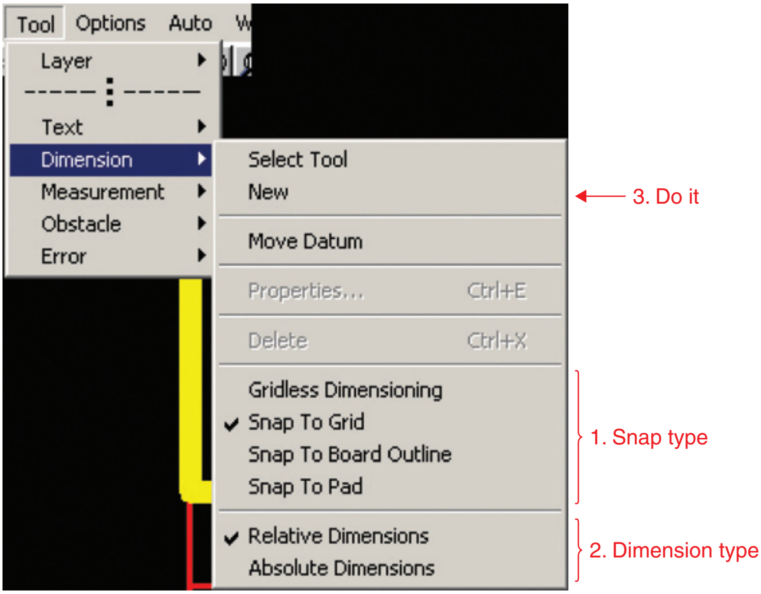

Tool
Options
Auto
Layer
Text
Dimension
Measurement
Obstacle
Error
Select Tool
New
Move Datum
Properties... Ctrl+E
Delete Ctrl+X
Gridless Dimensioning
✓ Snap To Grid
Snap To Board Outline
Snap To Pad
✓ Relative Dimensions
Absolute Dimensions
3. Do it
1. Snap type
2. Dimension type

Figure 9-31 Setting up and placing dimension lines.

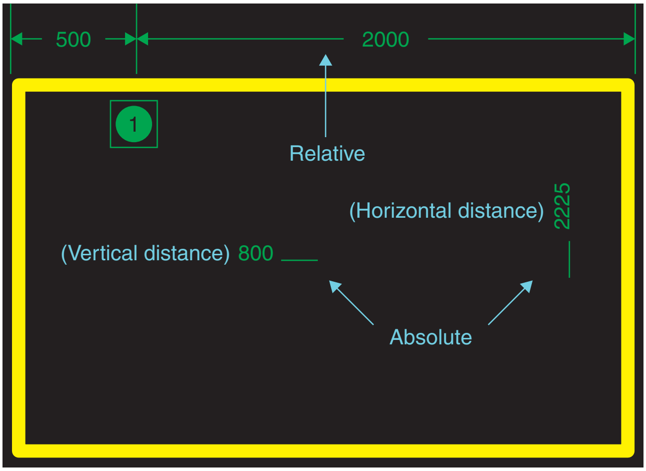

500
2000
1
Relative
(Horizontal distance)
2225
(Vertical distance) 800
Absolute

Figure 9-32 Relative and absolute dimension lines.

Once the grid and type are set you do not have to keep setting them. You need to repeat this process only if you want to change the grid or dimension type. **To set the dimension grid and type** select Tools → Dimension → Snap to Grid, then Tools → Dimension → Relative.

To place a relative dimension select Tools → Dimension → New (or right click and select New from the pop-up). Left click the mouse once to begin the dimension line. Move the mouse to the endpoint and left click once more to end the dimension line.

To place an absolute dimension select Tools → Dimension → Absolute. Then Tools → Dimension → New. A horizontal line (for vertical distance) or vertical dimension line (for horizontal distance) with dynamic text will be attached to your mouse. As you move the mouse the text will be immediately updated. To change the orientation of the dimension marker hit the R key on your keyboard repeatedly until it is the correct orientation. Left click once to place the marker.

Once you place a dimension and end the command, the line becomes a simple obstacle and the distance number becomes a simple text object. This means that you can move them with the Obstacle tool or the Text tool, but they will not be updated with new dimension information. If you need to change or move a dimension line to measure a new parameter you will have to place a new one.

Placing parts

Placing parts is part art and part science. How you ultimately place the parts on the board depends on both mechanical and electrical factors. Mechanical factors include designing for manufacturability (assembly and soldering processes) and physical board constraints (size, shape, etc.). Electrical factors include functional signal flow, thermal management, signal integrity, and electromagnetic compliance. Usually all of these considerations are important, and in some cases they can conflict with one another. These issues are discussed in greater detail in Chaps. 4, 5, and 6 and in the IPC standards. In this example, the parts will simply be placed so that the board layout is similar to the schematic.

When you initially set up the .MAX file the parts will be placed in a pile off to the left of the origin. The first step is to find the desired parts and begin moving them from the pile to the inside of your board outline. There are a couple of things that can be helpful in making the pile look less confusing. The first is to turn off the Assembly layers (AST and ASB), and the second is to turn off the rat's nest (the yellow net lines). The assembly layers do not tell us anything important for placing parts, and we are not ready to deal with the nets just yet, so they will just be a distraction.

To turn off the assembly layers, use the Layer Selection dropdown list, select the AST (assembly top) layer and hit the "-" key on your keyboard to turn that layer off. This will make easier to see what you are doing. If you want to turn it back on, just select the AST layer from the layer list or if the AST layer is already selected then just hit the "-" key again. Repeat this step for the bottom assembly layer if you plan on putting parts on the back side of the board. Finally, from the Layer list select layer 1 (TOP) to restore the view.

There are two ways to turn off the rat's nest. The first (and easiest way) is to toggle the Reconnect Mode button, . This just makes the nets look invisible and does not actually affect their connectivity. The second way is to actually disable the nets (which affects both the visibility and the routability). **To disable the nets**, toggle the Spreadsheets button and select Nets from the pop-up to display the Nets spreadsheet. Click the Routing Enabled cell at the top of the spreadsheet, right click, and toggle the Enable <-> Disable option and close the spreadsheet.

Before you begin placing parts you may want to **adjust the placement grid resolution**. Go to Options → System Settings and change the Place Grid [X, Y]: to 50 mils (or 25 mils for greater resolution as suggested by IPC). Click OK.

Finding parts

The first objective is to get the parts into their relative positions. After that you can begin to carefully and precisely place the components. It is often a shuffle game at first until you get a feel for the parts and the space you have to work with. There are a couple of ways to find, select, and place parts. You can manually find and place the parts one by one, or use the Find tool to locate a part and then place it on the board, or use the Queue to “fetch” parts for you.

To find and place parts manually select the Component tool button and look through the pile to find the part you want. When you find the part you are looking for, select the part by left clicking it once and then move the part to the inside of the board outline. Left click again to place the part. You can rotate the part by repeatedly hitting the R key on your keyboard. You can also place the part on the back side of the board by hitting the T key on your keyboard.

Another method of picking parts out of the pile is to use the Find/Goto function. When you use the Find/Goto function the pointer will be moved to the part (or a pin on a part) and a big X will mark its location. **To find a part** press Ctrl + F on your keyboard or select Find/Goto from the Edit menu to bring up the Find dialog box (Fig. 9-33). To find the resistor R1, for example, type R1 (or R1.1 to locate pin 1 of R1) in the Item Name: text box and then click OK. R1 will be marked with the X; click the part to select it and then move it into the board outline.

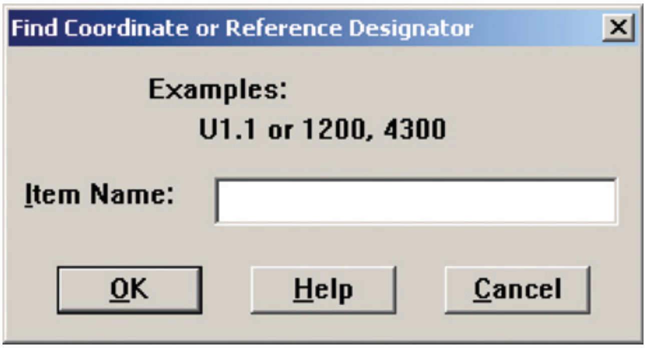
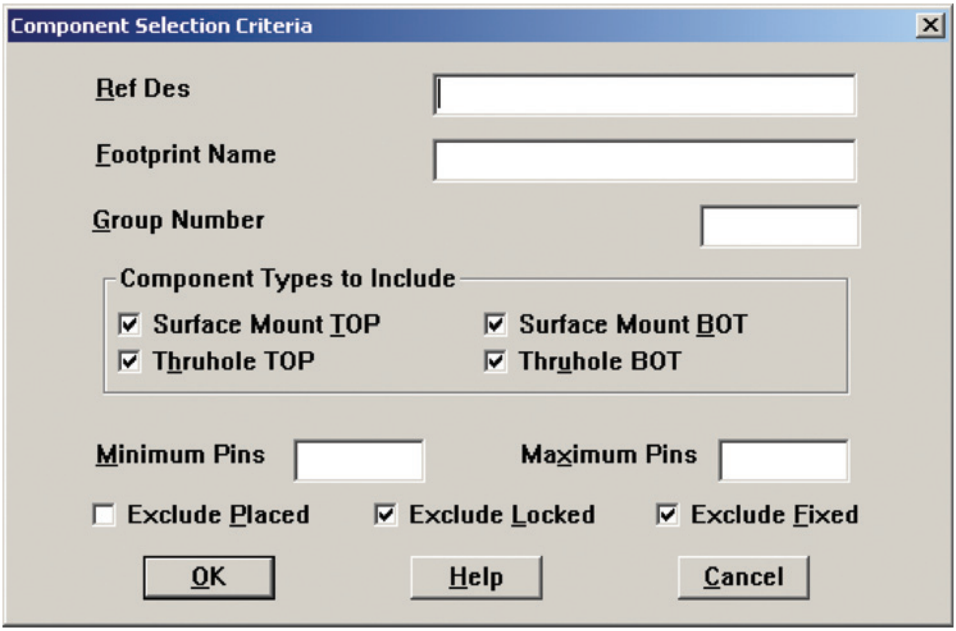


Figure 9-33 Using the Find function to select parts for placement.

To select certain parts without having to actually find them in the pile, you can have a part snap to your mouse cursor. **To make a part snap to the cursor**, display the Component Selection Criteria dialog box (Fig. 9-34) by pressing Alt + S on your keyboard or choosing Edit → Select Any from the tool menu, or right clicking and selecting Select Any from the pop-up. From the dialog box you can select a part by its reference designation (e.g., R1 or U23), by a footprint, or by group number (see below).



Component Selection Criteria

Ref Des

Footprint Name

Group Number

Component Types to Include

☑ Surface Mount TOP ☑ Surface Mount BOT

☑ Thruhole TOP ☑ Thruhole BOT

Minimum Pins

Maximum Pins

☐ Exclude Placed ☑ Exclude Locked ☑ Exclude Fixed

Figure 9-34 Using ***Component Selection Criteria*** *to select parts for placement.*

Placing parts in the queue

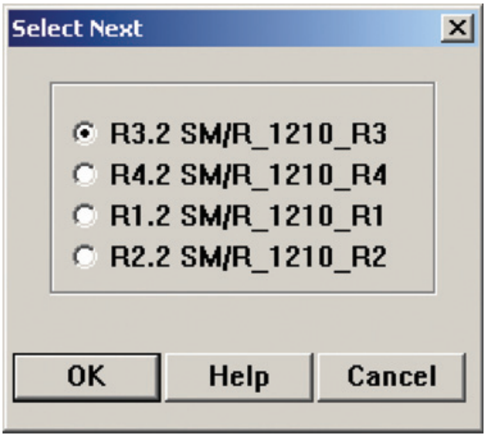
An elegant way to place parts is to make a placement list to queue parts for placement. Then all you need to do is hit N on your keyboard to cycle through the list. You can **add parts to the placement queue** using the Tool → Component → Queue For Placement... option or right click and select Queue For Placement... from the pop-up. A Component Selection Criteria dialog box (Fig. 9-34) will be displayed. You can place items in the queue based on their reference designators, footprints, or group numbers.

For example, to place all resistors in the queue, use one of the Queue For Placement... commands to display the Component Selection Criteria dialog box (Fig. 9-34) and enter R* in the Ref Des text box and then click OK. All resistors are now in the queue.

To select a particular part from the queue, display the Select Next dialog box (Fig. 9-35) by selecting Tools → Component → Place, or right click and select Place from the pop-up. Select the component of interest and click OK.

To automatically place the next part in the queue, just hit N (Select Next) on your keyboard and the next part in the queue will automatically be attached to your pointer. Left click to place the part.

You can use the parts queue in conjunction with the Group Number you specified on the schematic page in Capture. **To place a group into the queue**, display the Component Selection Criteria dialog box (Fig. 9-34) and enter the number for the group of parts you want to place and then click OK. All of the parts in the group will be attached to your pointer



● R3.2 SM/R_1210_R3
○ R4.2 SM/R_1210_R4
○ R1.2 SM/R_1210_R1
○ R2.2 SM/R_1210_R2

Figure 9-35 Selecting parts from the placement matrix.

as a minipile. To place the parts, left click inside the board outline in the location where the parts should go. The parts within the group will be stacked on top of each other like football players on a fumbled ball, so you will have to move them apart using the manual "one-by-one," the "select any," or the "select next" method described above.

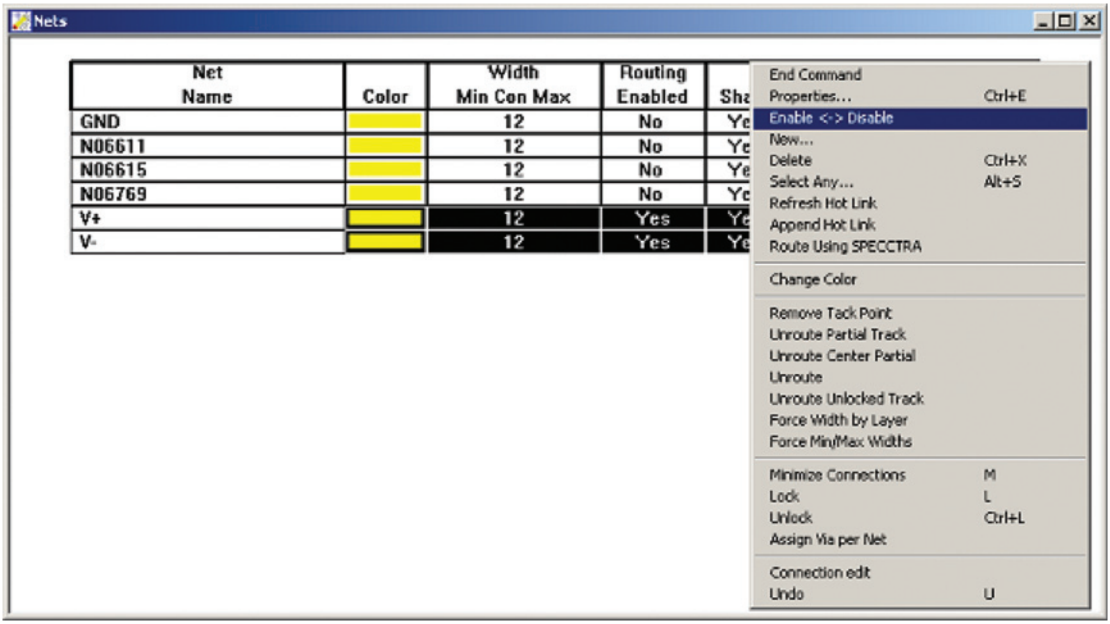
One trick that is often helpful is to disable all nets except for nets connected to key components. The few enabled nets help identify which parts are which and what they are connected to, thereby making it easier to decide where the parts should go. Take a look at the schematic again and decide which parts you want together regardless of how the board ends up being laid out. Enable those nets first. For example, in the schematic (Fig. 9-5) the bulk capacitors should be close to the connector, J1, and the bypass caps should be close to the amplifier, U1; enable the nets that connect those parts first and leave all others disabled. The Nets spreadsheet is used to make nets visible (invisible) by enabling (disabling) them.

To enable and disable nets open the Nets spreadsheet by clicking the View Spreadsheet button, ▦ and select Nets from the pop-up. Toggle the Routing Enabled property (see Fig. 9-36) by selecting (highlighting) a net (or nets). Right click and toggle the Enable <-> Disable selection. Disable all nets except the V+ and V− nets.

With just a few nets enabled it is easier to see the lay of the land. Figure 9-37 shows the board with the initial parts placed.

Once the first parts are placed, disable the V+ and V− nets again and enable the remaining nets (except GND). Place the resistors near the amplifier in a way that allows the signals to flow easily from one point to the next by the shortest route. One example of how the parts could be placed is shown in Fig. 9-38.

Once you have the parts in their preliminary locations, you can use the Text tool button to move the reference designators (U1, J1, etc.) around so that they are conveniently placed near their respective components and easy to read.


Nets
End Command
Properties... Ctrl+E
Enable <-> Disable
New...
Delete Ctrl+X
Select Any... Alt+S
Refresh Hot Link
Append Hot Link
Route Using SPECCTRA
Change Color
Remove Tack Point
Unroute Partial Track
Unroute Center Partial
Unroute
Unroute Unlocked Track
Force Width by Layer
Force Min/Max Widths
Minimize Connections M
Lock L
Unlock Ctrl+L
Assign Via per Net
Connection edit
Undo U

Net Name	Color	Width Min Con Max	Routing Enabled	Sha
GND	🟨	12	No	Ye
N06611	🟨	12	No	Ye
N06615	🟨	12	No	Ye
N06769	🟨	12	No	Ye
V+	🟨	12	Yes	Ye
V-	🟨	12	Yes	Ye

Figure 9-36 Enabling and disabling nets.

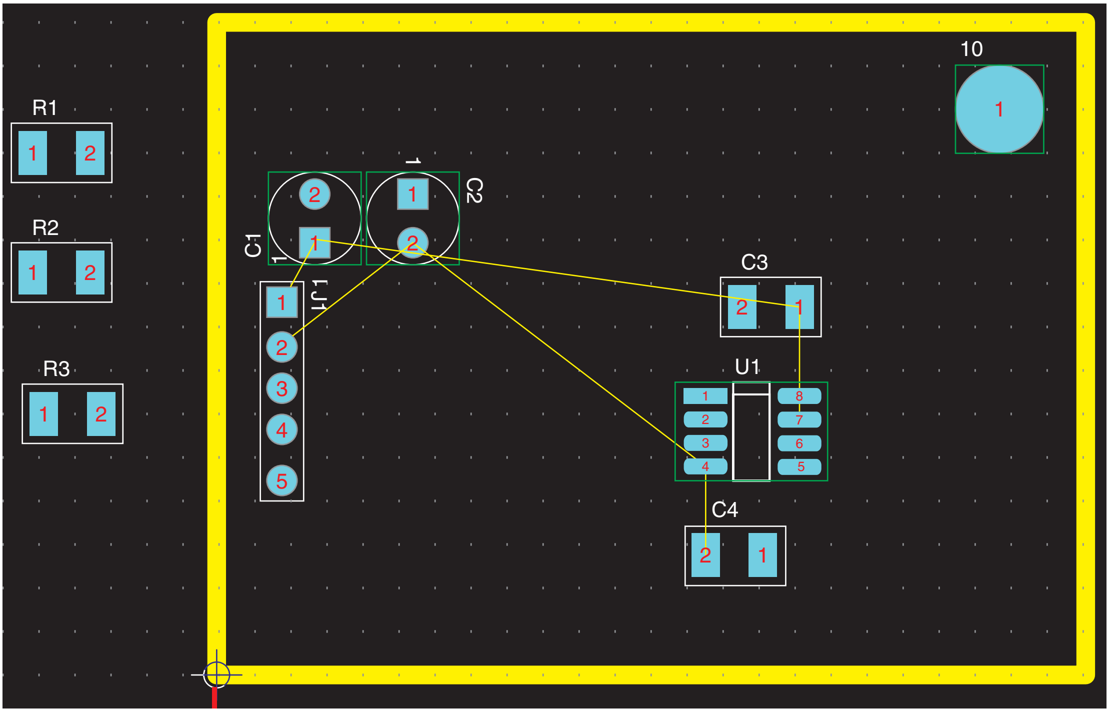

R1
1
2
R2
1
2
R3
1
2
C1
C2
J1
C3
U1
C4
10
1

Figure 9-37 Placing the first parts.

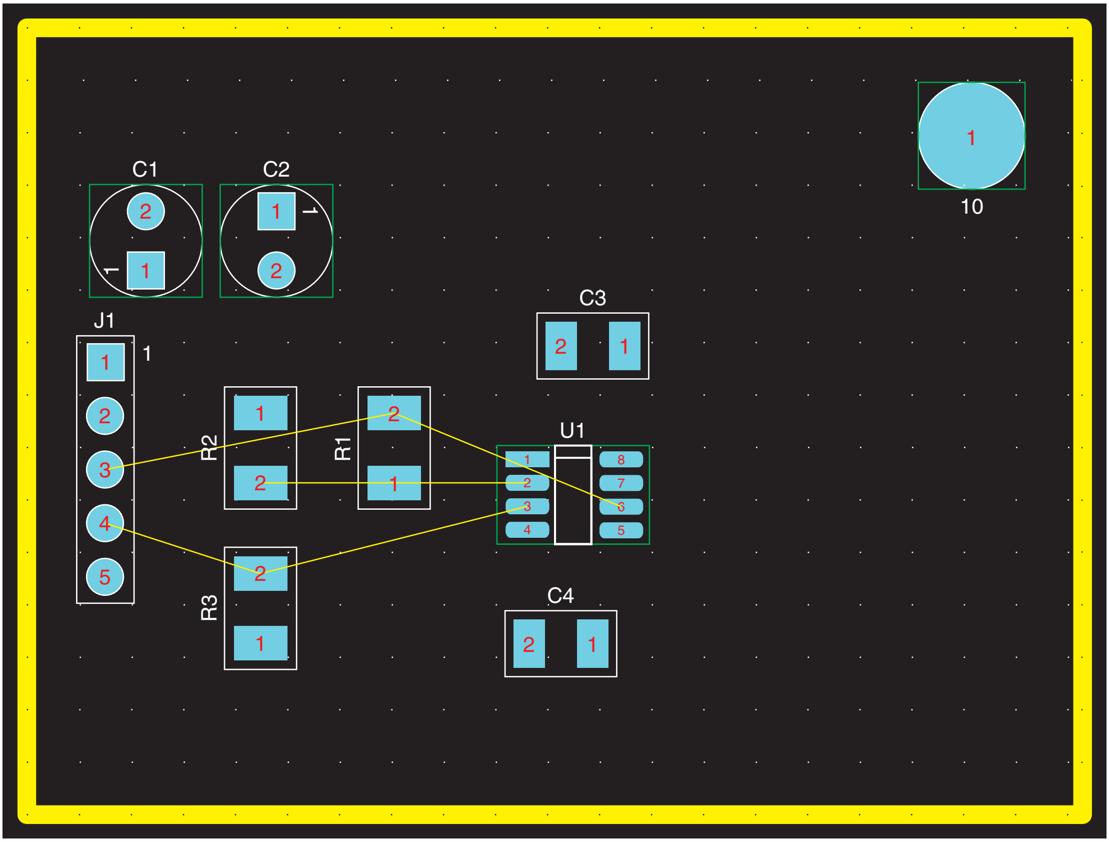


Figure 9-38 Final parts placement.

Perform a DRC to check for any major problems before you set up the layers and begin routing. If you used the footprints specified in Capture as described above and you used the 1bet_any technology file, you should not have any errors (yet). In the following steps and in the second example below it will be shown how to find and correct common errors.

Intertool communication

In large circuits it can be a challenge to find specific nets on the spreadsheet because of the large number of them and because they are given generic names like N06615. Nets can be given specific names in Capture (such as Input or Feedback) and those names will follow through to Layout and be displayed on the Nets spreadsheet. This can make it easier to identify specific nets, but for very large circuits this would still be cumbersome. It is easier, instead, to use the intertool communication capabilities between Capture and Layout to identify nets and parts.

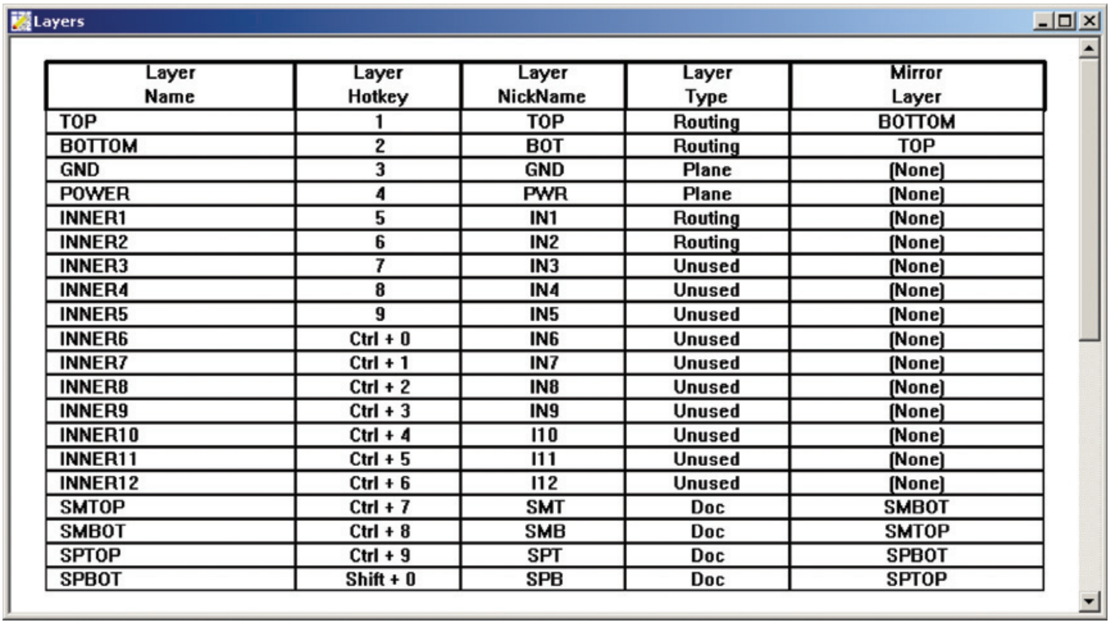
Intertool communication between Capture and Layout can be used to find specific nets in the Nets spreadsheet in Layout from Capture (Capture and Layout need to be running at the same time). If you select a net in Capture and open the Nets spreadsheet in Layout that net is automatically highlighted in the spreadsheet. You can use this technique to systematically find and enable/disable specific nets to assist in placing parts or to route traces in a controlled order.

You can also use the intertool communication to find parts in the Capture schematic from Layout. To see how this works select one of the parts on the board in Layout. That part will automatically be highlighted on the schematic in Capture too.

Setting up the layers

Once you have the parts in place, the next step is to set up the layers. In this design we said that we needed six layers—two power planes, two ground planes, and two routing layers.

First, let's take an inventory of what we have. Click the View Spreadsheets button on the toolbar and select the Layers option. Figure 9-39 shows the default layer configuration. Six layers are defined: two plane layers (power and ground) and four routing layers (top, bottom, and two inner layers). We need two more plane layers and two fewer routing layers.



Layer Name	Layer Hotkey	Layer NickName	Layer Type	Mirror Layer
TOP	1	TOP	Routing	BOTTOM
BOTTOM	2	BOT	Routing	TOP
GND	3	GND	Plane	(None)
POWER	4	PWR	Plane	(None)
INNER1	5	IN1	Routing	(None)
INNER2	6	IN2	Routing	(None)
INNER3	7	IN3	Unused	(None)
INNER4	8	IN4	Unused	(None)
INNER5	9	IN5	Unused	(None)
INNER6	Ctrl + 0	IN6	Unused	(None)
INNER7	Ctrl + 1	IN7	Unused	(None)
INNER8	Ctrl + 2	IN8	Unused	(None)
INNER9	Ctrl + 3	IN9	Unused	(None)
INNER10	Ctrl + 4	I10	Unused	(None)
INNER11	Ctrl + 5	I11	Unused	(None)
INNER12	Ctrl + 6	I12	Unused	(None)
SMTOP	Ctrl + 7	SMT	Doc	SMBOT
SMBOT	Ctrl + 8	SMB	Doc	SMTOP
SPTOP	Ctrl + 9	SPT	Doc	SPBOT
SPBOT	Shift + 0	SPB	Doc	SPTOP

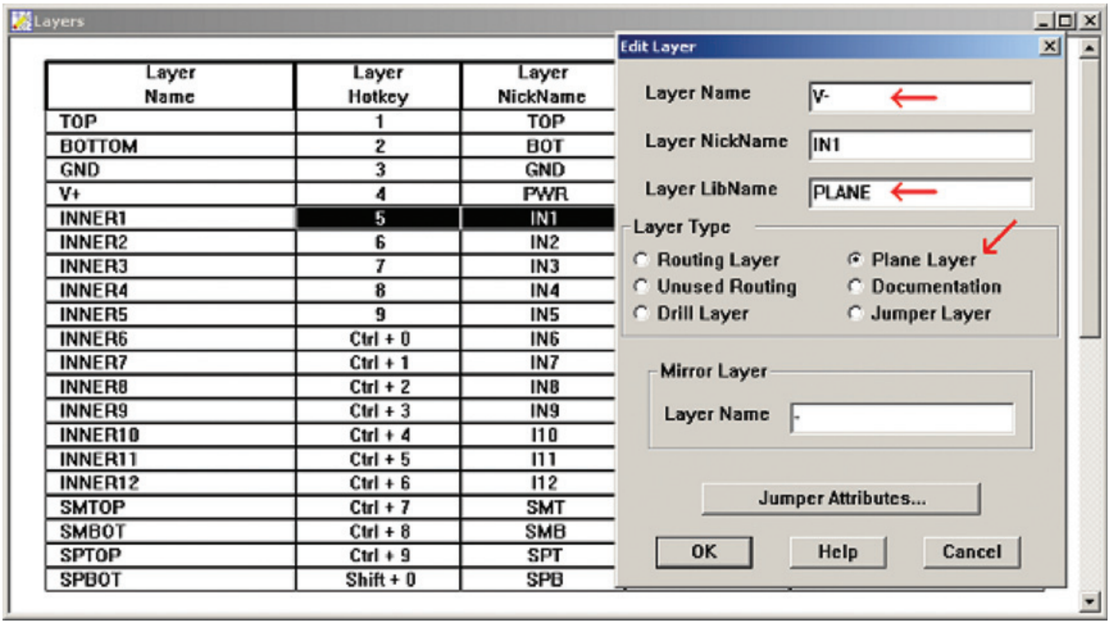
Figure 9-39 Default layer stack-up.

Converting a routing layer to a plane layer

There are two ways to add plane layers. The first method is to convert a routing layer into a plane layer. The second method is to add a new plane layer based on the properties of an existing plane layer. Both methods are demonstrated here.

We begin by using method 1 to convert routing layer, INNER1, into a second power plane. The two power planes will be V+ and V−. First, we will change the name of the existing power plane to match the name of the positive power supply net. The layer name does *not* have to be the same as the net name, but it makes it easier to identify when working on the board. **To change the name of a layer**, open the Layers spreadsheet and select the POWER cell to highlight the entire row. In the Layer Name text box replace the name POWER with the name V+, and click OK to close the dialog box.

Next, **to convert a routing layer into a plane layer**, double click the INNER1 layer to display the Edit Layer dialog box. As shown in Fig. 9-40, replace the name INNER1 with the name V− in the Layer Name text box. Also replace the layer template type INNER with PLANE in the Layer LibName box, and click the Plane Layer radio button. Layer IN1 now has the name V− and is a plane layer. Click OK.



Layer Name	Layer Hotkey	Layer NickName
TOP	1	TOP
BOTTOM	2	BOT
GND	3	GND
V+	4	PWR
INNER1	5	IN1
INNER2	6	IN2
INNER3	7	IN3
INNER4	8	IN4
INNER5	9	IN5
INNER6	Ctrl + 0	IN6
INNER7	Ctrl + 1	IN7
INNER8	Ctrl + 2	IN8
INNER9	Ctrl + 3	IN9
INNER10	Ctrl + 4	I10
INNER11	Ctrl + 5	I11
INNER12	Ctrl + 6	I12
SMTOP	Ctrl + 7	SMT
SMBOT	Ctrl + 8	SMB
SPTOP	Ctrl + 9	SPT
SPBOT	Shift + 0	SPB

Layer Name: V-

Layer NickName: IN1

Layer LibName: PLANE

Layer Type

○ Routing Layer ● Plane Layer
○ Unused Routing ○ Documentation
○ Drill Layer ○ Jumper Layer

Mirror Layer

Layer Name:

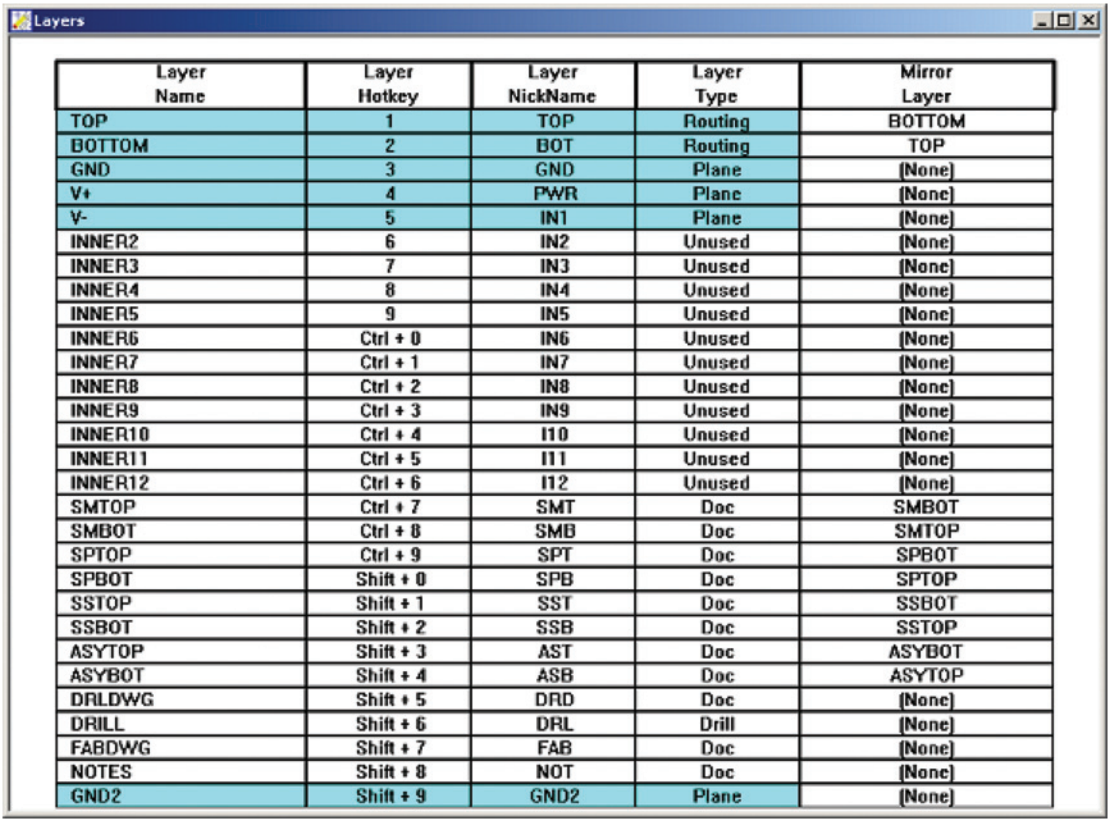
Figure 9-40 Converting a routing layer to a plane layer.

Note

- *Do **NOT** change the Layer NickName. The layer nickname is associated with a template file (that has a .PPS extension, located in the **Data** folder). If you change the nickname, Layout will not be able to associate the layer with a template and will not be able to route the layer correctly.*

Adding additional plane layers

The second method will now be used to **set up the second GND plane**. Display the Layers spreadsheet by clicking the View Spreadsheets button and selecting Layers from the menu. Select the GND layer by left clicking the GND cell name. Right click and select New... from the menu. A second ground plane, GND2, will be added to the Layers spreadsheet and will be located at the bottom of the list. This new layer is an exact copy of the first GND plane. Your layer setup should look like Fig. 9-41 (the six active layers are highlighted). The Stackup Editor can be used to move the GND2 cells up with the other active cells (the Stackup Editor is demonstrated at the end of the chapter). Close the Layers spreadsheet.

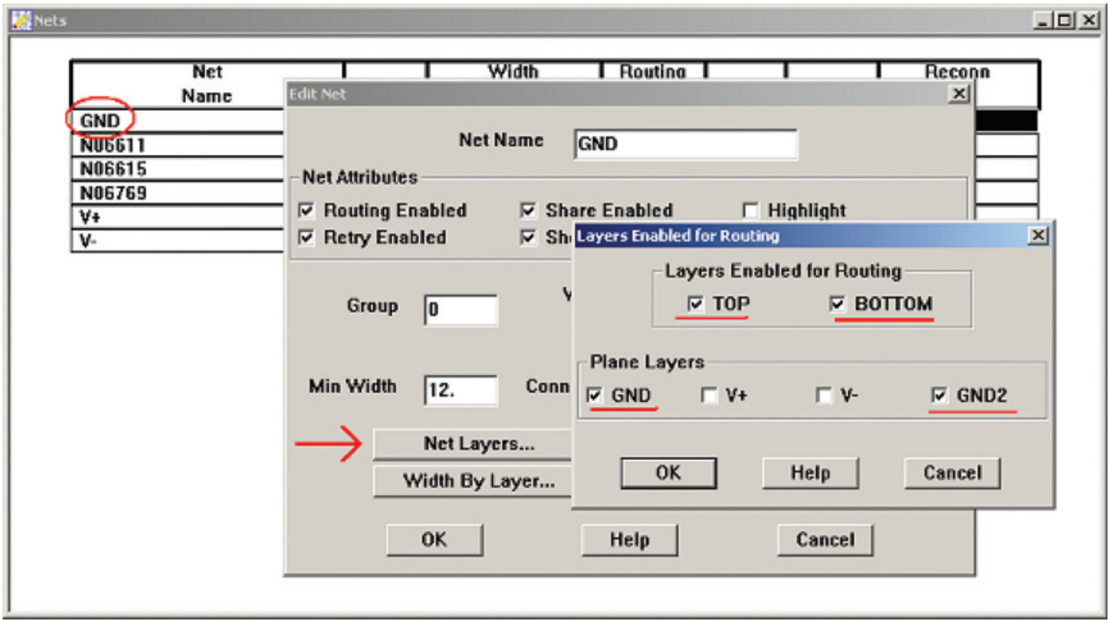


Layer Name	Layer Hotkey	Layer NickName	Layer Type	Mirror Layer
TOP	1	TOP	Routing	BOTTOM
BOTTOM	2	BOT	Routing	TOP
GND	3	GND	Plane	(None)
V+	4	PWR	Plane	(None)
V-	5	IN1	Plane	(None)
INNER2	6	IN2	Unused	(None)
INNER3	7	IN3	Unused	(None)
INNER4	8	IN4	Unused	(None)
INNER5	9	IN5	Unused	(None)
INNER6	Ctrl + 0	IN6	Unused	(None)
INNER7	Ctrl + 1	IN7	Unused	(None)
INNER8	Ctrl + 2	IN8	Unused	(None)
INNER9	Ctrl + 3	IN9	Unused	(None)
INNER10	Ctrl + 4	I10	Unused	(None)
INNER11	Ctrl + 5	I11	Unused	(None)
INNER12	Ctrl + 6	I12	Unused	(None)
SMTOP	Ctrl + 7	SMT	Doc	SMBOT
SMBOT	Ctrl + 8	SMB	Doc	SMTOP
SPTOP	Ctrl + 9	SPT	Doc	SPBOT
SPBOT	Shift + 0	SPB	Doc	SPTOP
SSTOP	Shift + 1	SST	Doc	SSBOT
SSBOT	Shift + 2	SSB	Doc	SSTOP
ASYTOP	Shift + 3	AST	Doc	ASYBOT
ASYBOT	Shift + 4	ASB	Doc	ASYTOP
DRLDWG	Shift + 5	DRD	Doc	(None)
DRILL	Shift + 6	DRL	Drill	(None)
FABDWG	Shift + 7	FAB	Doc	(None)
NOTES	Shift + 8	NOT	Doc	(None)
GND2	Shift + 9	GND2	Plane	(None)

Figure 9-41 Layer setup that defines the six-layer stack-up.

Assigning nets to layers

The next step is to assign the power and ground nets to their respective plane layers. **To assign ground and power nets to plane layers** click the View Spreadsheet button and select Nets from the pop-up to open the Nets spreadsheet. Select the GND net and then right click and select Properties from the pop-up. In the Edit Net dialog box (Fig. 9-42), click the Net Layers... button in the lower left corner. In the Layers Enabled for Routing dialog box, deselect INNER2 routing layer and select the GND plane layer. You can leave the TOP and BOTTOM routing layers enabled because traces will need to run on the top layers for a short ways from the component to the fan-out via (or bottom for bottom-mounted parts). Click OK in the Layers Enabled for Routing dialog box and then click OK in the Edit Net dialog box.



Net Name: GND

Net Attributes

☑ Routing Enabled ☑ Share Enabled ☐ Highlight

☑ Retry Enabled ☑ Sh

Group: 0

Min Width: 12.

Conn

Layers Enabled for Routing

☑ TOP ☑ BOTTOM

Plane Layers

☑ GND ☐ V+ ☐ V- ☑ GND2

Figure 9-42 Assigning power/ground nets to plane layers.

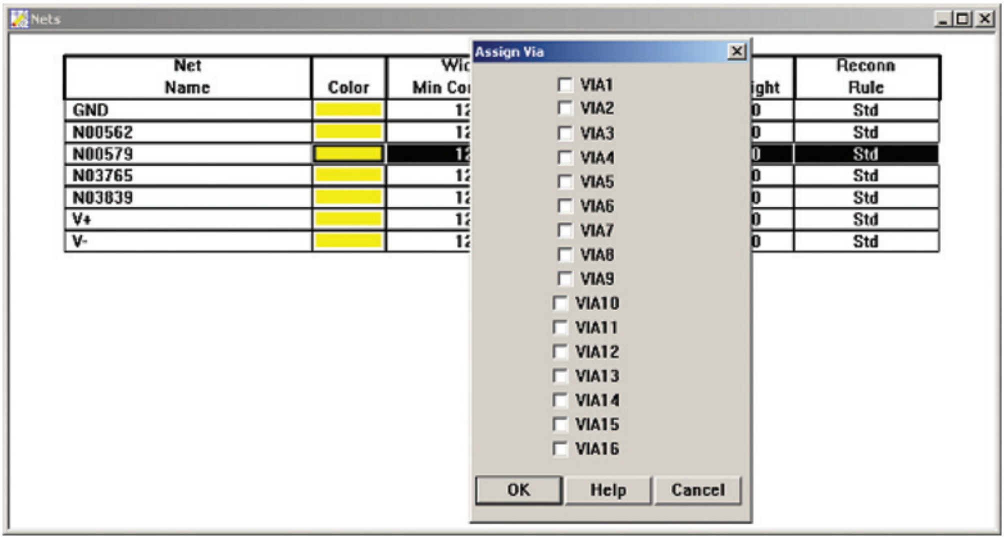
Repeat the procedure and assign the V+ and V− nets to the V+ and V− plane layers, respectively, and include the TOP and BOTTOM layers. You should now see YES* in the Routing Enabled column of the spreadsheet for each of the plane layers (at least before performing a fanout). An asterisk indicates that the net is assigned to at least one plane layer and all available routing layers. A double asterisk (**) indicates that the net has been restricted from being routed on at least one of the available routing layers.

Specifying vias for fanouts

Layout uses the default via, which is VIA1, for all routing and fanouts unless you specify otherwise. You can specify which via will be used for fanouts and which ones will be used for specific nets. To Change the default fanout via use the Fanout Settings dialog box as described below. To assign special vias to particular nets you use the nets spreadsheet (also described below). To specify a via other than the default it must be defined.

To define a new via, click the View Spreadsheets tool button and select the Padstacks option. Scroll through the list of padstacks until you find a via padstack that has not been defined (all of its properties are "0"). You can modify and use this via as an alternate via for fanouts or particular nets.

To assign a specific via to a net, click the View Spreadsheets button and select Nets from the pop-up. On the Nets spreadsheet select the net that you want to assign a particular net to. Right click and then select Assign Via per Net to display the Assign Via check box (Fig. 9-43).



Net Name	Color	Wic Min Co	ight	Reconn Rule
GND	🟨	1	0	Std
N00562	🟨	1	0	Std
N00579	🟨	1	0	Std
N03765	🟨	1	0	Std
N03839	🟨	1	0	Std
V+	🟨	1	0	Std
V-	🟨	1	0	Std

- ☐ VIA1
- ☐ VIA2
- ☐ VIA3
- ☐ VIA4
- ☐ VIA5
- ☐ VIA6
- ☐ VIA7
- ☐ VIA8
- ☐ VIA9
- ☐ VIA10
- ☐ VIA11
- ☐ VIA12
- ☐ VIA13
- ☐ VIA14
- ☐ VIA15
- ☐ VIA16

Figure 9-43 Assigning alternate vias to a net.

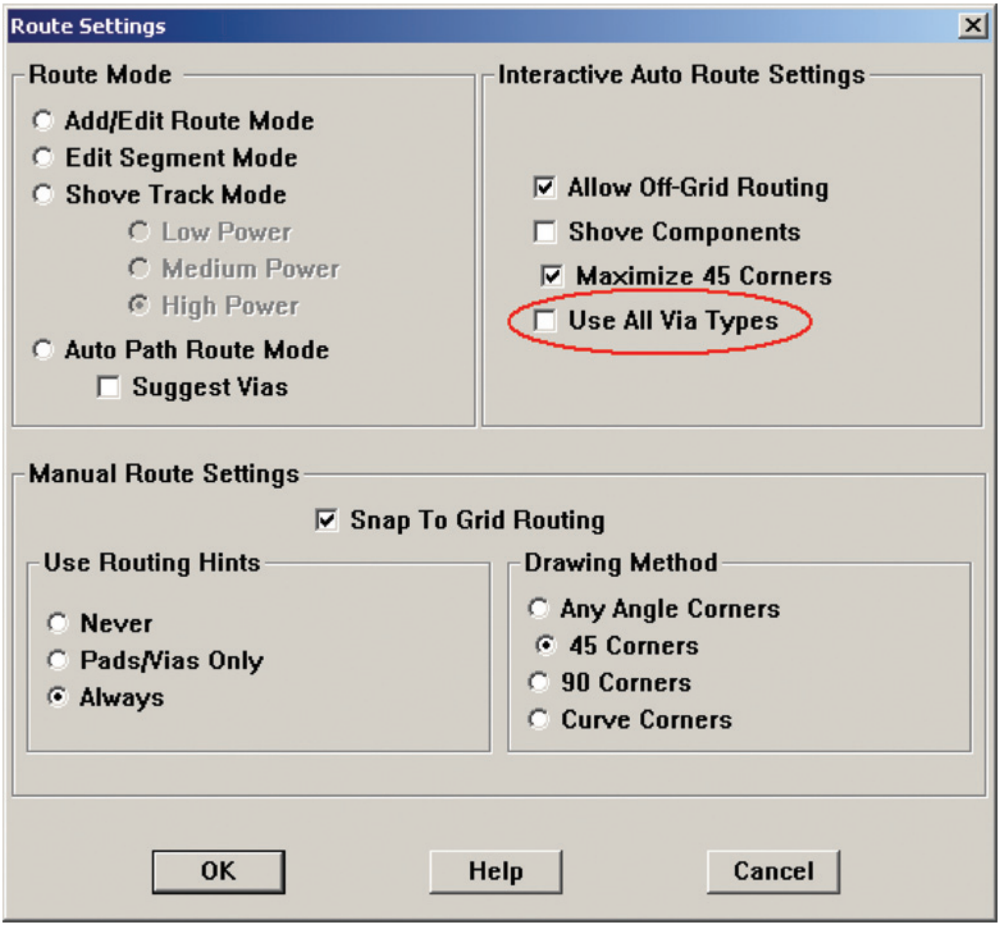
You can select more than one via for the autorouter to use, but you also need to let Layout know it is allowed to use other vias than the default via. Go to Options → Route Settings to display the Route Settings dialog box (Fig. 9-44). Check the Use All Via Types option. Layout will then use whichever via most easily accomplishes the routing task.

You can also assign a specific via to use for fanouts. **To specify a particular fan-out via**, select Fanout Settings... from the Options menu to display the Fanout Settings dialog box shown in Fig. 9-45. From there you can control both power and ground fanouts and signal fanouts. If you will be working with the fanouts a lot, you might want to disable the automatic lock after fanout feature (the default). **To disable the automatic lock after fanout feature**, deselect Lock after fanout. You may also select the Share close vias option. Click OK to close the dialog box.

Prerouting the board

Routing power and ground nets

The next step is to route the power and ground nets to their assigned planes. Since we will be working with only the power and ground nets for the moment, disable all of the other nets.



Route Mode
○ Add/Edit Route Mode
○ Edit Segment Mode
○ Shove Track Mode
○ Low Power
○ Medium Power
● High Power
○ Auto Path Route Mode
☐ Suggest Vias

Interactive Auto Route Settings
☑ Allow Off-Grid Routing
☐ Shove Components
☑ Maximize 45 Corners
☐ Use All Via Types

Manual Route Settings
☑ Snap To Grid Routing

Use Routing Hints
○ Never
○ Pads/Vias Only
● Always

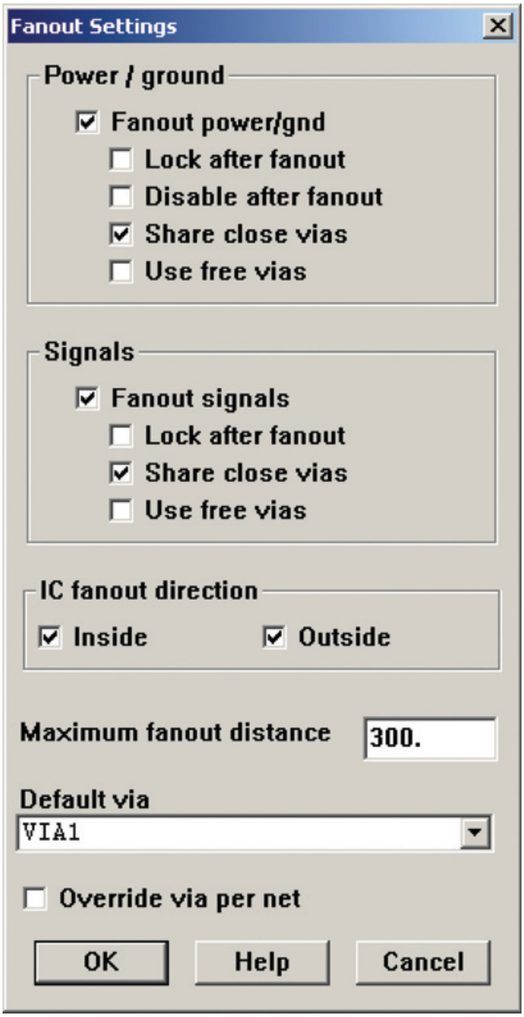
Drawing Method
○ Any Angle Corners
● 45 Corners
○ 90 Corners
○ Curve Corners

Figure 9-44 ***Route Settings*** *dialog box to specify via usage.*

Open the Nets spreadsheet and drag a box across all of the nonpower and nonground nets (cells) to select them. Right click and select Enable <-> Disable from the pop-up to toggle off the selected nets. Close the spreadsheet.

On your board layout you should notice that some of the rat's nest lines (nets) have disappeared. The only lines you should see are the power and ground lines. To identify which lines are which, enable one of the routing tool buttons (Add/Edit Route Mode, for example). Use Ctrl + left click and select one of the nets. In the bottom left corner of your screen you should see: Net "GND" Width 12... (or "V+", etc.), depending on which net you selected. Hit the Esc key on your keyboard to deselect the net.

Click the Refresh All button, . More lines will disappear. The lines that disappear are ones that are connected to through-hole pins that are connected to their respective plane layers by thermal reliefs. To view thermal reliefs make each layer active one at a time by cycling



Fanout Settings

Power / ground

☑ Fanout power/gnd
  ☐ Lock after fanout
  ☐ Disable after fanout
  ☑ Share close vias
  ☐ Use free vias

Signals

☑ Fanout signals
  ☐ Lock after fanout
  ☑ Share close vias
  ☐ Use free vias

IC fanout direction

☑ Inside ☑ Outside

Maximum fanout distance: 300.

Default via: VIA1

☐ Override via per net

Figure 9-45 Specifying fanout settings.

through the layer list. Each pin that is connected to a plane layer will have a thermal relief around it as that layer is made active as shown in Fig. 9-46. The lines that did not disappear are not connected to a plane yet because the surface-mount devices do not have a way to get to the plane(s). So the next step is to provide paths (called fanouts or stringers) for the surface-mount devices to become connected to their planes.

Fanning out power and ground

Normally it is recommended that power and ground are fanned out separately and that ground is fanned out first. Ground can usually be fanned out using the automatic fanout feature but power may need to be fanned out manually. The example below routes ground and power at the same time to illustrate why and how to fix the problems that can occur.

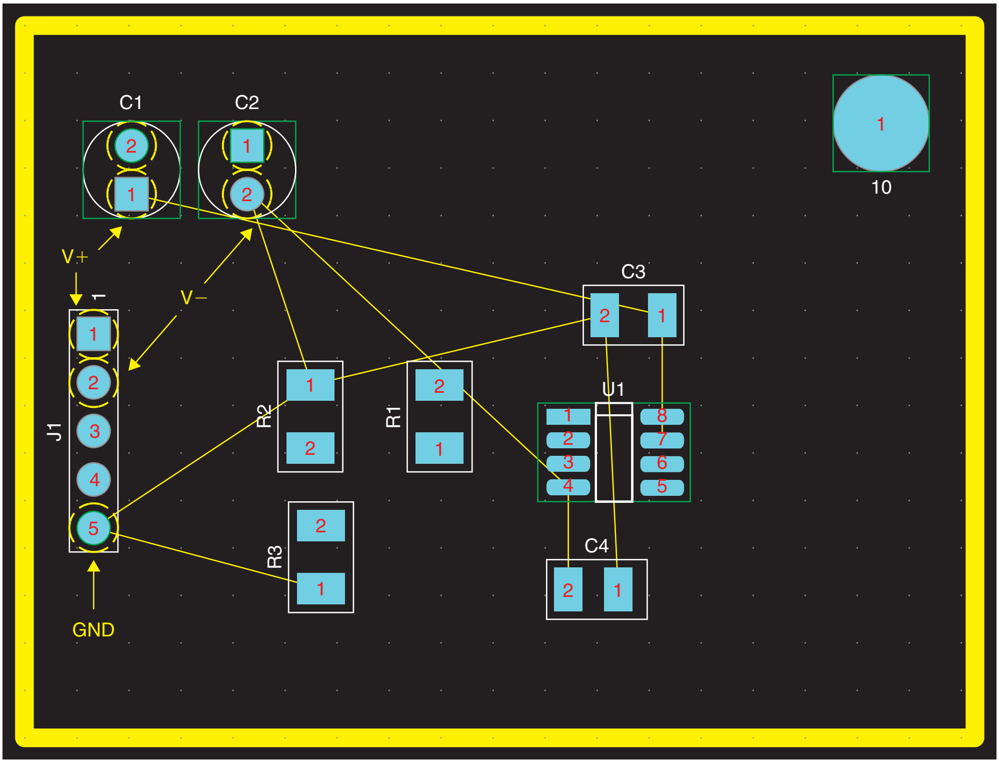


Figure 9-46 Through-hole pins connected to planes by thermal reliefs.

To fan out the surface-mounted devices, enable the ground net (and in this example the power nets), and select Auto → Fanout → Board from the menu bar. Click the Refresh All button again. All nets that are attached to plane layers should now be invisible and vias should be attached to the surface-mount devices. To verify connectivity to the planes, make each of the plane layers active one at a time by selecting them from the layer selection list. When you select a plane layer, the thermals used to connect it to the plane should become visible.

Changing colors of nets

All of the thermals are bright yellow by default. You can change the color of a thermal by changing the color of the net to which it belongs. **To change the color of a net** open the Nets spreadsheet and select the net of interest, right click, and select Change Color from the pop-up. Select the desired color from the pop-up. Click the Refresh All button and make the layer of interest active again. The thermal will be shown in the new color. Now if you select the plane layers (layers 3, 4, 5, and 29), you will see the thermals in their respective colors as shown in Fig. 9-47.

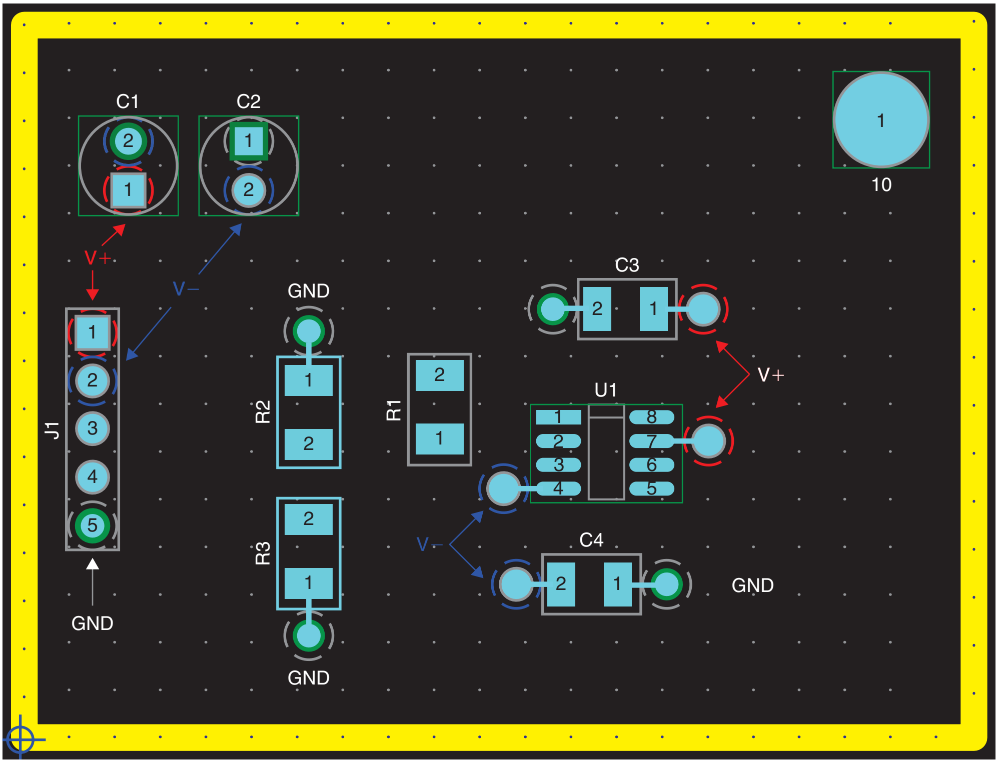


Figure 9-47 Fanned out power and ground nets in different colors.

Manually routing fanouts

When Layout fanned out the bypass capacitors vias were added to both the capacitors and the amplifier pins (see Fig. 9-47). As a result, the bypass capacitors are indirectly connected to the power pins through vias and the power plane. There are three basic methods to fanning out power pins. The first method is simply to have the capacitors near the IC's power pins and use vias on both as shown in Fig. 9-47, the second method is to route the power pin to the bypass capacitor using a "T" before the fan-out via (either across the pad or using traces) and then to the power plane as Fig. 9-48(a) shows, and the third method is to route the power pin to the power plane first by placing the fan-out via between the power pin and the bypass capacitor as shown in Fig. 9-48(b). Not everyone agrees on which method is best (see Chap. 6 for more details). Manual routing techniques will be used to fan out to the capacitors as shown in Figs. 9-48(a) and 9-48(b).

We will begin by rerouting the V− fanout by the "T" method. First the "T" will be made using traces and then the across-the-pad method will be demonstrated so that V− is similar to the fanout shown in Fig. 9-48(a).

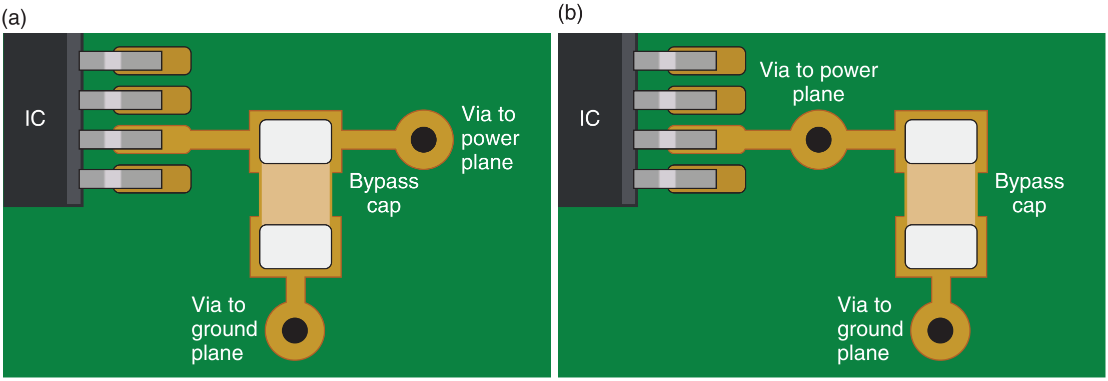


Figure 9-48 Power pin fanout methodologies. (a) "T" method (across the pad). (b) "Pin to plane" method.

Moving and unrouting fanouts

It is possible to move the vias around using the Add/Edit Route Mode or Edit Segment Mode routing tools, but it is often faster and easier to completely unroute the fanout and start over. **To unroute a fanout**, click the Add/Edit Route Mode button. Select the trace and/or via that you want to unroute, then right click, and select Unroute from the pop-up.

Fanouts and their associated traces are, by default, automatically locked after every fanout operation. If the fanout is locked and you try to unroute it, you will be asked, "Segment is LOCKED, override?" Click OK. If you need to redo many fanouts, you can disable the automatic lock after fanout option. **To disable the automatic lock after fanout option** choose Options → Fanout Settings. From the Fanout Settings dialog box you can control the various fanout options by checking the appropriate boxes. After a fanout has been unrouted, make sure the net is enabled (open the Nets spreadsheet and enable it if necessary) so that the rat's nest is visible and routable.

To route a "T" fanout manually using traces (as shown in Fig. 9-49(a)) select the Add/Edit Route Mode button (also make sure the Online DRC tool is off). Step 1: Click on the rat's nest near the IC's power pin, draw a trace outward from the pin, and left click to create a vertex a short distance from the pin (this ensures a good pad exit and will allow the routing tool to place subsequent traces on the routing grid). Extend the trace out to the desired via location, left click to place a vertex, right click and select Add Free Via (or a standard Via) from the pop-up, right click again and select End Command from the pop-up. Step 2: Click on the rat's nest near the capacitor's pad, draw a trace outward from the pad and left click a short distance from the pad to create a vertex (ensures a good pad exit). Continue the trace from the capacitor pad toward the trace (the IC pin-to-via trace) and left click on the trace to create the "T". If the "T" makes a good connection the routing tool will automatically become inactive. If the "T" cannot be made on a routing grid point the routing tool may persist. If so place a vertex (left click) as close to the existing trace as possible, right click and select Finish from the pop-up. The routing tool will do its best to create a clean "T", but a slight

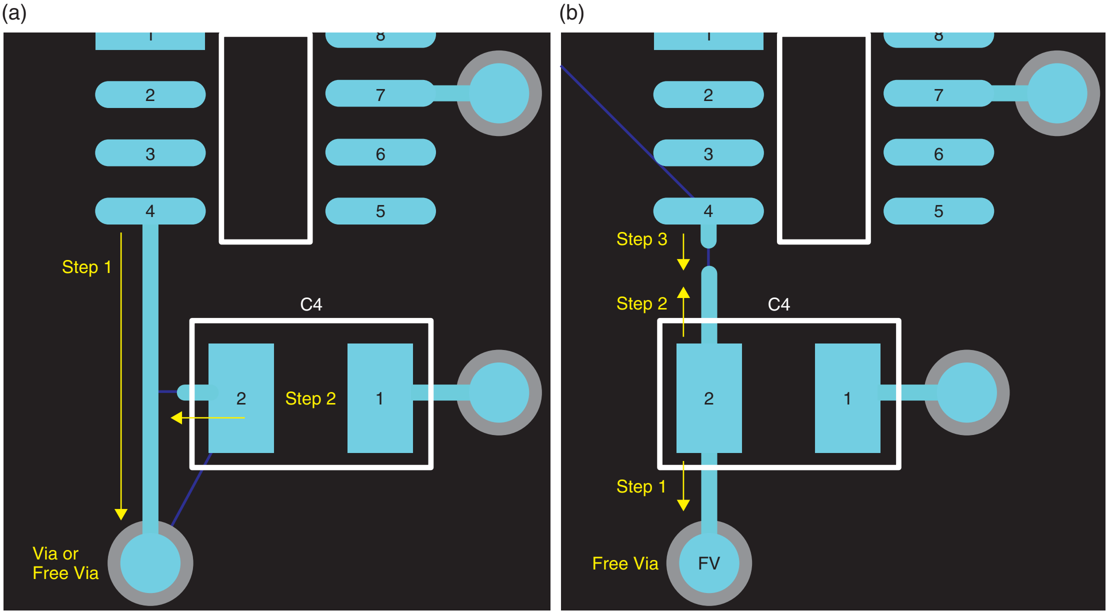


Figure 9-49 Manually routing fanouts from power pins. (a) The "T" method with traces. (b) "Across the pad" method.

jog may result. You can either use the Edit Segment Mode to remove the jog or use the Component tool to move the capacitor to an on-grid location and then remove the jog.

When routing a fanout using this method you can usually use a standard via. However, occasionally Layout may unroute them if it thinks they are unnecessary. To prevent this, use a free via because Layout will leave free vias alone since it considers them to be part net and part component (Note: if you are using the Demo version Layout will not let you place free vias if you have more than 10 parts on the board). Using free vias is demonstrated next.

Using free vias

To route a fanout across a pad manually as shown in Fig. 9-49(b) select the Add/Edit Route Mode button. Step 1: Click on the rat's nest near the capacitor's pad and draw a trace outward from the pad and left click to end the trace at the desired via location. Right click and select Add Free Via from the pop-up, right click again, and select End Command from the pop-up. Step 2: Click on the rat's nest near the capacitor's pad and draw a trace outward from the IC's power pin. If the routing tool tries to route from the IC pin instead of the capacitor, right click and select Exchange Ends from the pop-up. Left click to end the trace a short distance from the pad, right click again, and select End Command from the pop-up. Step 3: Click on the rat's nest near the power pin and draw a trace outward from the pin. Left click to create a vertex a short distance from the pin, right click, and select Finish from the pop-up. The reason for routing the fanout with three segments instead of one long segment is to prevent bad pad exits (described below in the miscellaneous section).

The V+ fanout to C3 will be routed using the pin-to-plane method shown in Fig. 9-48(b). The finished fanout is shown in Fig. 9-50. First unroute the fanouts and delete the vias for C3 as described above. Begin the fanout at the IC pin. Step 1: Click on the rat's nest near the IC's power pin (pin 7), draw a trace outward from the pin, and left click to create a vertex at the desired via location, left click to tack the end, right click and select Add Free Via from the pop-up, right click again and select End Command from the pop-up. Step 2: Click on the rat's nest near the capacitor's pad, draw a trace outward from the pad, and left click a short distance from the pad to create a vertex (ensures a good pad exit). Right click and select Finish from the pop-up. You can use the Edit Segment Mode to remove the jog or use the Component tool to move traces or vertices as necessary.

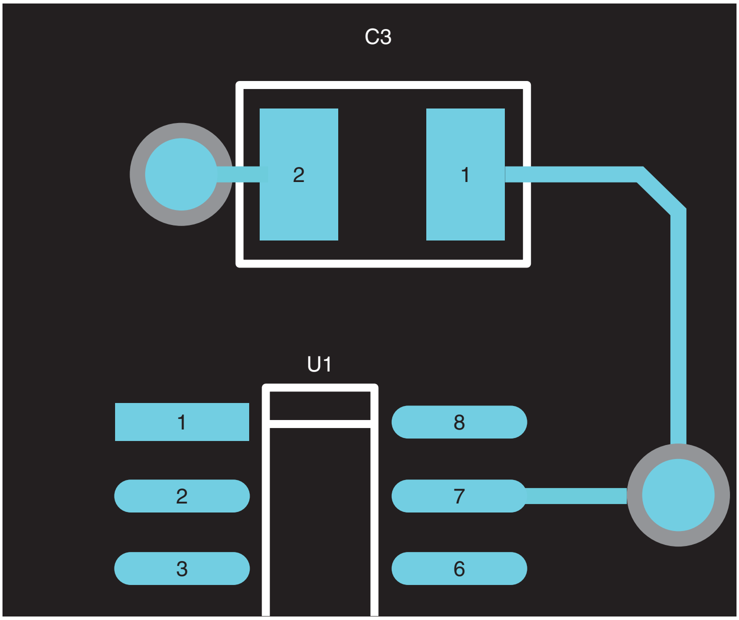


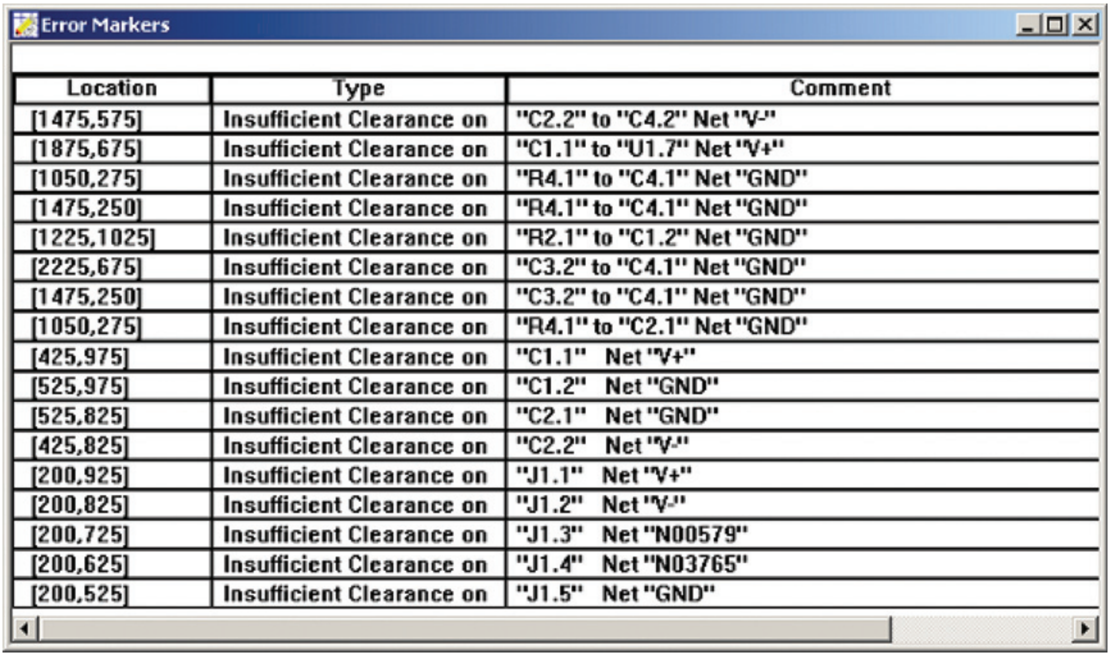
Figure 9-50 A completed pin-to-plane fanout method.

Locking traces

Once the manual fanouts are completed you can lock them to prevent them from being inadvertently unrouted. **To lock traces**, select one of the manual routing tools and select the net (a trace or a via) by left clicking on the trace while holding down the Ctrl key (to prevent moving the trace). Right click and select Lock from the pop-up. As long as a net is enabled, you can continue routing traces even if it is locked. Disabling a net prevents it from being routed, while locking a trace (or via) prevents it from being unrouted.

Viewing DRC errors

Before autorouting the board, perform another DRC. Press the button. The DRC should report about 19 errors. The errors are marked on the board by circled X's. The markers are color coded according to the layers on which the errors have occurred. You can check to see which layers contain error markers by making each layer the active layer (use the Layer selection list or the number pad on your keyboard). You can also view a description of the errors. **To view the error descriptions**, click the View Spreadsheet button and select Error Markers. Figure 9-51 shows an example of the error spreadsheet.



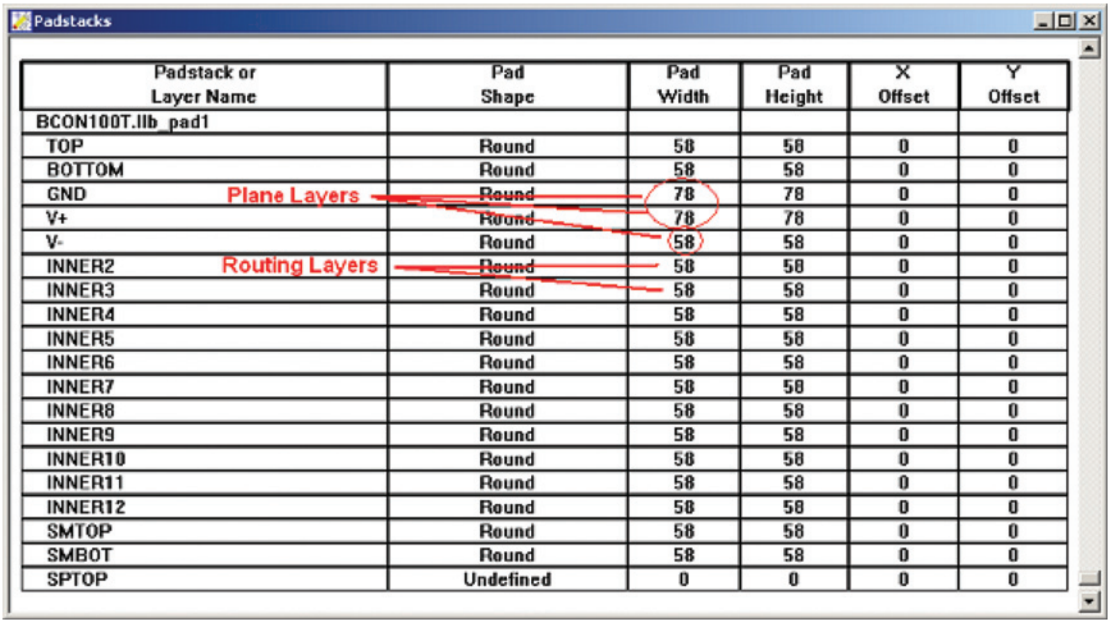
Location	Type	Comment
[1475,575]	Insufficient Clearance on	"C2.2" to "C4.2" Net "V-"
[1875,675]	Insufficient Clearance on	"C1.1" to "U1.7" Net "V+"
[1050,275]	Insufficient Clearance on	"R4.1" to "C4.1" Net "GND"
[1475,250]	Insufficient Clearance on	"R4.1" to "C4.1" Net "GND"
[1225,1025]	Insufficient Clearance on	"R2.1" to "C1.2" Net "GND"
[2225,675]	Insufficient Clearance on	"C3.2" to "C4.1" Net "GND"
[1475,250]	Insufficient Clearance on	"C3.2" to "C4.1" Net "GND"
[1050,275]	Insufficient Clearance on	"R4.1" to "C2.1" Net "GND"
[425,975]	Insufficient Clearance on	"C1.1" Net "V+"
[525,975]	Insufficient Clearance on	"C1.2" Net "GND"
[525,825]	Insufficient Clearance on	"C2.1" Net "GND"
[425,825]	Insufficient Clearance on	"C2.2" Net "V-"
[200,925]	Insufficient Clearance on	"J1.1" Net "V+"
[200,825]	Insufficient Clearance on	"J1.2" Net "V-"
[200,725]	Insufficient Clearance on	"J1.3" Net "N00579"
[200,625]	Insufficient Clearance on	"J1.4" Net "N03765"
[200,525]	Insufficient Clearance on	"J1.5" Net "GND"

Figure 9-51 Viewing Error Markers.

The list of errors may look formidable, but as you will soon see, one problem often causes several errors. By looking for patterns between the comments on the error spreadsheet and the layers on which the errors have occurred, you should be able to get an idea of the problems.

Most of the error markers (if not all) will be bright green and located on the IN1 layer. The INNER1 layer is the V− power plane layer, which was originally a routing layer. All of the errors on the INNER1 layer involve pins and plane layers. Based on these clues, the first place to look might be the padstack settings for layer V− (INNER1).

To view padstack settings activate the Pin tool, ① and select a pin with an error marker (e.g., one of the round pins on J1). Open the Padstacks spreadsheet. The Padstacks spreadsheet is shown in Figure 9-52 for one of the round pads (pins 2–5) on J1. Notice that the pads for layers GND and V+ (which was originally called PWR) are 20 mils larger than the pads on all of the other layers. Remember that “pads” on plane layers are actually *clearances*. Recall also that we renamed layer INNER1 to V− and changed it from a routing layer to a plane layer. Notice too that V−’s pad clearance is 20 mils smaller than the other plane layers because it still has the routing layer dimensions. Therefore, the first step is to change the V− pads from routing dimensions to clearance dimensions. This can be done manually or by copying pad properties from another layer.



Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
BCON100T.llb_pad1					
TOP	Round	58	58	0	0
BOTTOM	Round	58	58	0	0
GND	Round	78	78	0	0
V+	Round	78	78	0	0
V-	Round	58	58	0	0
INNER2	Round	58	58	0	0
INNER3	Round	58	58	0	0
INNER4	Round	58	58	0	0
INNER5	Round	58	58	0	0
INNER6	Round	58	58	0	0
INNER7	Round	58	58	0	0
INNER8	Round	58	58	0	0
INNER9	Round	58	58	0	0
INNER10	Round	58	58	0	0
INNER11	Round	58	58	0	0
INNER12	Round	58	58	0	0
SMTOP	Round	58	58	0	0
SMBOT	Round	58	58	0	0
SPTOP	Undefined	0	0	0	0

Figure 9-52 Errors caused by padstack settings on a defined plane layer.

Changing padstack properties

To change pad dimensions manually double click the cell for the V− layer, right click, and select Properties to display the Edit Padstack Layer dialog box. Change the Pad Width and Pad Height values to match the other plane layers (78 mils) and click OK.

Alternatively, you can automatically copy the pad properties of one of the default plane layers into the V− layer. **To copy the pad properties of one layer to another layer**, select the V− cell, right click, and select Copy Layer... from the pop-up. The Copy Padstack Layer dialog box is shown in Fig. 9-53. Select one of the default plane layers (V+ or GND) as the source layer and select V− as the target layer. Leave the oversize setting at 0 and click OK. The pad on layer V− will now have the same properties as the pad on the V+ layer. You can perform this operation on a single padstack (selecting only the row for a specific padstack) or the entire design (by selecting the entire padstack name column). Note that after changing the pad dimensions you may have to deselect the cell(s) in order for the spreadsheet to be visibly updated.

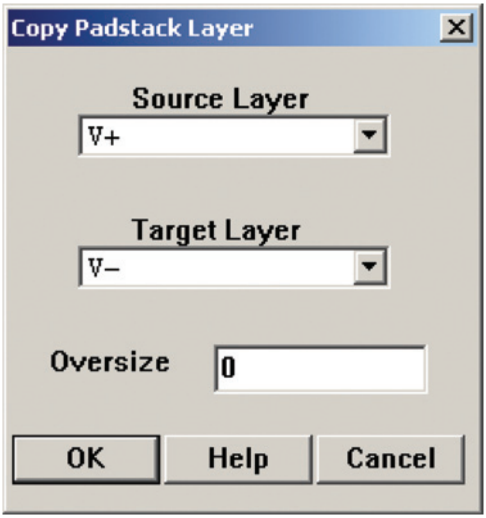


Figure 9-53 Copying plane-type padstack layers.

If the second ground plane had been generated by converting another routing layer (INNER2, for example) into a plane layer it would have had the same errors and the same process could have been used to fix the errors (i.e., copy all GND padstack layers into the GND2 padstack layers). However, since the GND2 layer was produced by copying the GND layer during the layer setup process, GND2 inherited exact copies all of the properties of the GND PLANE layer. Since V− was declared a generic PLANE layer it did not inherit any particular plane layer properties; it just became a negative plane that makes connections to padstacks using thermal reliefs.

Another error that might exist is the “off-grid via” error. To fix this error you can either use one of the manual routing tools to move the via onto a grid point or change the via grid settings to a smaller value (including 0). **To change the via grid settings**, select System Settings from the Options menu. Change the value in the Via grid: box as required and click OK.

Another error that might exist is the “bad pad exit” error. See the section at the end of this chapter on how to correct bad pad exits.

Autorouting the board

Once the power and ground connections and any critical traces have been prerouted and all errors eliminated, you can let the autorouter route the rest of the board. Before running the autorouter make sure to disable and lock the ground and power nets and enable the signal nets using the Nets spreadsheet.

Controlling the route box

The autorouter routes the board in areas defined by the DRC box. You have the option of telling the autorouter to route the entire board or to route only the area defined by the DRC box (which enables you to route the board in controlled increments). When you tell the autorouter to route the whole board the autorouter routes the area defined by the DRC box and then automatically moves the box to the next location (as defined in the routing strategy settings) and continues routing there. You can specify the size of the DRC box and the location where the autorouter should begin routing. For simple board designs (as in the examples here) it is usually not necessary to change the DRC autoroute box settings, but for larger and more complex boards you may want to have more control of the autorouter box.

To display the DRC box (if not already displayed), toggle the Online DRC button, DRC. Once the DRC box (the dotted rectangle) is displayed you can change the size and starting location of the box. **To define the size of the DRC box**, select Zoom DRC/Route Box from the View menu. The cursor shape changes to the zoom cursor (a "Z") and behaves like the zoom cursor. Click and drag the pointer to outline the new DRC box. In addition to the DRC box being drawn, the view will also be zoomed to the size of the new DRC box. To zoom out again toggle the Zoom All button, 🔍 or hit the O key on your keyboard. The view will be zoomed back out, but the size of the DRC box will be unchanged. **To move the DRC box**, select Zoom DRC/Route Box from the View menu. Move the "Z" cursor to the center of the area where you want DRC box to be located and press the "*" key on the keyboard's numeric keypad. The "Z" cursor will persist so that you can continue moving the DRC box. Once the DRC box is in the correct position, right click and select End Command from the pop-up. If you want to move the DRC box and zoom in at the same time click the left mouse button instead of pressing the "*" key.

Loading and editing a routing strategy file

Routing strategy files influence how the autorouter goes about routing your board. The strategy files are located in Layout's Data folder. The contents of the strategy file are not readable directly, but a strategy file's parameters can be viewed and modified with the route strategies dialog boxes and spreadsheets. **To view routing strategy parameters** select Route Strategies from the Options menu. From the Route Strategies menu you can view the Manual Route Strategy dialog box and the Route Layer, Route Sweep, and Route Passes spreadsheets. Unless your board has unique routing requirements these parameters should not be changed (see the *Note* below about the Route Pass Done flag) because some changes can adversely affect the operation of the autorouter. If your board requires nonstandard routing parameters it is better to use one of the specialized strategy files in place of the standard strategy file (STD.SF). The various routing strategy files are described in Chap. 4 of the *Layout User's Guide* (lay_ug.pdf located in OrCAD 10.5 doc folder). **To load a strategy file** choose Load... from the File menu from your design window's menu bar.

Note

- *the **Route Pass spreadsheet** contains one parameter that you may need to change on occasion. It contains a flag that tells the autorouter if the DRC route box has completed routing all areas of the board. Once the flag is set, the autorouter will not attempt to route the board again. If after completing a board route, you need to unroute some of the board (say, for example, to move parts around) and then have the autorouter reroute the nets, you have to clear the "done" flag first (see Fig. 9-56).* **To clear the Route Pass Done flag,** *select **Route Strategies** from the **Options** menu and choose **Route Passes** to display the **Route Pass** spreadsheet. Select the **Enable** column, right click, and select **Properties**... from the pop-up. Uncheck the **Done** box in the **Edit Route Pass** dialog box and click **OK.** All of the route pass types will be reenabled, allowing the autorouter to run again.*

Running the autorouter

Once you are satisfied with the prerouting and the autorouter setup you can **start the autorouter** by selecting Auto → Autoroute → Board from the menu bar. The autorouter will begin routing the board. When the autorouter has finished routing the board, it will inform you, "All sweeps completed (or disabled)." This sets the "done" flag as described above.

Finalizing the design

Postrouting inspection

After the autorouter has finished routing the board, it should be checked for problem areas such as acute angles, long parallel traces, and bad via locations. Chapter 6 discusses several these and other routing issues. It is a good idea to perform another DRC to check for new errors that may have been caused by the routing process.

Depending on how you placed your parts your board might look something like Fig. 9-54. It may be necessary to move or unroute traces using the manual routing tools.

Checking routing statistics

Once you have all of the traces routed, you can view a statistics report (see Fig. 9-55) to make sure nothing was missed. Click the Spreadsheet button and select Statistics from the menu. Make sure that it shows 100% routed.

If it shows it is something like 99.8% routed, but the board looks like it is completely routed then there is a small segment of rat's nest between two routed segments or between a segment and a pad (probably under the pad, making it hard to see) that has not been routed.

To find the unrouted segment hit the Backspace key on your keyboard to clear the display, and then hit the 0 (zero) key to show only the global layer. All unrouted traces are on the global layer and should show up as small yellow segments (for layers that are enabled).

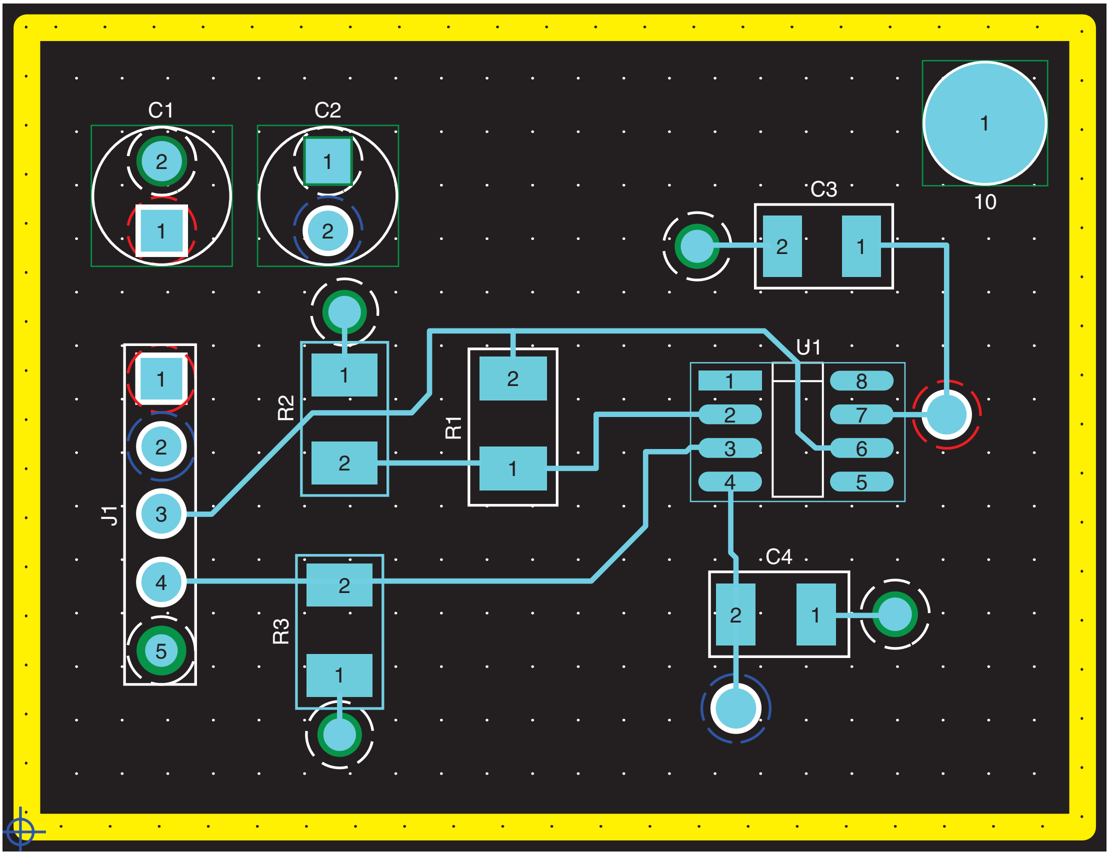


Figure 9-54 Board after autorouting.

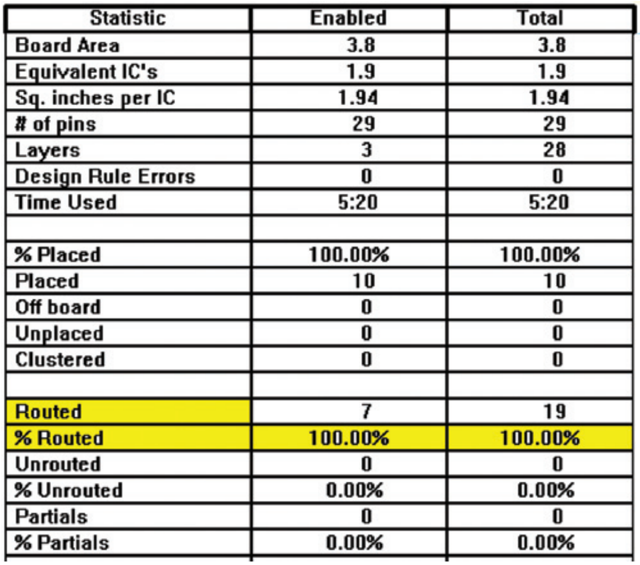
You can either route the segment manually or try to reroute the board using the autorouter. If the autorouter responds with the message, “All sweeps completed or disabled,” it thinks there is nothing to do because the routing flags have all been set to “done.”

To clear the autorouter’s “done” flags, toggle the Spreadsheets button and then select Strategy → Route Pass to bring up the Route Pass spreadsheet. Select the entire Enable column and then right click and select Properties from the pop-up. Clear the Done checkmark in the Edit Route Pass dialog box as shown in Fig. 9-56. Click OK and close the spreadsheet. You should now be able to route the board with the autorouter again.

Check the statistics again to make sure everything has been routed. You can do a Cleanup Design and do one last DRC.

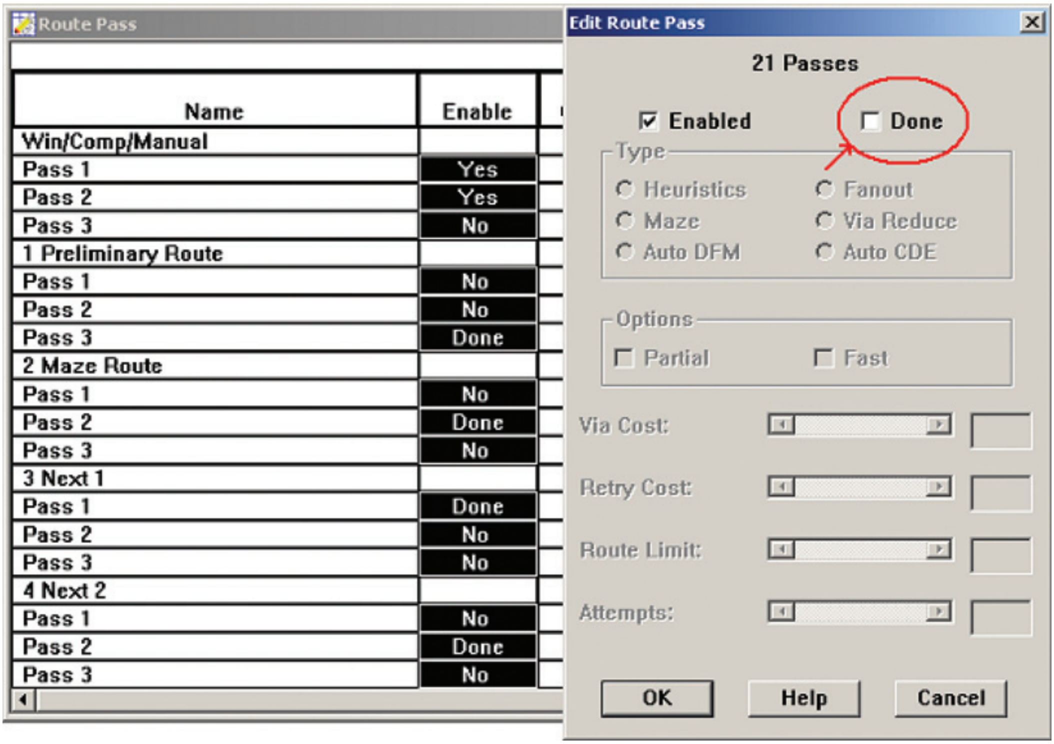
Synchronizing the design with Capture (back annotation)

Once the board has been completely routed, you can export information from your PCB layout (such as component location) to your schematic by performing a back annotation. To see the



Statistic	Enabled	Total
Board Area	3.8	3.8
Equivalent IC's	1.9	1.9
Sq. inches per IC	1.94	1.94
# of pins	29	29
Layers	3	28
Design Rule Errors	0	0
Time Used	5:20	5:20
% Placed	100.00%	100.00%
Placed	10	10
Off board	0	0
Unplaced	0	0
Clustered	0	0
Routed	7	19
% Routed	100.00%	100.00%
Unrouted	0	0
% Unrouted	0.00%	0.00%
Partials	0	0
% Partials	0.00%	0.00%

Figure 9-55 Board statistics spreadsheet.



Route Pass

Name	Enable
Win/Comp/Manual	
Pass 1	Yes
Pass 2	Yes
Pass 3	No
1 Preliminary Route	
Pass 1	No
Pass 2	No
Pass 3	Done
2 Maze Route	
Pass 1	No
Pass 2	Done
Pass 3	No
3 Next 1	
Pass 1	Done
Pass 2	No
Pass 3	No
4 Next 2	
Pass 1	No
Pass 2	Done
Pass 3	No

Edit Route Pass

21 Passes

☑ Enabled ☐ Done

Type
○ Heuristics ○ Fanout
○ Maze ○ Via Reduce
○ Auto DFM ○ Auto CDE

Options
☐ Partial ☐ Fast

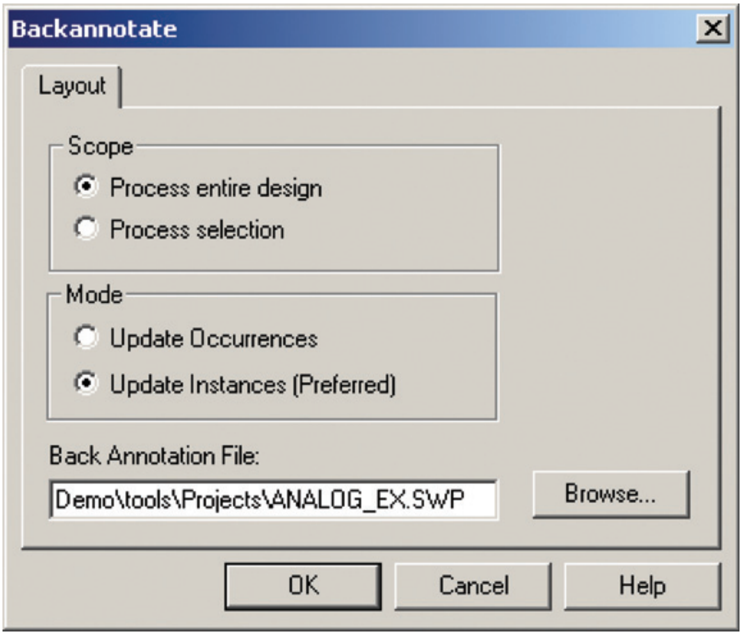
Via Cost:
Retry Cost:
Route Limit:
Attempts:

Figure 9-56 Clearing Route Pass flags to redo autoroute.

effects of back annotation, first go back to Capture and double click one of the components (the op-amp for example). Select OrCAD—Layout from the Filter by: selection list. You will see that just a few of the cells have data in them. Next, do a back annotation and see what happens.

To perform a back annotation from Layout to Capture go to the PCB design in Layout and select Back Annotate from the Auto menu. Take note of the .SWP file displayed in the information box, click OK, and save the .MAX file.

Go back to the design in Capture again and select the Design icon in the Project Manager. Go to Tools menu and select Back Annotate. Use the default settings and make sure you have the correct .SWP file as shown in Fig. 9-57. Click OK.



Backannotate

Layout

Scope
● Process entire design
○ Process selection

Mode
○ Update Occurrences
● Update Instances (Preferred)

Back Annotation File: Demo\tools\Projects\ANALOG_EX.SWP

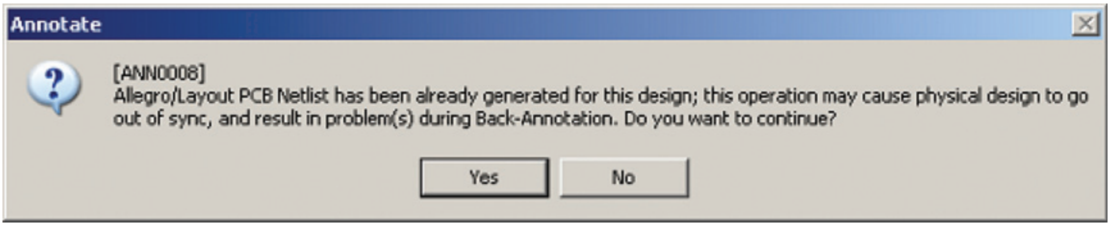
Figure 9-57 Setting up back annotation settings in Capture.

On the schematic in Capture double click on the part that you looked at before you did the back annotation and see how the spreadsheet has changed. The locations and orientation of the parts on the board (and any new footprints, etc.) will be listed in Capture. If you want (or need) to start a new board layout, all of this information will be included with the .MNL file and imported into the new .MAX file, which means that you would not have to start over again placing all of the components from the pile.

Warning!

- *Do* ***NOT*** *perform an annotation in Capture after you have back annotated the board from Layout to Capture. If you do you will get the warning shown in*

Fig. 9-58. If the design goes out of sync, you may have to rename all of the components and reenter all of the values on the schematic. You will likely have to make a new.MNL file and start over with a new board in Layout. One way that is guaranteed to cause your design to become unsynchronized is to renumber the parts in Layout and then back annotate to Capture.



[ANN0008]
Allegro/Layout PCB Netlist has been already generated for this design; this operation may cause physical design to go out of sync, and result in problem(s) during Back-Annotation. Do you want to continue?

Figure 9-58 Forward annotation warning.

This completes the first example. At this point you would postprocess the board and send it off to a board house for manufacturing. We will look at this in greater detail in Chap. 10.

Example 2: Mixed Analog/Digital Design Using Split Power, Ground Planes

The next example shows how to design a circuit with a mixture of analog and digital parts with multiple power planes and with a single ground plane split into analog and digital sections that have a common reference point.

Mixed-signal circuit design in Capture

Figure 9-59 shows the circuit design example. The circuit consists of a mixture of analog and digital parts (both heterogeneous and homogeneous), multiple power sources, and separate analog/digital grounds. It has an off-board connector, an analog signal conditioning circuit (the op-amp U1), an analog-to-digital converter (U2), a digital microcontroller (U3), and a digital serial-to-parallel shift register (U4). Note that the bypass capacitors have been omitted to accommodate the Demo part count limitations.

The circuit has five global power nets, which include analog power (V+, V−) and analog ground (AGND) for U1 and U2, and +5V digital power (VCC) and digital ground (GND) for U3 and U4. Analog and digital grounds are often kept separate to help prevent digital switching noise from affecting the analog ground. But in order for the circuit to work (especially when using analog-to-digital and digital-to-analog converters) the two grounds must have a common reference point. The two grounds are tied together through a low-impedance, single point connection at the connector.

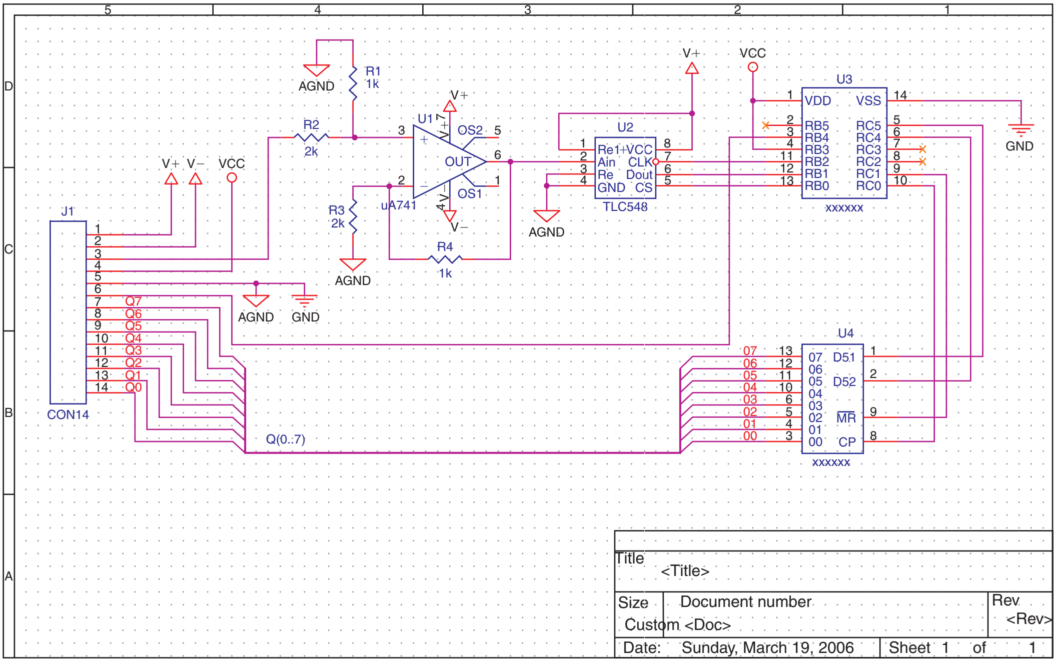

5
4
3
2
1
D
C
B
A
AGND
R1
1k
R2
2k
V+
U1
7
OS2
5
3
+
OUT
6
2
−
OS1
1
4
V−
uA741
R3
2k
AGND
R4
1k
V+ V− VCC
J1
1
2
3
4
5
6
7 Q7
8 Q6
9 Q5
10 Q4
11 Q3
12 Q2
13 Q1
14 Q0
CON14
AGND
GND
Q(0..7)
V+
VCC
U2
1 Re1+VCC 8
2 Ain CLK 7
3 Re Dout 6
4 GND CS 5
TLC548
AGND
U3
1 VDD VSS 14
2 RB5 RC5 5
3 RB4 RC4 6
4 RB3 RC3 7
11 RB2 RC2 8
12 RB1 RC1 9
13 RB0 RC0 10
xxxxxx
GND
U4
07 13 07 D51 1
06 12 06
05 11 05 D52 2
04 10 04
03 6 03
02 5 02 MR 9
01 4 01
00 3 00 CP 8
xxxxxx
Title
<Title>
Size
Custom
Document number
<Doc>
Rev
<Rev>
Date: Sunday, March 19, 2006
Sheet 1 of 1

Figure 9-59 Mixed-signal schematic design in Capture.

The procedures and tools described in the first example are used to start a new project, place the parts onto the schematic page, connect the parts, and assign footprints. Table 9-6 lists the parts used and the footprint assignments.

Reference	Part	Part Library	Footprint
J1	CON14	..CAPTURE\LIBRARY\CONNECTOR.OLB	BLKCON.100/VH/TM1SQ/W.100/14
R1,R4	1k	..CAPTURE\LIBRARY\DISCRETE.OLB	SM/R_1210
R2,R3	2k	..CAPTURE\LIBRARY\DISCRETE.OLB	SM/R_1210
U1	uA741	..CAPTURE\LIBRARY\PSPICE\EVAL.OLB	SOG.050/8/WG.244/L.225
U2	TLC548	..CAPTURE\LIBRARY\USERLIB\CHAPTER9.OLB	SOG.050/8/WG.244/L.225
U3	PIC16C505	..CAPTURE\LIBRARY\USERLIB\CHAPTER9.OLB	DIP.100/14/W.300/L.800
U4	CD74HC164	..CAPTURE\LIBRARY\USERLIB\CHAPTER9.OLB	SOG.050/14/WG.244/L.350

Table 9-6 Design parts list and schematic and footprint libraries

There are a couple of significant differences between this and the last example. The differences include:

1. All analog parts and some digital parts have explicit connections to power and ground nets, while the shift register is connected to the digital power and ground globally as described below.
2. Two different ground symbols (CAPSYMs) are connected to one net.
3. Some of the connections are made with a bus rather than wires.

Power and ground connections to digital and analog parts

Digital gates from the Capture libraries have *nonvisible (invisible)* power and ground pins. Their power pins are named VCC and their ground pins are named GND. Connecting a wire to an invisible power pin does nothing. Connections from nets to invisible power pins can be made only through **global net names** (made global by CAPSYM power or ground symbols or off-page connectors). So the power pin VCC on U4 (CD74HC164) is connected to the schematic's VCC symbol by the name "VCC" and the ground pin is connected to the digital ground symbol by the name "GND."

To connect a digital gate's ground pin to a ground net in your schematic, you have to either name the digital ground net "GND" or change the name of the digital gate's ground pin to match the name you assigned to the digital ground net (e.g., DGND instead of GND)—this is required for all digital gates. It is easiest to use the default GND name for the digital ground.

Most other Capture parts use either *visible power pins* or *input or passive pins* for power and ground. And instead of using VCC and GND as names of the power pins, they often use V+ and V−, or VDD and VSS. When parts use visible power and ground pins you can either take advantage of their global nature (and simply use their names to make connections to global nets as in the analog example) or make direct connections to the pins with wires. When parts use input or passive pins for power and ground, you have to make explicit connections (using wires) between the pins and the power or ground nets. Said another way, you *cannot* make connections to invisible power pins, and you *have* to make connections to pins that are not power pins; but visible power pins may have *either* wired or global connections to them. When you make an explicit connection to a visible power pin with a wire, the pin becomes connected to that net (the name of the wire) regardless of the name of the pin.

Connecting separate analog and digital grounds to a split plane

The CAPSYM power and ground symbols are global in nature and share characteristics of nonvisible power pins (i.e., connections to nets can be made by name or by physical connections). Figure 9-60 shows how the analog and digital grounds are named and displayed. Two different CAPSYM symbols are used with distinct names to differentiate the two ground systems. The analog parts of the circuit are referenced to the analog ground (AGND) symbol and the digital components are referenced to the digital ground (GND) symbol. At some point the two grounds need to be connected together in order for the analog-to-digital converter to work correctly (particularly with single ended inputs). At the connector the two grounds may

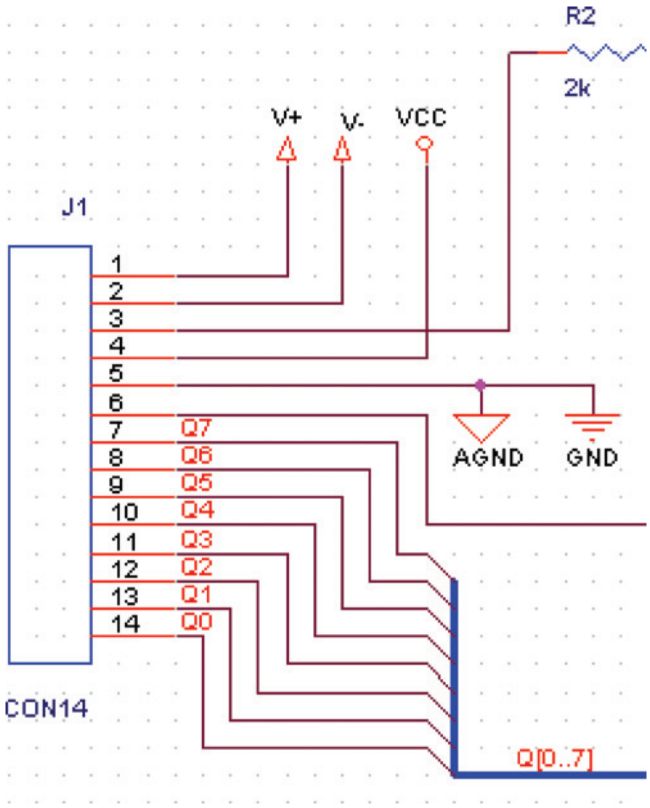
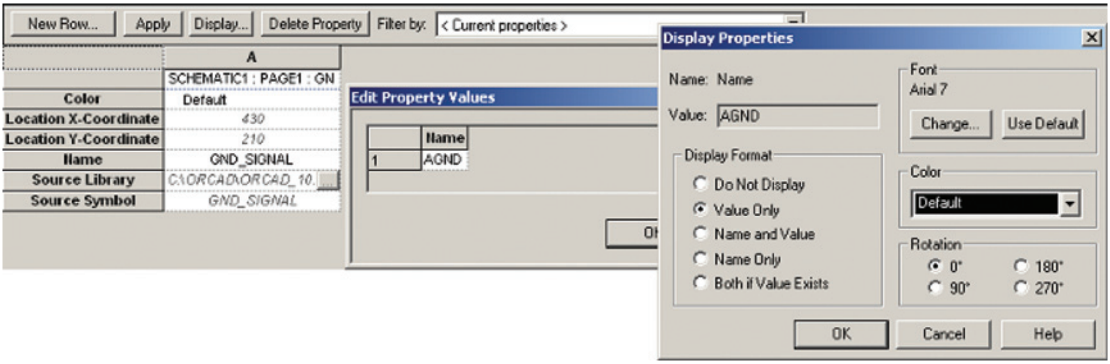


Figure 9-60 Connection of the analog and digital grounds.

leave the board separately and be connected at the power supply, or they may be connected at a pin (or pins) and leave the board together as one common ground. In this example the two grounds are connected at pin 5.

To place the analog and digital ground symbols use the Place Ground tool, GND and select the desired ground symbols. To change the symbol's name select the ground symbol (for example, from GND_SIGNAL to AGND), select the symbol on the schematic page to highlight it, right click, and select Properties from the pop-up to display the properties spreadsheet (see Fig. 9-61(a)). Select the Name row, right click, and select Edit from the pop-up to display the Edit Property Values dialog box. Enter the new name of the ground symbol and click OK. **To display the name of the symbol** on the schematic page click the Display button on the top of the spreadsheet and select the appropriate radio button on the Display Properties dialog box (Fig. 9-61(b)).

Place the second ground symbol and rename it (if applicable). Use the Wire tool to connect the two ground symbols together and then to the connector pin. The two ground symbols were distinct global nets until they were connected by the wire (net). Nets typically have names


New Row...
Apply
Display...
Delete Property
Filter by:
< Current properties >
Edit Property Values
OK
Display Properties
Font
Change...
Use Default
Color
Rotation
OK
Cancel
Help

	A
	SCHEMATIC1 : PAGE1 : GN
Color	Default
Location X-Coordinate	430
Location Y-Coordinate	210
Name	GND_SIGNAL
Source Library	C:\ORCAD\ORCAD_10.
Source Symbol	GND_SIGNAL

	Name
1	AGND

Name: Name

Value: AGND

Font: Arial 7

Color: Default

Display Format

○ Do Not Display
● Value Only
○ Name and Value
○ Name Only
○ Both if Value Exists

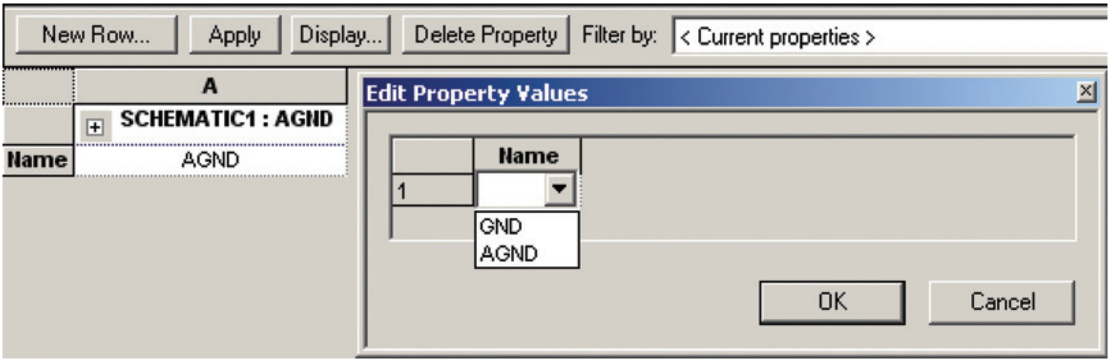
Rotation

● 0°
○ 90°
○ 180°
○ 270°

Figure 9-61 (a) Change a ground/power symbol's name and (b) display it.

such as N04432 unless they are connected to a global net or symbol, then they take on the global name. A net can have only one name, and since the net just placed is connected to two global symbols with different names, it has to pick one of them (it decides alphabetically).

To select the name of a global net double click the net (or select the net and right click and select Properties), to display the Schematic Net Properties spreadsheet (Fig. 9-62), select the Name row, right-click, and select Edit to display the Edit Property Values dialog box. Use the dropdown selection list to choose which name the net should go by. Click OK and then close the spreadsheet.


New Row...
Apply
Display...
Delete Property
Filter by:
< Current properties >
Edit Property Values
OK
Cancel

	A
	SCHEMATIC1 : AGND
Name	AGND

	Name
1	

GND
AGND

Figure 9-62 Select ground net name (analog or digital).

It appears on the schematic that the analog and digital grounds are separate ground systems and that they are connected only at J1. As far as Capture is concerned, they are actually one and the same net—the name of which was decided in the dropdown list in Fig. 9-62. Once we get to Layout we will separate the ground systems using a split plane.

Using busses for digital nets

Digital circuits often have multiple, related input/output wires. The serial-to-parallel shift register in Fig. 9-60 is an example, in which Q0 through Q7 are data lines that represent the analog voltage sampled by the analog-to-digital converter as an 8-bit word. Rather than draw all eight lines throughout your schematic you can group the eight members of the word into a single bus (the blue line in Fig. 9-60).

A bus is a solid line that represents a group of wires or signals. Busses are not used to make connections to pins, but busses contain the signals that are connected to pins. Signal lines are added to a bus through aliases. Nets that are contained in busses are named, for example, A0, A1, A2, and A3 and the bus that contains them is named A[0..3].

Busses are placed on the schematic using the Place Bus tool, . After you have placed the bus you define (name) it with an alias using the Place Net Alias tool, N1. Busses are named by a specific convention, *busname*[n..m], in which *busname* is the alias (a name you give it) and [n..m] is a member list made up of integers. The integer n in *busname*[n..m] is the first member of the list and integer m is the last member of the bus list. The integers within the list can be separated with two periods, [n..m]; a colon, [n;m]; or a dash, [n-m]. The nets (wires) that make up the members are placed on the schematic using the Place Wire tool, . The bus members are placed on the schematic as you would place any other wire, but they are added to the bus by giving the wire a name (a member alias) that associates it with the bus. The members are named as *busname***n** through *busname***m** with the Place Net Alias tool. So in this example the bus alias is named Q[0..7], and the member aliases are named Q0, Q1, etc., to Q7.

The microcontroller (U3) has a couple of unused pins. To indicate that the pin is a "no-connect," place a no-connect symbol on the pins by selecting the Place No Connect button, , from the toolbar and place no-connect symbols on the unused pins.

Note

- *Any pin in a schematic used to make a PCB can have a no-connect symbol, but when PSpice simulations are performed some pins are not allowed to "float" and the no-connect symbol cannot be used. In that case use the RtoGND in the FLOAT property setting (see the Capture User Guide, cap_ug.pdf, and search for RtoGND).*

Once the design is completed, it is a good idea to do some housecleaning and design checking before making the netlist. Such tasks include:

1. Perform an annotation to clean up part numbering.
2. Make sure that global power/ground nets are properly named.
3. Make sure all parts have the correct footprints assigned to them (use BOM to assist).
4. Perform a DRC to verify that the circuit design has no issues.
5. Correct any errors and reperform the DRC as needed.

Once the design has been second-checked and is free of errors, create the Layout netlist as described above (from the Project Manager go to **Tools → Create Netlist** and select the **Layout** tab).

Defining the layer stack-up for split planes

As discussed in the first example, it is a good idea to have the board constraints defined prior to starting the board layout. Items to consider are defining board technology, board size constraints, noise and shielding requirements, part placement restrictions, the number of power and ground planes and number of signal layers, and trace width and spacing requirements.

The voltage and current constraints are similar to those of the analog design except that the analog parts should be segregated from the digital parts on the board. In the earlier analog design example we used four planes for V+, V−, and ground. A similar approach could be taken here, but in this example we will use one plane for V+, V−, and VCC, and we will use one plane for both the analog and the digital grounds as shown in Fig. 9-63 to demonstrate the process of working with split planes. The default PWR layer will be divided into three completely separate power planes using three different copper pour areas to supply analog V+ (P_{A+}), analog V− (P_{A+}), and digital VCC (P_D). The ground plane will be partially divided into two ground planes for analog ground (AGND) and digital ground (GND) but left connected by a small section of copper near the connector's ground pin. This arrangement will segregate the analog components from the digital components and therefore reduce switching noise in the analog circuitry. To accomplish this the board will require two plane layers and at least two routing layers.

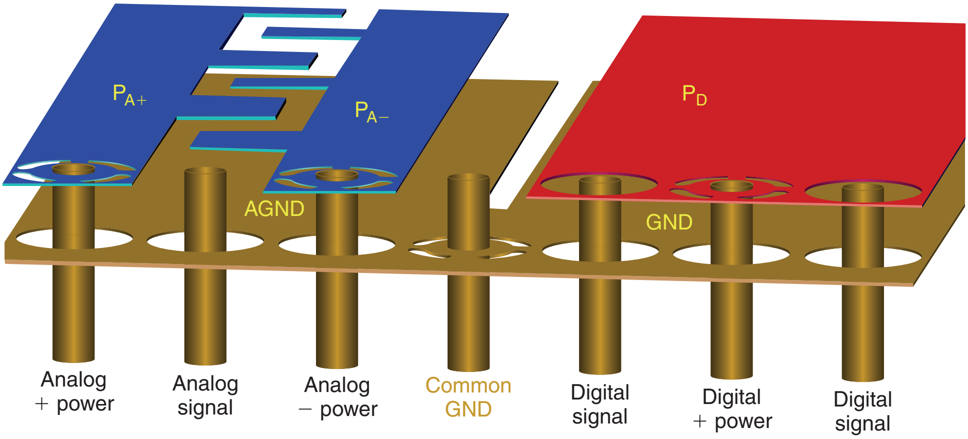


Figure 9-63 A mixed-signal power and ground system.

Table 9-7 lists the design constraints and the technology files that meet the constraints. The requirements are similar to the analog design, so we will again use **1bet_any.tch.**

Component and board requirements		Supporting technology files
Component mounting	Mixed (SMT and THT)	*bet_any.tch
No. sides w/parts	1	All
No. plane layers	2	All
No. routing layers	2	All
Total no. layers (minimum)	4	All
Smallest leads	SOIC-8	All
Pad spacing (minimum)	50 mils	All
Pad width (maximum)	25 mils	All
Max current	0.1 A	All
INNER trace width (min)	1.3 mils	All
OUTER trace width (min)	0.5 mils	All
Max voltage	10 V	All
Trace spacing (INNER)	4 mils	All
Trace spacing (OUTER)	5 mils	All

Table 9-7 Mixed-signal PCB design constraints and applicable technology files

To begin the board layout, we follow the same procedure as outlined at the beginning of the chapter and discussed in detail in the analog design example, but will not discuss them in detail here.

Start Layout and start a new board (File → New from the session window menu). From the AutoECO dialog box load the desired technology file (e.g., 1bet_any.tch as chosen above). Select the .MNL file generated by Capture and then save the .MAX file.

As described earlier, use the Obstacle tool to draw the board outline, use the search tools to find parts and groups from the pile and place them into the board outline, and perform a DRC to check for footprint problems prior to doing anything else. Figure 9-64 shows an example of how the parts might be placed. Notice that the analog parts are segregated from the digital parts.

Figure 9-65 shows the 1bet_any default layer stack-up. When the board constraints were defined above (Table 9-7), we said that we wanted two plane layers and two routing layers. The default has two plane layers (PWR and GND) and four routing layers (TOP, BOTTOM, INNER1, and INNER2). For the time being we will leave the inner routing layers enabled, and after we get through the first autorouting pass, we will see if we can squeeze everything onto the TOP and BOTTOM layer and eliminate the inner layers. So for the time being, we will use the default layer setup as is.

The next step is to assign the ground and power nets to their layers. Use the Nets spreadsheet (from the View Spreadsheet button). Beginning with the GND net (or AGND, whichever you named it—see Fig. 9-62), double click the cell to display the Edit Net dialog box, and then click the Net Layers... button to display the Layers Enabled for Routing dialog box shown in Fig. 9-66(a). Since there really is only one ground net it gets assigned to the GND plane. Below we will see how to split the plane into analog and digital areas.

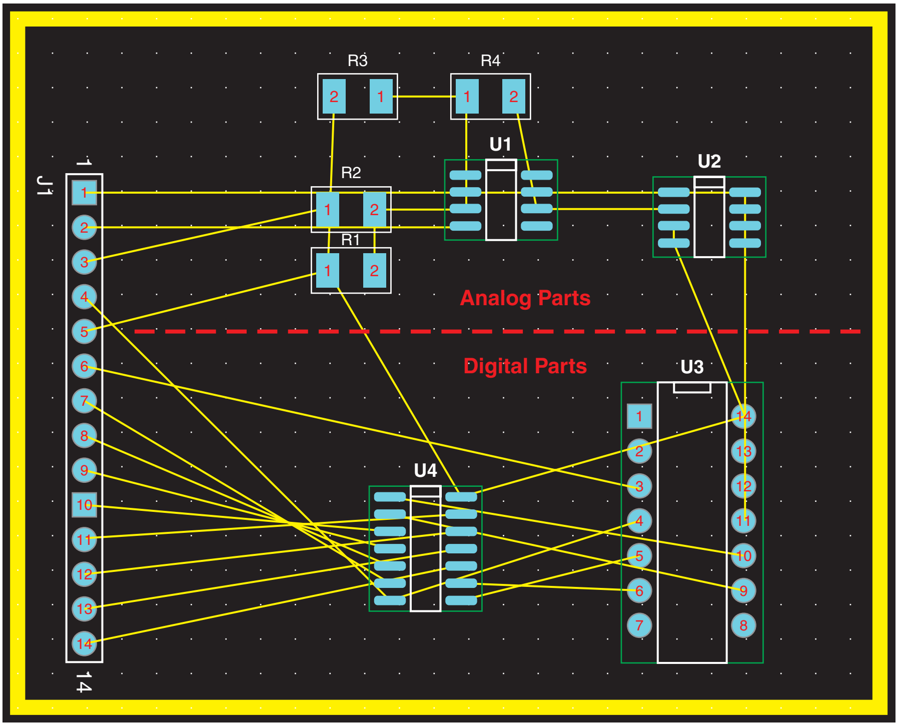


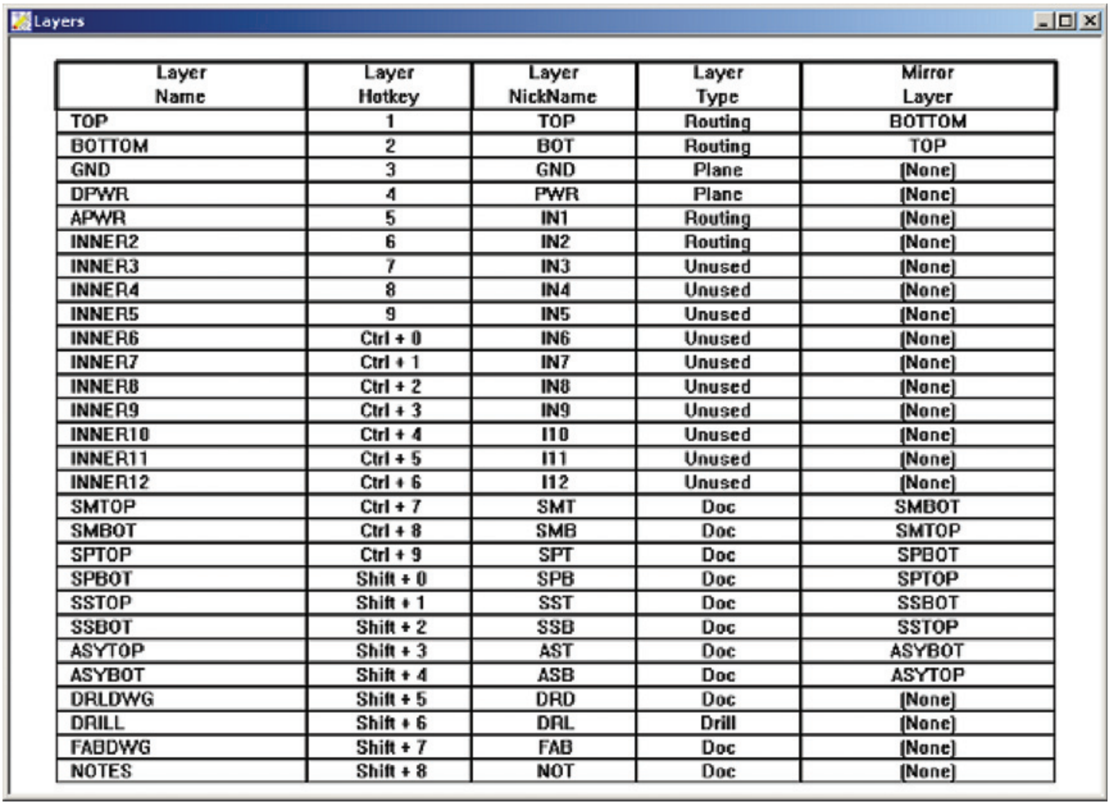
Figure 9-64 Initial parts placement.

Establishing a primary power plane

Unlike the ground system, in which there is really only one ground net and one ground plane, the power system has three distinct power nets (V+, V−, and VCC) that need to share the PWR plane. **For any plane layer, there can be only one net assigned to it; this net is called the primary net**. The other nets will be added to the plane later using nested copper pours within the plane, which is shown below. So for now we assign the VCC net to the PWR plane and leave the V+ and V− nets alone. Use the procedure described above and the Layers Enabled for Routing dialog box shown in Fig. 9-66(b) to assign VCC to the PWR plane.

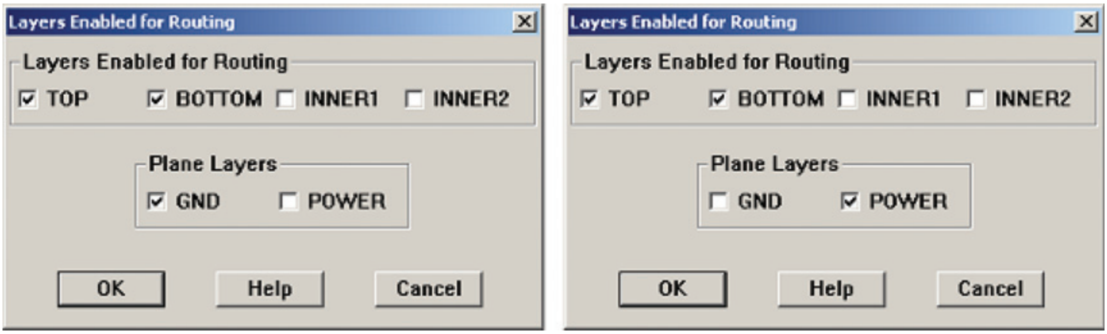
When we begin fanning out power and ground we will have four global nets to work with and it may be helpful to give each net its own color. **To change the color of a net**, open the Nets spreadsheet and select the net by left clicking its row once, right click, and select Change Color from the pop-up. Select a new color from the list (see Fig. 9-67 as an example). Note that the color of the net has nothing to do with which layer it will be routed on. After a net is routed (becomes a trace), the trace color will be determined by the layer on which it is routed and the thermals retain the net color.

Next we begin the process of fanning out power and ground. Disable all of the nets except for the power and ground nets. Select all of the nonpower and nonground nets by dragging a box



Layer Name	Layer Hotkey	Layer NickName	Layer Type	Mirror Layer
TOP	1	TOP	Routing	BOTTOM
BOTTOM	2	BOT	Routing	TOP
GND	3	GND	Plane	(None)
DPWR	4	PWR	Plane	(None)
APWR	5	IN1	Routing	(None)
INNER2	6	IN2	Routing	(None)
INNER3	7	IN3	Unused	(None)
INNER4	8	IN4	Unused	(None)
INNER5	9	IN5	Unused	(None)
INNER6	Ctrl + 0	IN6	Unused	(None)
INNER7	Ctrl + 1	IN7	Unused	(None)
INNER8	Ctrl + 2	IN8	Unused	(None)
INNER9	Ctrl + 3	IN9	Unused	(None)
INNER10	Ctrl + 4	I10	Unused	(None)
INNER11	Ctrl + 5	I11	Unused	(None)
INNER12	Ctrl + 6	I12	Unused	(None)
SMTOP	Ctrl + 7	SMT	Doc	SMBOT
SMBOT	Ctrl + 8	SMB	Doc	SMTOP
SPTOP	Ctrl + 9	SPT	Doc	SPBOT
SPBOT	Shift + 0	SPB	Doc	SPTOP
SSTOP	Shift + 1	SST	Doc	SSBOT
SSBOT	Shift + 2	SSB	Doc	SSTOP
ASYTOP	Shift + 3	AST	Doc	ASYBOT
ASYBOT	Shift + 4	ASB	Doc	ASYTOP
DRLDWG	Shift + 5	DRD	Doc	(None)
DRILL	Shift + 6	DRL	Drill	(None)
FABDWG	Shift + 7	FAB	Doc	(None)
NOTES	Shift + 8	NOT	Doc	(None)

Figure 9-65 Default layer stack-up for the mixed-signal board design.


(a)

Layers Enabled for Routing

☑ TOP ☑ BOTTOM ☐ INNER1 ☐ INNER2

Plane Layers

☑ GND ☐ POWER

(b)

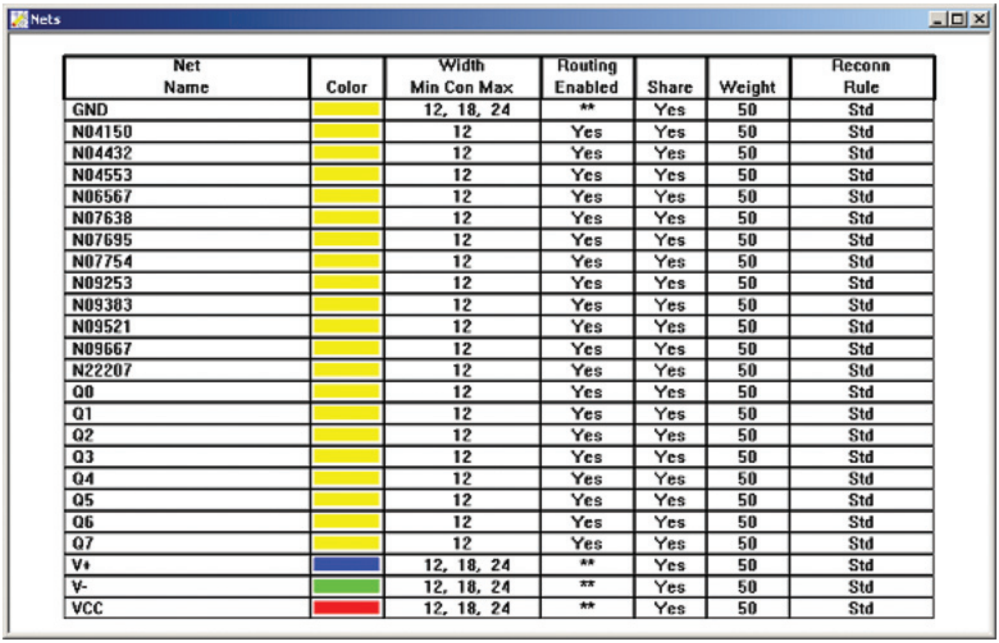
Layers Enabled for Routing

☑ TOP ☑ BOTTOM ☐ INNER1 ☐ INNER2

Plane Layers

☐ GND ☑ POWER

Figure 9-66 Assigning ground and power nets to planes. (a) Ground net assignment. (b) VCC net assignment (primary).



Net Name	Color	Width Min Con Max	Routing Enabled	Share	Weight	Reconn Rule
GND	🟨	12, 18, 24	**	Yes	50	Std
N04150	🟨	12	Yes	Yes	50	Std
N04432	🟨	12	Yes	Yes	50	Std
N04553	🟨	12	Yes	Yes	50	Std
N06567	🟨	12	Yes	Yes	50	Std
N07638	🟨	12	Yes	Yes	50	Std
N07695	🟨	12	Yes	Yes	50	Std
N07754	🟨	12	Yes	Yes	50	Std
N09253	🟨	12	Yes	Yes	50	Std
N09383	🟨	12	Yes	Yes	50	Std
N09521	🟨	12	Yes	Yes	50	Std
N09667	🟨	12	Yes	Yes	50	Std
N22207	🟨	12	Yes	Yes	50	Std
Q0	🟨	12	Yes	Yes	50	Std
Q1	🟨	12	Yes	Yes	50	Std
Q2	🟨	12	Yes	Yes	50	Std
Q3	🟨	12	Yes	Yes	50	Std
Q4	🟨	12	Yes	Yes	50	Std
Q5	🟨	12	Yes	Yes	50	Std
Q6	🟨	12	Yes	Yes	50	Std
Q7	🟨	12	Yes	Yes	50	Std
V+	🟦	12, 18, 24	**	Yes	50	Std
V-	🟩	12, 18, 24	**	Yes	50	Std
VCC	🟥	12, 18, 24	**	Yes	50	Std

Figure 9-67 Defining net colors and routing widths.

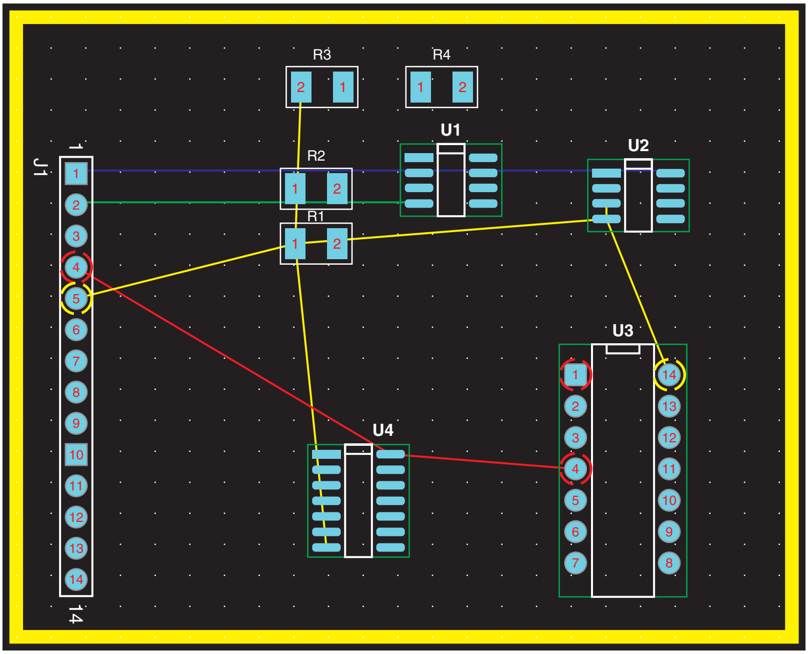
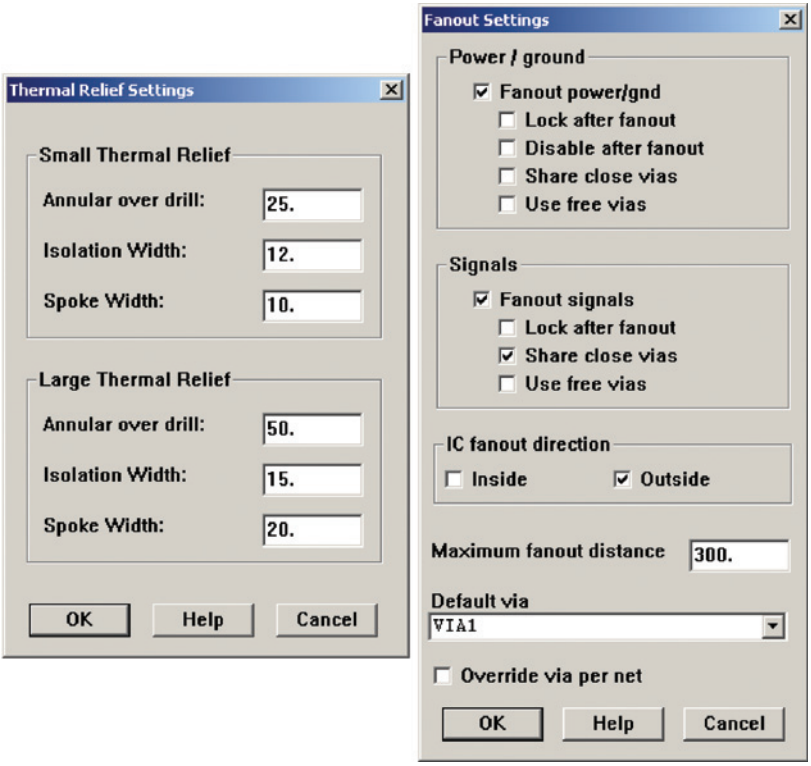

R3
2
1
R4
1
2
U1
U2
J1
1
R2
1
2
R1
1
2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
14
U3
1
2
3
4
5
6
7
14
13
12
11
10
9
8
U4

Figure 9-68 Global power and ground nets.

across the cells or using the Ctrl + left click to select more than one, right click, and toggle the Enable <-> Disable option. Close the spreadsheet, click the Refresh All button (!) and cycle through the layers to update the routing and refresh the view. Figure 9-68 shows the ground and power nets, in which GND is yellow, V+ is blue, V− is green, and VCC is red. Notice that some of the through-hole pins have thermals around them (indicating that they are already connected to their ground or power plane). None of the surface-mount pads have a path to a plane yet so they still have a rat's nest net attached to them. J1.1 and J1.2 (although through-hole) also still have rat's nest nets attached to them and no thermals because V+ and V− nets are not connected to planes at this point. Once we have the fanouts complete and the rest of the power planes set up, there will be no more rat's nest lines and all power and ground pins will be connected to a plane through thermal reliefs.

Begin the fan-out process by setting or checking the thermal relief and fanout settings. Use the Thermal Relief Settings and the Fanout Settings dialog boxes (shown in Fig. 9-69) from the Options menu. For this example we can use the default thermal relief settings. The only thing we might want to change in the fanout settings is to uncheck the Lock after fanout and Disable after fanout boxes. This allows you to move or unroute fanouts until you are satisfied with them. Once the fanouts are where you want them you can go to the fanout settings again and lock them and disable them to protect them from being disturbed.


Thermal Relief Settings

Small Thermal Relief
Annular over drill: 25.
Isolation Width: 12.
Spoke Width: 10.

Large Thermal Relief
Annular over drill: 50.
Isolation Width: 15.
Spoke Width: 20.

Fanout Settings

Power / ground
☑ Fanout power/gnd
☐ Lock after fanout
☐ Disable after fanout
☐ Share close vias
☐ Use free vias

Signals
☑ Fanout signals
☐ Lock after fanout
☑ Share close vias
☐ Use free vias

IC fanout direction
☐ Inside ☑ Outside

Maximum fanout distance 300.

Default via: VIA1

☐ Override via per net

Figure 9-69 Controlling thermal relief and fanout settings.

After making adjustments to the fanout setting you can fan out the board. Go to the Auto menu and select Fanout → Board. Once the fan-out process is complete, click the Refresh All button. The result is shown in Fig. 9-70. All ground and VCC nets are now connected to their planes. Although U1 and U2 V+ and V− pins have fanouts, V+ and V− are still rat's nest lines because they do not have a plane to go to. This will be addressed below. If you need to move a fan-out via unlock the net and use the Shove Track Mode interactive routing tool to reposition it.

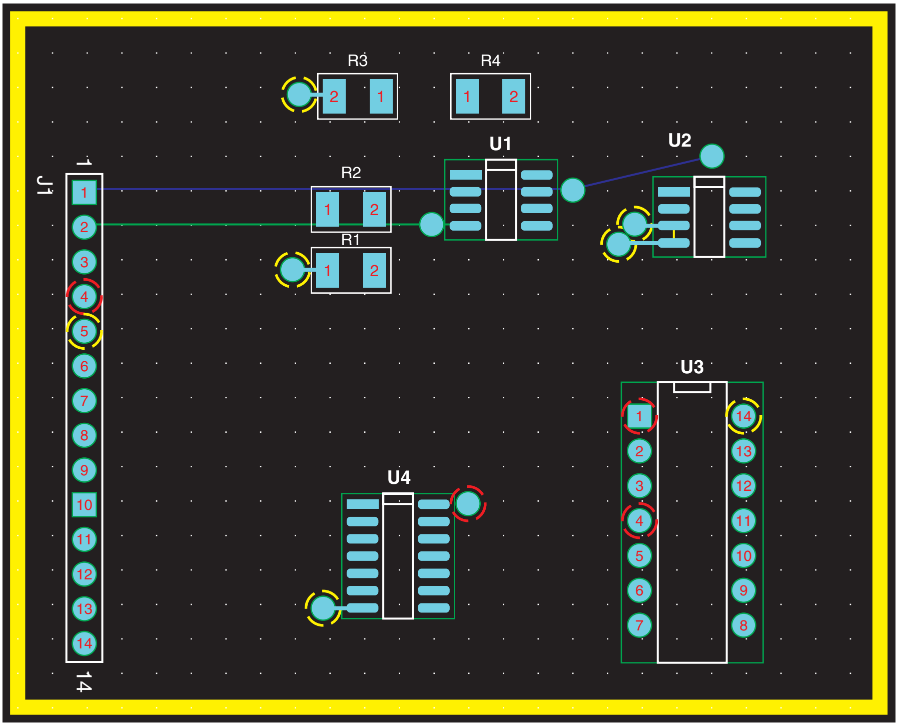


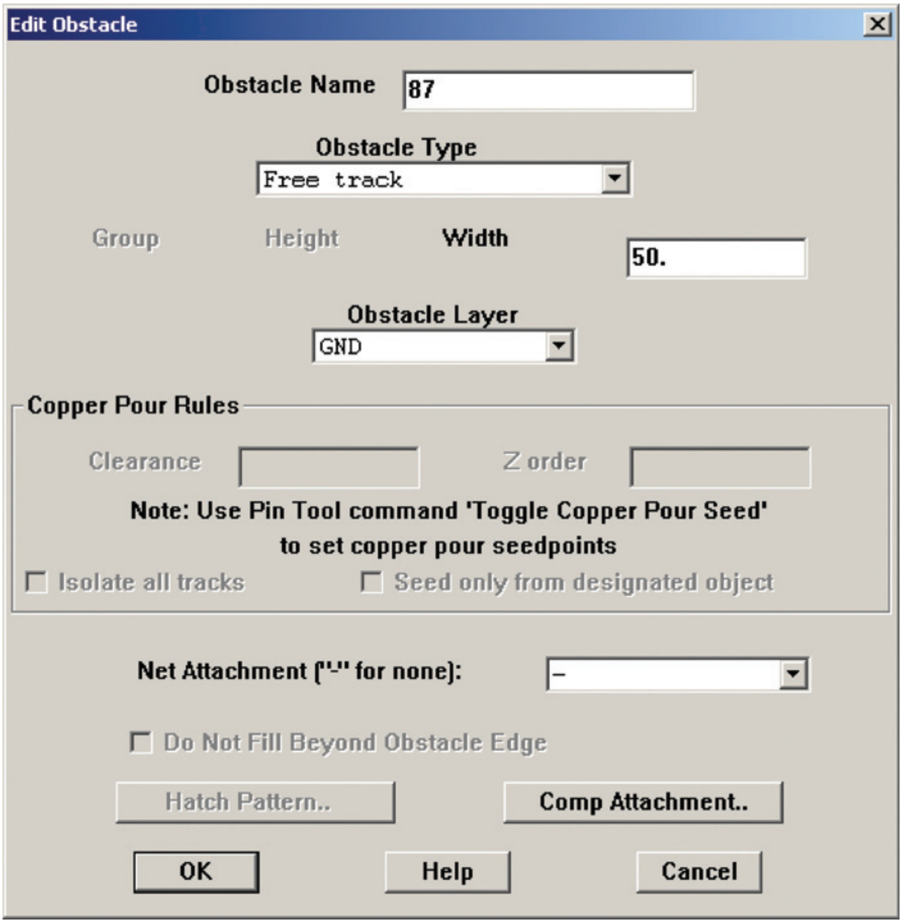
Figure 9-70 Mixed-signal board after fanout.

Creating split ground planes

Before we make power plane areas for V+ and V− we need to establish the ground plane areas so that we know where the positive and negative power planes boundaries will be (see Fig. 9-63). We will do this by splitting the ground plane into analog and digital sections.

To split a ground plane, select the Obstacle tool and right click to display the Edit Obstacle dialog box. As shown in Fig. 9-71, select Free Track from the Obstacle Type list, set the Width (spacing between ground planes) to 50 mils, and select GND from the Obstacle Layer list. Leave the Net Attachment as "-" and click OK.

The objective in splitting a plane layer into analog and digital sections is to remove copper from the plane using the free track (which is anti-copper on a negative layer). Figure 9-72



Edit Obstacle

Obstacle Name: 87

Obstacle Type: Free track

Width: 50.

Obstacle Layer: GND

Copper Pour Rules

Note: Use Pin Tool command 'Toggle Copper Pour Seed' to set copper pour seedpoints

☐ Isolate all tracks ☐ Seed only from designated object

Net Attachment ("-" for none): –

☐ Do Not Fill Beyond Obstacle Edge

Figure 9-71 Setting up a free track (anti-copper) to split the ground plane.

shows the desired split ground plane. Draw the 50-mil-wide free tracks to remove copper from the GND plane to separate AGND from GND. Left click once to start the track, move the mouse to the endpoint (or a vertex), and left click once again. To end the track, right click, and select End Command from the pop-up or hit the Esc key on your keyboard. Draw two separate tracks, leaving a space under the analog-to-digital converter (U2) shown as “Common GND Reference Under ADC” in Fig. 9-72. Notice that at the J1 connector we have the “Common Ground Area” in Fig. 9-72, but that the analog and digital ground areas are separated throughout the rest of the board. The area under the ADC does not defeat the “split” plane. Recall from Chap. 6 that return currents will follow the path of least impedance, so return currents related to U3 and U4 will not go out of their way to pass through the area under the ADC. Also note the V+ fan-out via on the right side of the board. At the moment it is located within the removed copper area. The fan-out via was placed there by the autorouter when we did the fanout. As far as board fabrication is concerned this is not a problem, but

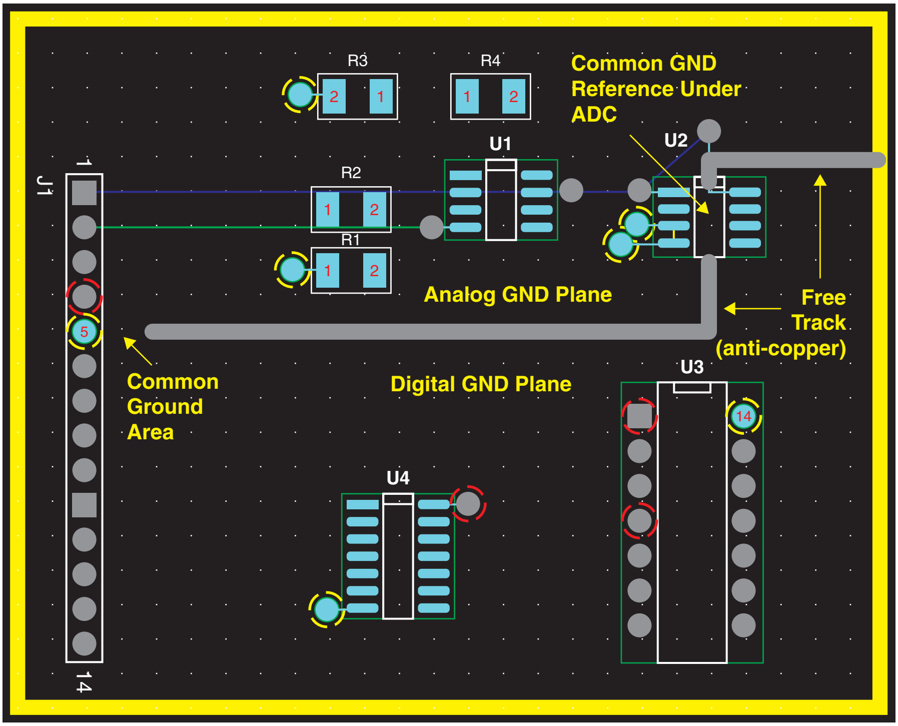


Figure 9-72 A split ground plane for AGND and GND.

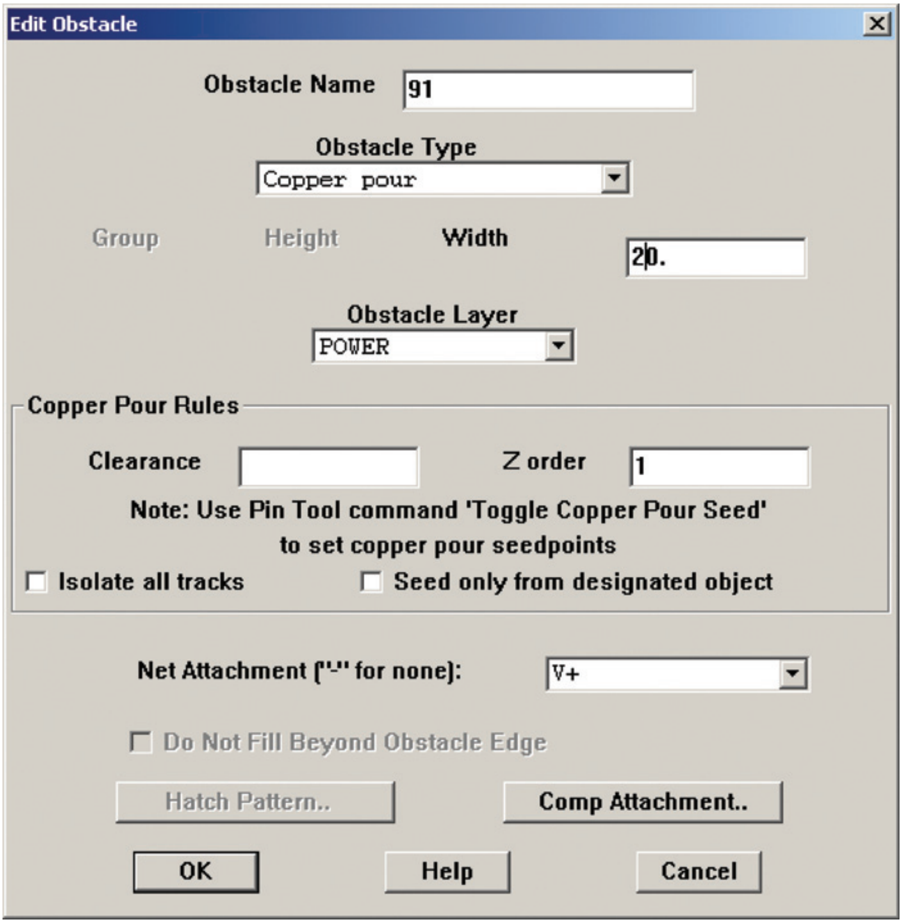
we will move the via in the next section when we place the V+ ground plane area to keep the analog and digital power panes definitively separated.

Creating nested power planes with copper pours

Next we will split the PWR plane into two more sections, V+ and V−, by using copper pours on the analog portion of the PWR plane. To create isolated areas on a plane and assign additional nets you must first assign a primary net to the initial plane layer. Then, as you pour the new copper areas (copper pour obstacles), you assign secondary nets to the copper pour obstacles. If the isolated area does not contain a pin or a net (a heat spreader, for example) then you have to assign a Z order to the copper pour to create a nested copper pour. Using the Z order you can place nested copper pours on top of nested copper pours. In this example the copper pours will be attached to pins on J1, so we do not have to assign Z orders to them (see p. 398 of the *Layout User's Guide*).

To place isolated plane areas on a plane layer begin by assigning a primary net to the plane layer. This was done earlier in this example when the Nets spreadsheet was used in conjunction with the Edit Net dialog box to assign net VCC to the POWER plane (see Fig. 9-66).

Next, **assign a secondary net** to the power plane. Select the Obstacle tool button, right click, and select New from the pop-up, right click again, and select Properties to display the Edit Obstacle dialog box shown in Fig. 9-73. From the Obstacle Type list select Copper pour. Enter 20 in the Width box to provide 20 mils of space between the copper pour and the copper plane that it will be poured into. From the Obstacle Layer list select the POWER layer. From the Net Attachment list select V+. You can leave the Z order as 0 in this case since we will pour the copper area to include the J1 pin connected to the V+ net. Click OK.


Edit Obstacle

Obstacle Name: 91

Obstacle Type: Copper pour

Width: 20.

Obstacle Layer: POWER

Copper Pour Rules

Clearance:

Z order: 1

Note: Use Pin Tool command 'Toggle Copper Pour Seed' to set copper pour seedpoints

☐ Isolate all tracks

☐ Seed only from designated object

Net Attachment ("-" for none): V+

☐ Do Not Fill Beyond Obstacle Edge

Figure 9-73 Using a copper pour as a secondary net on a plane layer.

Draw the V+ copper pour obstacle as shown in Fig. 9-74 making sure to include J1 pin 1 and the V+ fanouts for U1 pin 7 and U2 pin 8 within the obstacle and making sure the copper pour obstacle stays on the analog side of the split ground plane.

Note that in Fig. 9-74 the V+ fanout for U2 had to be moved up about 100 mils to get it out of the AGND/GND boundary (see Fig. 9-72 for comparison). **To move a fanout (or any free via)**, select one of the routing tools (Shove Track Mode works well for moving vias), select the via, move it to its new location, and left click once to place it. If the via's net is locked, click OK when Layout asks you if you want to **override the lock.**

Once you have the copper pour drawn, right click and select Finish or End Command from the pop-up. Click Refresh All button (!). Note that J1 pin 1 and the V+ fanouts now have thermals and the V+ rat's nest lines have disappeared. This indicates that the V+ net and its associated pins are connected to the copper pour.

Draw the V− copper pour using the procedure used for V+, except assign the obstacle to V− and making sure to include J1 pin 2 within the boundary and making sure to stay on the analog side of the ground plane as shown in Fig. 9-74. The edges (the outlines) of the V− pour and the V+ pour may overlap, but do not overlap the pours (the inside area of the copper pour obstacle). The outlines are actually 20-mil clearances so it is OK if they (the clearances) are on top of each other, but if the actual pours overlap by more than the clearance width then disconnected islands will result, causing DRC errors caused by incorrect copper pours. Note that U1 pin 4 (and its fanout) is the only connection to the V− pour so the pour could have been just large enough to include the fanout. The pour in Fig. 9-74 was made larger so that it is about the size of the V+ pour to provide for symmetry, which helps to minimize board warping. Click the Refresh All button again to make sure that the V− net and pins are connected to the pour as indicated by thermals.

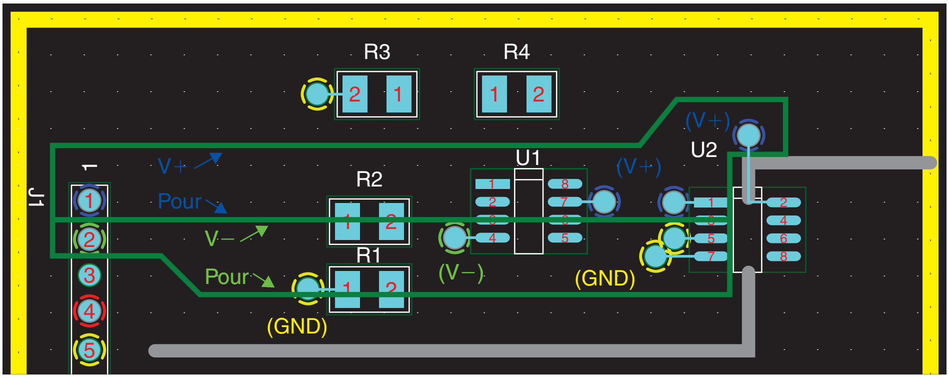
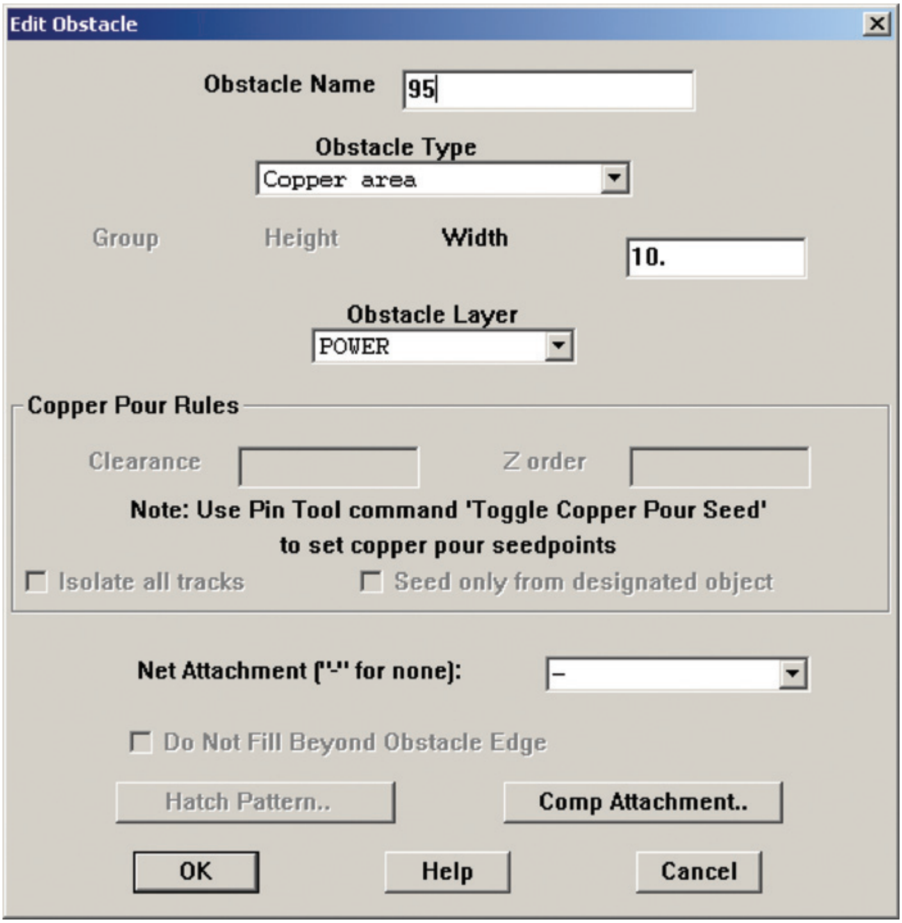


Figure 9-74 Copper pours added to the power plane.

Once you have completed adding the two copper pours to the POWER plane there are three power planes on the one plane. Although V+ and V− are isolated electrically from VCC, VCC surrounds V+ and V− and overlaps the analog ground plane. We need to get rid of VCC on the analog side of the board, and we will do so using copper area obstacles (a copper area on a negative layer is actually anti-copper).

Using anti-copper on plane layers

To remove copper areas from a plane layer, draw a copper area obstacle where the copper is to be removed. Select the Obstacle tool, right click and select New, right click again and select Properties. At the Edit Obstacle dialog box (shown in Fig. 9-75) select the Copper area Obstacle Type on the POWER layer. Use a width of 10 mils or smaller and select none, "-", for the net attachment. Click OK.


Edit Obstacle

Obstacle Name: 95

Obstacle Type: Copper area

Width: 10.

Obstacle Layer: POWER

Copper Pour Rules

Note: Use Pin Tool command 'Toggle Copper Pour Seed' to set copper pour seedpoints

Net Attachment ('-' for none): -

Group
Height
Clearance
Z order
☐ Isolate all tracks
☐ Seed only from designated object
☐ Do Not Fill Beyond Obstacle Edge
Hatch Pattern..
Comp Attachment..
OK
Help
Cancel

Figure 9-75 Use a copper area obstacle to remove copper from a plane layer.

It is easiest to define irregular areas by using multiple obstacles. VCC copper will be removed from around the analog power areas in two steps as shown in Fig. 9-76. Draw the first copper area as shown by the dashed red line in Fig. 9-76(a) and the second area as shown by the dashed red line in Fig. 9-76(b). This will remove VCC copper all the way up to the boundary of the digital ground plane. Click the Refresh All button when you have finished drawing the obstacles. This completes routing the power and ground planes. Lock and disable the VCC, V+, V−, and GND nets. **To disable and/or lock nets** open the Nets spreadsheet, and select the nets you want to disable and/or lock by holding down the Ctrl key and left clicking each net. Right click and select Enable <-> Disable and/or Lock from the pop-up.

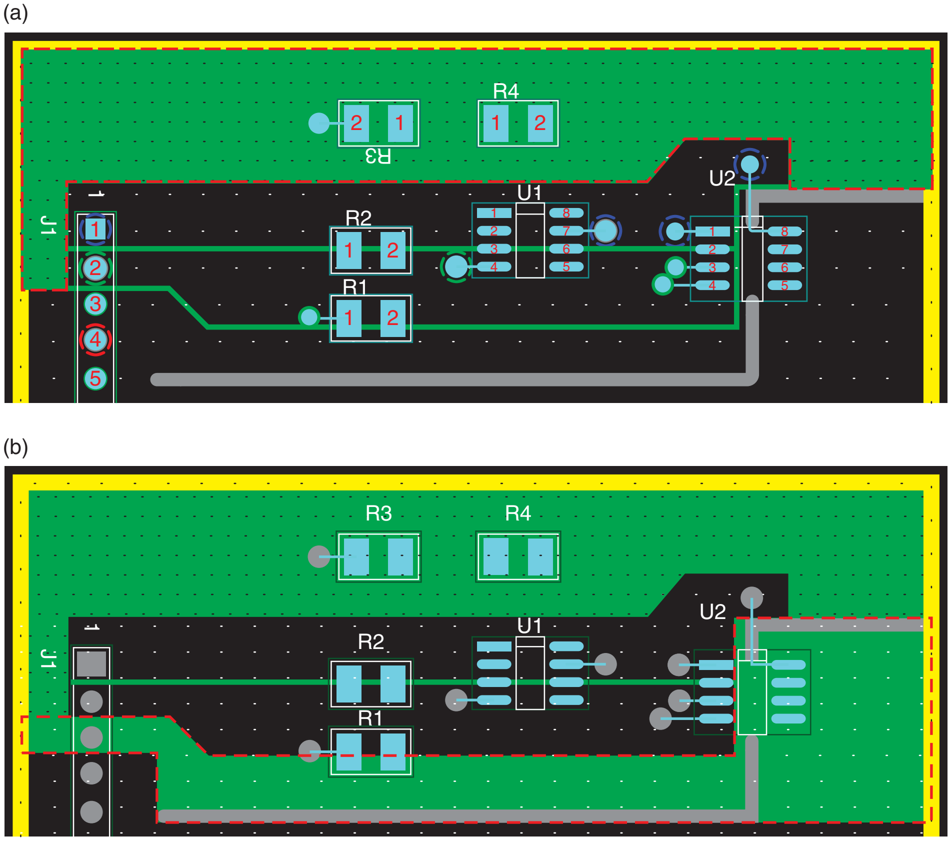


Figure 9-76 Copper areas removed from the power plane. (a) First copper area. (b) Second copper area.

Once all of the power and ground have been routed we can prepare to autoroute the board.

Enable all other nets that you want the autorouter to route. **To enable nets for routing**, or to find out which nets are enabled/disabled, open the **Nets** spreadsheet as described above, select and enable or disable nets as desired by toggling **Enable** <-> **Disable** from the pop-up.

Setting up and running the autorouter

With this example there are no special settings that need to be made to the autorouter. For highly dense boards or boards with special needs you can make adjustments to the autorouter by setting the size of the Route/DRC box, selecting specific route strategy files, modifying route strategy files, and automatically generating test points. To find out more about these options see the *Layout Autorouter User's Guide* located in the docs folder of the OrCAD directory. You can also use SPECCTRA to assist in the autorouting process. We will look at SPECCTRA in Chap. 11.

One thing we will take note of here is that we currently have four routing layers enabled (TOP, BOTTOM, INNER1, and INNER2). **To see which layers are enabled, or to enable/disable routing layers**, select the Layers spreadsheet from the View Spreadsheets button on the toolbar. Select layer(s) that you want to change, right click, and select Properties from the pop-up to display the Edit Layer dialog box. Select the desired option for the layer(s). For the time being we will leave the four routing layers enabled to make sure the board routes OK, and we can change this layer if we want to or are able to.

To run the autorouter, select Autoroute → Board from the Auto menu. An example of a routed board is shown in Fig. 9-77.

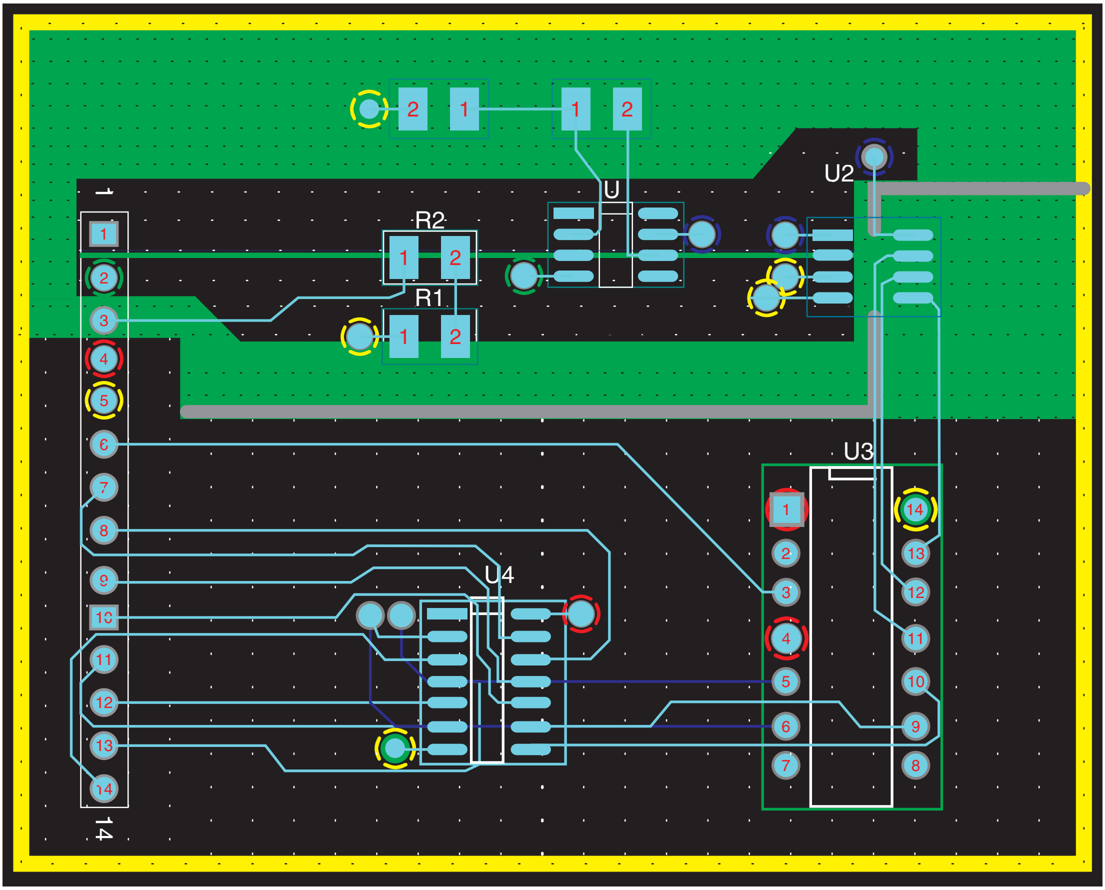


Figure 9-77 The routed board generated by the Layout autorouter.

As in the earlier example, a postrouting inspection is performed after autorouting to look for problem areas, and offending traces are unrouted and then rerouted. Figure 9-77 shows a couple of areas that could use some work. The first area is the clock and data traces that run between the microcontroller (U3) and the ADC (U2). The traces are running over an area from which the digital ground plane was removed (the gray area on the GND layer), and the traces run side by side in close proximity for a relatively long distance. The traces should be moved over the digital ground plane and moved farther apart (discussed next), or guard traces can be added to provide isolation between the traces (discussed below and in the next section).

To move routed traces use one of the manual routing tools (such Add/Edit Route Mode or Edit Segment Mode) or one of the interactive routing tools (such Autopath Route Mode or Shove Track Mode) to reposition or rip up and reroute the traces. For more detail on how to use the manual routing tools see the previous example and additional routing tips at the end of this chapter. See also Chap. 3 of this book or Chap. 10 of the *Layout User's Guide*.

Another thing that could be better is that the number of routing layers can be reduced. Initially four routing layers were enabled, and in this board the autorouter used only the TOP and INNER2 layers. We can move the few traces that are on the INNER2 layer to the BOTTOM layer and then disable the INNER layers altogether to reduce the total layer count to just four (two routing layers and two plane layers).

Moving a routed trace to a different layer

As long as a trace has a through-hole or fan-out via on each of its ends, you can easily change which layer the trace is on without having to rip it up. **To change the layer of a trace**, select one of the manual routing tools, hold down the Ctrl key on your keyboard, and select the trace that you want to move. Select the destination layer by pressing the appropriate number on your keyboard or selecting the layer from the layer selection list on the toolbar. So, for example, to change one of the traces on the INNER2 layer (the blue layer) in Fig. 9-77 to the BOTTOM layer, select the trace and press the "2" key on your keyboard. The trace is automatically moved to the BOTTOM layer but is otherwise unaffected. You can then move or otherwise edit the trace as desired using one of the manual routing tools. Figure 9-78 shows the board after moving traces from the INNER2 layer to the BOTTOM layer and cleaning up some of the other traces.

Adding ground planes and guard traces to routing layers

As discussed at the beginning of this chapter and in Chap. 6 it was said that you can reduce noise levels on signal lines by surrounding traces with copper planes and guard traces. Not everyone agrees with this practice but it is demonstrated here in the interest of completeness. The following procedures demonstrate how to use copper pours, add free vias, use the Connection tool to add ground nets, and use obstacles to add copper planes and guard traces to routing layers.

We begin by adding ground planes to the TOP and BOTTOM routing layers. **To add ground plane areas to a routing layer**, make the TOP layer active and select the Obstacle tool. Right click and select New from the pop-up. The Edit Obstacle dialog box will be displayed (see Fig. 9-79). Choose the Copper pour Obstacle Type, choose the TOP Obstacle Layer, and attach the obstacle to the GND net. Click OK.

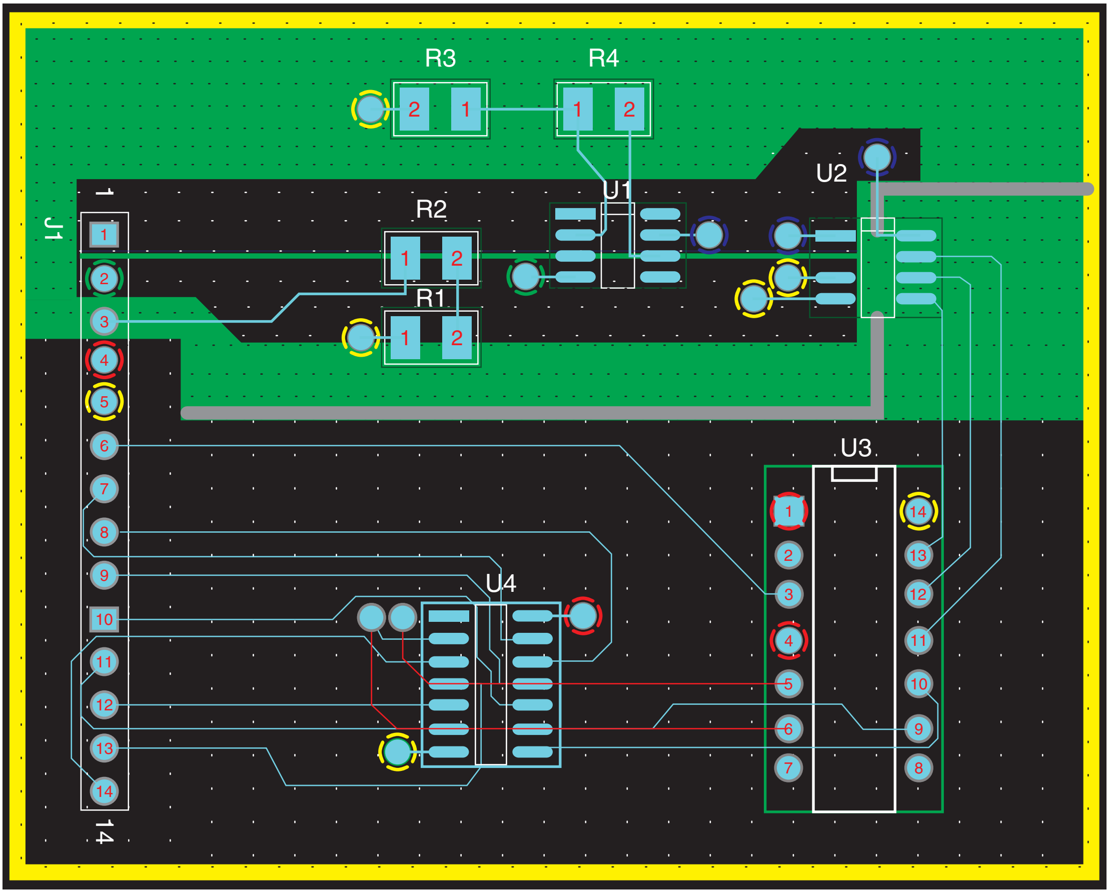


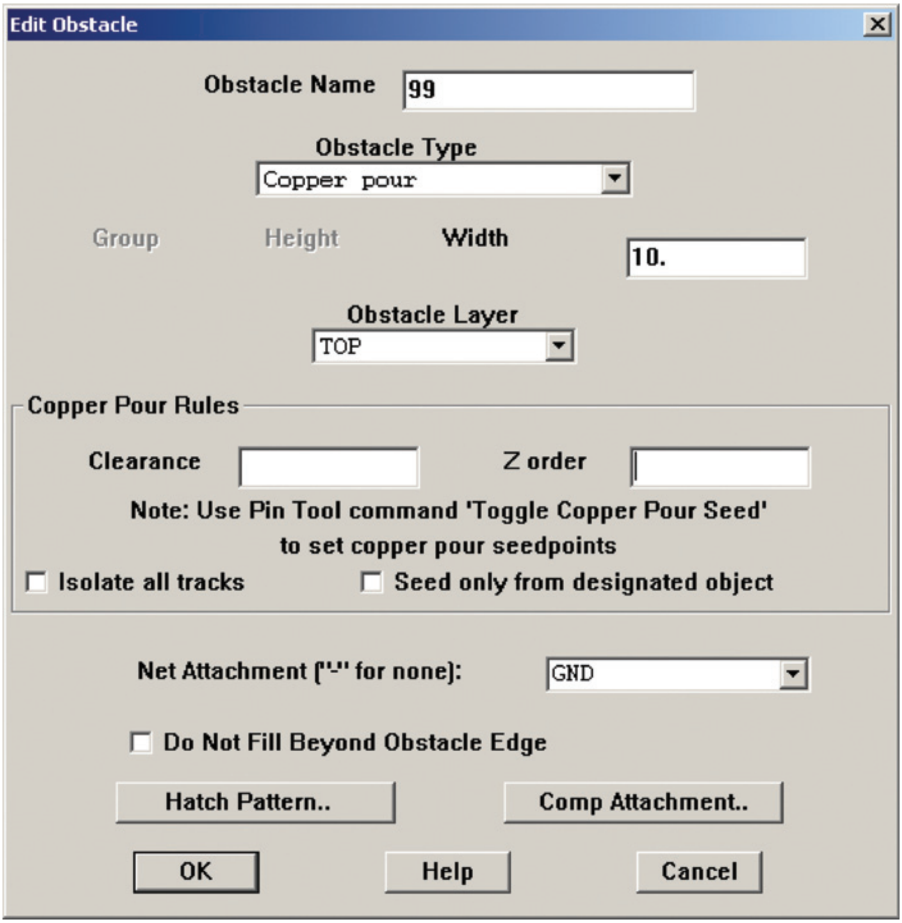
Figure 9-78 The mixed-signal board after routing and cleanup.

Place the copper pour on the TOP layer in two sections as shown in Figs. 9-80(a) and 9-80(b), as was done with the copper pours on the plane layers above. The copper pour obstacle will automatically fill in empty areas, avoid routed traces, and create thermals to vias and through-holes. Remember to provide spacing between the analog and the digital ground areas.

When you are finished adding the ground plane to the TOP layer click the **Refresh All** button to make sure that everything that should be connected to the ground plane is and that anything that should not be is not. Perform a DRC to make sure the copper pour did not cause any errors.

You can add a ground plane to the BOTTOM layer (or any other routing layer for that matter) using the same procedures used for the TOP layer.

Although we have split the ground plane (on the TOP and the GND plane) and limited the common reference point to the area close to the connector, some chips (particularly analog-to-digital converters) require the analog and digital ground planes be connected near



Edit Obstacle

Obstacle Name: 99

Obstacle Type: Copper pour

Width: 10.

Obstacle Layer: TOP

Copper Pour Rules

Clearance:

Z order:

Note: Use Pin Tool command 'Toggle Copper Pour Seed' to set copper pour seedpoints

☐ Isolate all tracks ☐ Seed only from designated object

Net Attachment ("-" for none): GND

☐ Do Not Fill Beyond Obstacle Edge

Figure 9-79 Using a copper pour to place a ground plane on a routing layer.

the chip—typically underneath. The analog and digital ground planes are connected under U2 on the GND plane because the free track (removed copper) has a gap in it directly under U2 (i.e., the copper is intact on the GND plane), but the ground plane on the top layer is completely split under U2. The area under U2 could have been accounted for when the second copper pour was added, but a copper area will be placed under U2 to demonstrate how to do it.

To use a copper area as part of a ground plane select the Obstacle tool, make the TOP layer active, and select the Obstacle tool. Right click and select New from the pop-up. The Edit Obstacle dialog box will be displayed (see Fig. 9-79). Choose the Copper area Obstacle Type, choose the TOP Obstacle Layer, and attach the obstacle to the GND net. Click OK. Place a small square of copper under the ADC (U2). Make it just big enough to fill the gap but no bigger because copper areas are not smart enough to reshape themselves like copper pours do. To connect copper areas to the ground plane, use a free via as shown in Fig. 9-81 and described below.

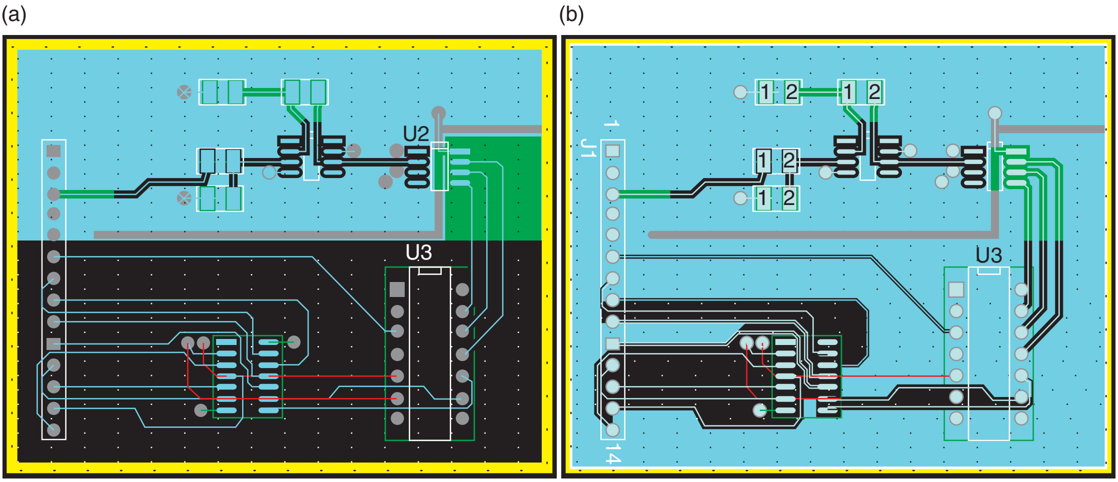


Figure 9-80 A multisection ground plane on the TOP routing layer. (a) Poured copper analog ground. (b) Poured copper split ground.

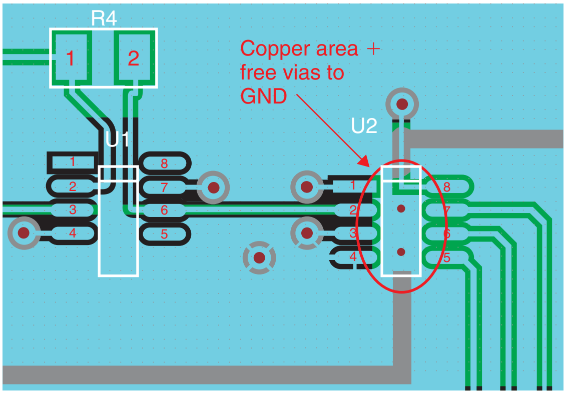
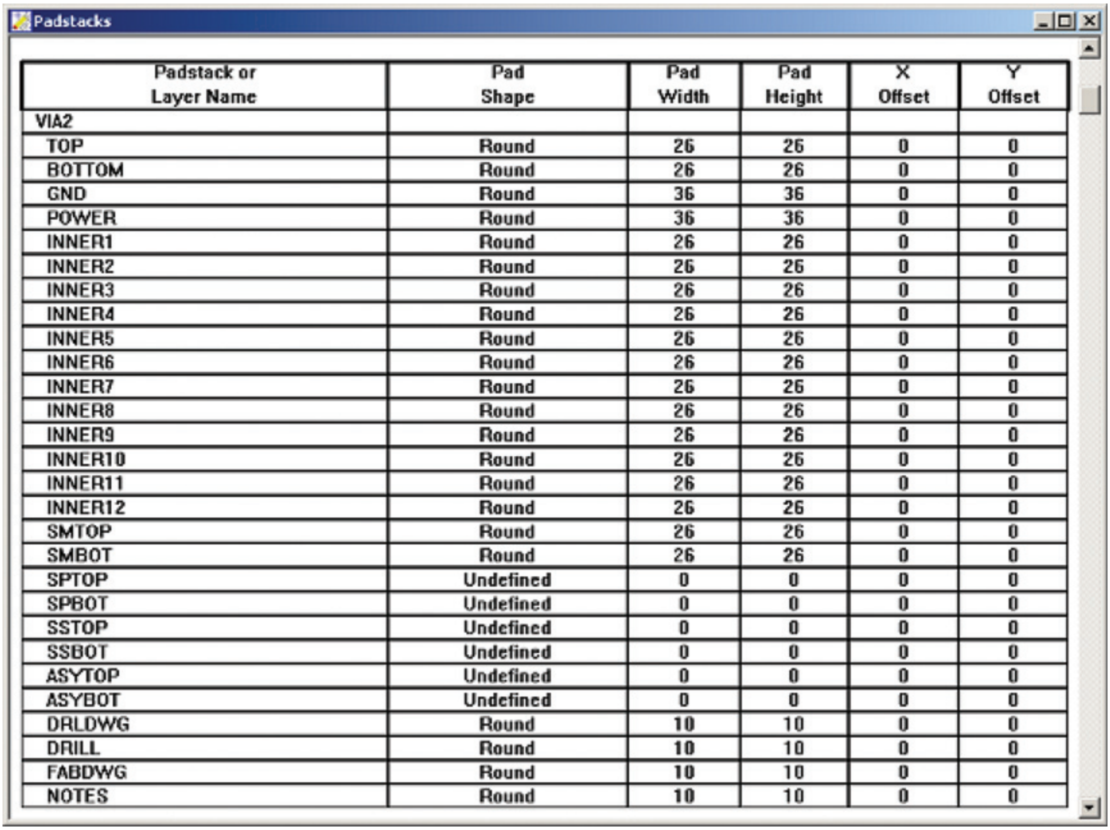


Figure 9-81 Using a copper area and free vias to add ground areas.

You can use default vias as free vias but they are typically large for how we want to use them here. So we need to make a small via specially for this application. The new via dimensions are 10-mil drill hole, 25-mil pad diameter, no thermals (not being soldered), and no soldermask (tented).

Defining vias for flood planes/pours

To define a new via, open the Padstacks spreadsheet and select the first unused via (Via2 in this case). Set the layers up as shown in Fig. 9-82. Also select the entire padstack (click on the VIA2 cell), right–click, and select Properties; check the Copper Planes/Pours box so that thermals are not used on the ground planes.



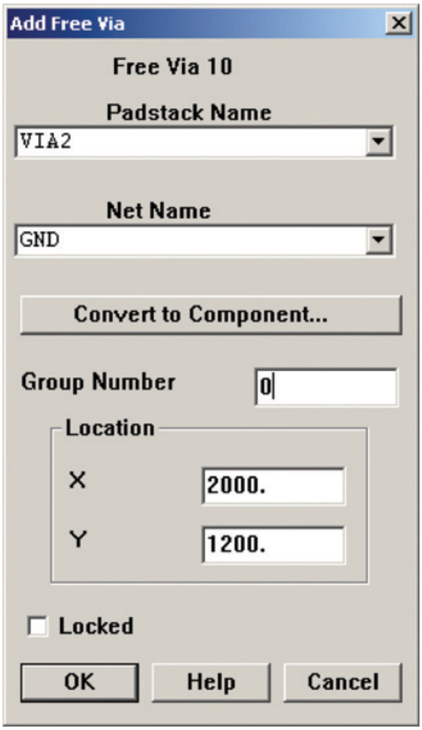
Padstack or Layer Name	Pad Shape	Pad Width	Pad Height	X Offset	Y Offset
VIA2					
TOP	Round	26	26	0	0
BOTTOM	Round	26	26	0	0
GND	Round	36	36	0	0
POWER	Round	36	36	0	0
INNER1	Round	26	26	0	0
INNER2	Round	26	26	0	0
INNER3	Round	26	26	0	0
INNER4	Round	26	26	0	0
INNER5	Round	26	26	0	0
INNER6	Round	26	26	0	0
INNER7	Round	26	26	0	0
INNER8	Round	26	26	0	0
INNER9	Round	26	26	0	0
INNER10	Round	26	26	0	0
INNER11	Round	26	26	0	0
INNER12	Round	26	26	0	0
SMTOP	Round	26	26	0	0
SMBOT	Round	26	26	0	0
SPTOP	Undefined	0	0	0	0
SPBOT	Undefined	0	0	0	0
SSTOP	Undefined	0	0	0	0
SSBOT	Undefined	0	0	0	0
ASYTOP	Undefined	0	0	0	0
ASYBOT	Undefined	0	0	0	0
DRLDWG	Round	10	10	0	0
DRILL	Round	10	10	0	0
FABDWG	Round	10	10	0	0
NOTES	Round	10	10	0	0

Figure 9-82 Setup for small free via.

Once the new via has been defined, it can be placed on the board as a free via. **To insert a free via** that is to be connected to a ground net, select Tool → Via → New from the menu bar, select Via2 from the Add Free Vias dialog box, and select the GND net as shown in Fig. 9-83. If you know the desired location enter it into the location boxes, otherwise clear the boxes so that the via can be placed with the mouse pointer. Click OK. Place a couple of vias underneath the ADC (U2) as shown in Fig. 9-81.

If you look closely at the ground strips between the traces going from pins 11 through 14 of U3 (the microcontroller) to pins 5 through 7 on U2 (the ADC) you will notice that the ground plane (the thin copper strips) is not connected to a solid ground (similar to a diving board that is attached to the ground plane at only one end). This causes the ground strips to act like antennas, which can pick up high-frequency noise (EMI) and cause problems for the rest of the circuit. To solve this problem the strips need to be either removed or tacked down to the ground plane at the unsupported end (near the ADC).

The strips can be removed in two ways. The first is to change the copper pour clearance setting so that Layout does not have enough room to pour the strips between the traces and



Add Free Via

Free Via 10

Padstack Name: VIA2

Net Name: GND

Group Number: 0

Location

X: 2000.

Y: 1200.

☐ Locked

Figure 9-83 Use the Add Free Via tool to connect copper pours to the ground plane.

obey spacing rules at the same time. The second method is to place anti-copper obstacles where you want to keep the copper from being poured.

Setting the copper pour spacing

To change a copper pour spacing clearance select the Obstacle tool from the toolbar and Ctrl + left click to select the copper pour, then right click, and change the clearance setting in the Edit Obstacle dialog box. You can also change all copper pour clearances by changing the global track-to-track spacing rules in the Route Spacing spreadsheet (go to Options → Global Spacing... on the menu bar), but using this method will change all route spacing, which may not be desirable.

After you make changes to the copper pour clearance or change the global spacing rules, click the Refresh All button to display the changes. Figure 9-84 shows the copper pour after changing the obstacle clearances. The affects of doing this are indicated by solid blue circles where the autorouter did not pour copper in areas that would result in unconnected islands of copper. You can further restrict the copper pour by changing the track-to-pad spacing on the Route Spacing spreadsheet. The effects of doing this are indicated by dashed red circles in Fig. 9-84. In order for the autorouter to obey the spacing rules it will not pour copper between package and header pins. This can create open slots in the ground planes, which can significantly increase the loop inductance of traces on other layers that are routed across the slots.

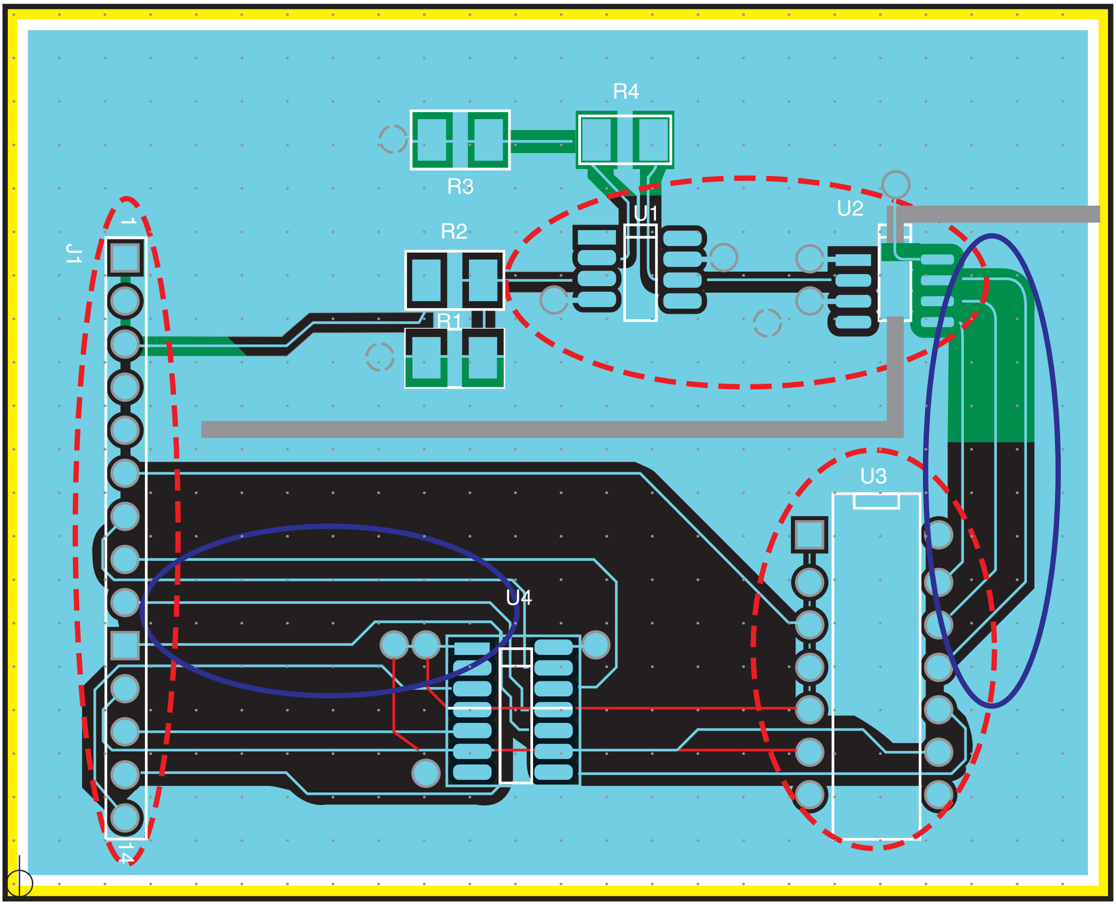


Figure 9-84 Copper pour after changing clearances.

Stitching a ground plane manually

Since the purpose of pouring the copper was to have a copper plane around traces in the first place, increasing the clearance spacing is not always the best solution. A better way to prevent ground plane antennas from copper pours is to tack the unsupported end to the dedicated ground plane using free vias. This is often referred to as "stitching" a ground plane. For this application use the small via defined above.

To "stitch" a ground plane, place vias along copper pours to attach them securely to the underlying ground plane (GND) as shown in Fig. 9-85. You can place the vias manually by

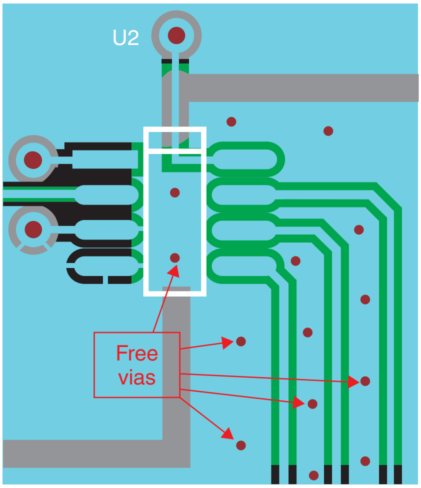


Figure 9-85 Using free vias to "stitch" copper pours to the ground plane.

choosing Tool → Via → New from the menu as described above (see Fig. 9-83), or you can use the free via matrix to place the vias (see the digital design example below).

Using anti-copper obstacles on copper pours

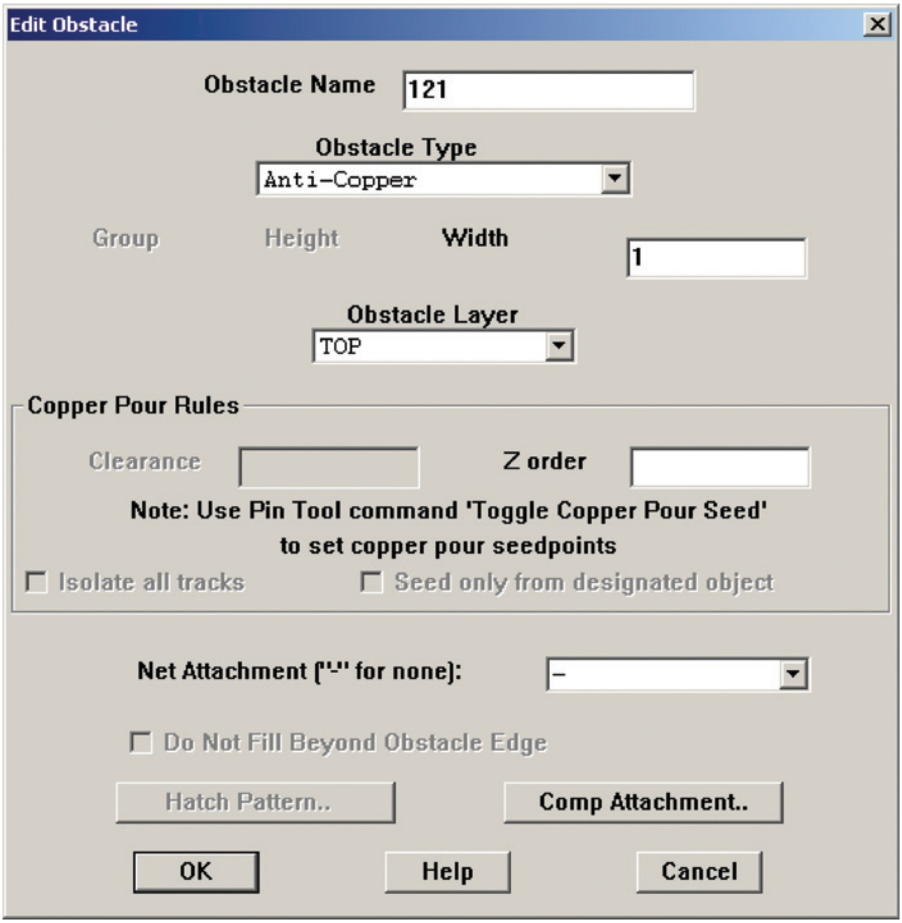
To further reduce the antennas created by the copper pours you can trim unwanted copper by using anti-copper areas with (or instead of) the vias. **To place an anti-copper area** select the Obstacle tool, right click, and select New from the pop-up. In the Edit Obstacle dialog box (see Fig. 9-86) select Anti-Copper as the Obstacle Type and select the appropriate Obstacle Layer. Leave the Z order blank and do not attach the obstacle to any net. Click OK.

Use the left mouse button (click and release) to place vertices that define the area where the copper should be removed as shown in Fig. 9-87. The obstacle will be indicated by an outline of the same color as the active layer, but the outline will not be present when the board is fabricated.

Routing guard traces and rings

Rather than shaping copper pours to add ground strips between traces, you can add guard traces and guard rings that can be attached to the ground plane with vias. It should be noted though that their usefullness is debated in the literature because they can cause more problems than they fix if not applied correctly (see the Subject Index, Appendix F for references). Figure 9-88 shows examples of guard traces between the control and the data lines and guard rings around one of the microcontroller pins (the TOP ground plane is partially removed for clarity).

To place guard traces that are attached to the ground plane, place free vias that are attached to the ground plane (net) at locations that define the ends of the guard traces. Use the


Edit Obstacle
Group
Height
Copper Pour Rules
Clearance
Z order
☐ Isolate all tracks
☐ Seed only from designated object
☐ Do Not Fill Beyond Obstacle Edge
Hatch Pattern..
Comp Attachment..
OK
Help
Cancel

Obstacle Name: 121

Obstacle Type: Anti-Copper

Width: 1

Obstacle Layer: TOP

Note: Use Pin Tool command 'Toggle Copper Pour Seed' to set copper pour seedpoints

Net Attachment ('-' for none): -

Figure 9-86 Edit Obstacle dialog box for defining an anti-copper area.

Connection tool, to add new rat's nest lines between via pairs. Use the Add/Edit Route Mode manual routing tool, to route the new net. Lock the traces when they are completed.

To place guard rings that are attached to the ground plane, select the Obstacle tool, right click and select New, right click again and select Arc, right click one more time and select Properties from the pop-up. In the Edit Obstacle dialog box select the Free Track Obstacle Type, enter the desired width of the guard ring (annular ring width), select the layer on which to place the guard ring, and select GND from the Net Attachment list. Click OK. Left click and release at the center of the pad to be guarded to define the center of the ring. Move the mouse outward to draw the ring. When the ring is the correct size, left click the mouse to complete the guard ring (see Fig. 9-88). At this point the guard ring is "attached" to the ground net (i.e., belongs to it), but the ring is not physically connected to it. To attach the guard ring physically to the ground plane add a free via (which is connected to the ground

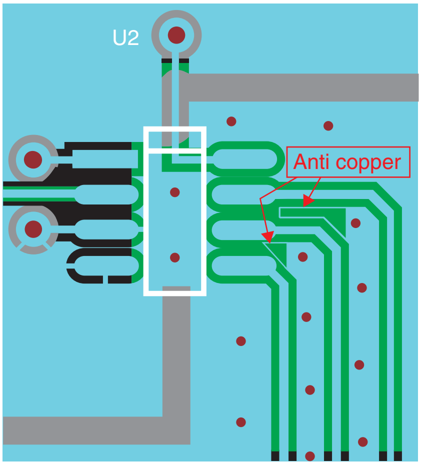

U2
Anti copper

Figure 9-87 Using anti-copper obstacles to trim copper pours.

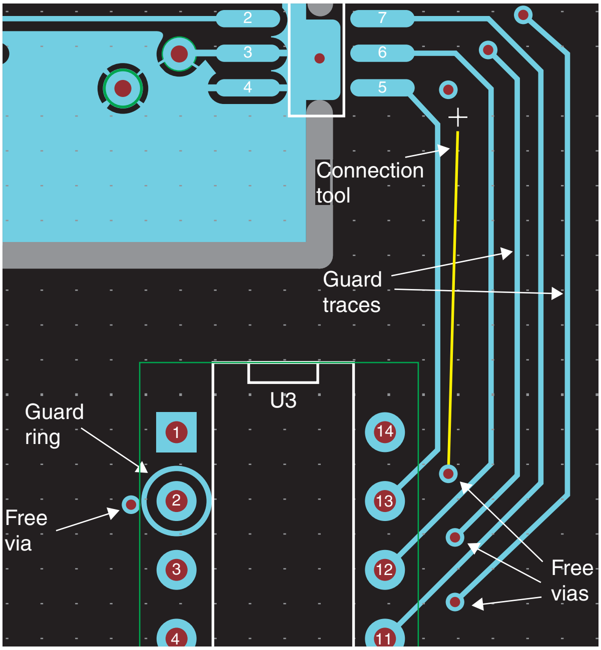

2
3
4
7
6
5
Connection tool
Guard traces
U3
Guard ring
Free via
1
2
3
4
14
13
12
11
Free vias

Figure 9-88 Examples of guard traces and guard rings.

net) next to the guard ring. Place the via close enough to the ring so that the annular ring on the via is touching (or on) the guard ring so that the guard ring is electrically connected to the via and in turn the ground plane (see p. 410 of the *Layout User's Guide*—Creating Duplicate Connections). That completes design example 2.

Example 3: Multipage, Multipower, and Multiground Mixed A/D PCB Design with PSpice

Multipage schematics can be used to organize and simplify large circuit designs and to incorporate PSpice simulations into a PCB Layout design. The mixed analog/digital circuit from the last example (see the schematic in Fig. 9-59) is reused in this example but is modified to demonstrate how to route a single PCB from a multipage schematic project and add PSpice simulation capabilities. The example also demonstrates two methods used to establish isolated ground planes using blind vias and a buried chassis shield. The technique allows quiet circuits to be placed on one side of the board and shielded from noisy digital circuits, which are placed on the other side of the board.

In the previous example a single plane layer was used to produce a digital ground and an analog ground even though there was really only one ground net. The two ground systems were produced by physically segregating the parts on the board and removing a strip of copper from the one plane (creating a split plane) between the two circuit areas.

In high-density, high-frequency digital designs multiple ground planes are often used even when there is only one type of circuit ground (as demonstrated in the Example 4 below). This helps reduce loop inductance when using multiple routing layers and control trace impedance (see Chap. 6 for details). When two plane layers are used for a single net, connections are made to both planes simultaneously through plated through-holes (whether for through-hole leads or fanouts from surface-mounted devices) any time a connection is made to the net. This is shown in Fig. 9-89.

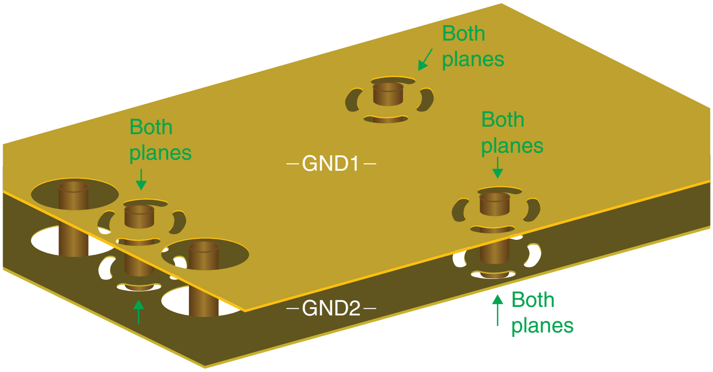


Figure 9-89 Multiple ground planes for one ground net, multiple connections.

In this example continuous plane layers are desired for both the analog and the digital parts of the circuit. As described in Chap. 6 significant cross talk can occur between adjacent planes if there is any overlap between the two plane areas. Since both the analog and the digital planes extend out to the limits of the board, there is complete overlap. The only way to keep the two planes separate is to insert a shield between them.

Figure 9-90 shows the system design concept for this example. This is just one of many possible types of power PCB power distribution schemes. The system uses a dual power supply for ±analog power for op-amps and a single power supply (VCC) for digital circuits. The analog and digital systems each have their own ground system on the PCB; however, a common reference voltage is required for the analog-to-digital converter. To facilitate both requirements the grounds are tied together at a single point on the PCB before returning to the power supply. To keep the two ground systems from experiencing cross talk on the PCB they are separated by a shield layer buried inside the PCB that is connected to the chassis ground and the shielded wire bundle. Extensive coverage of noise reduction and shielding is provided in the literature (see Ott for detailed coverage of this topic).

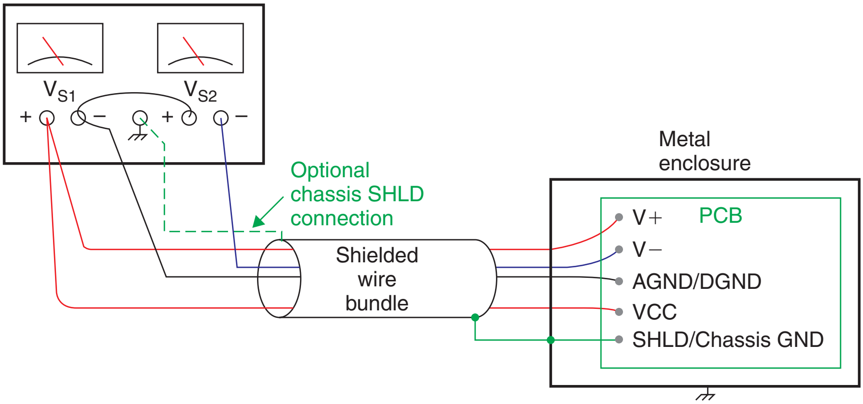


Figure 9-90 A multipower/multiground system with a chassis shield.

There are several ways to connect the two grounds at a controlled point (or points). The simplest would be to use a jumper wire at the connector. However, the analog-to-digital converter in this example also requires a common ground area under the IC package. A jumper wire is not practical in this case.

The challenge in setting up a ground system like this is that the two ground systems must be kept separate everywhere except at the tie point. This is not possible in Capture (at least not in a straightforward manner). As soon as the two ground nets are connected on the schematic (even if only at one point) the two nets become one everywhere in the netlist and cannot be separated in Layout since it is a single net. Therefore the two distinct ground nets (or three counting the shield) are kept separate in Capture and only made to appear to be connected (for documentation purposes). The individual nets are then tied together at the common reference point in Layout.

There are two methods that can be used in Layout to tie the distinct grounds together at the common reference point. The first method uses a plane-to-plane connector (a shorting strip) as shown in Fig. 9-91. The shorting strip is a footprint that has two padstacks that are shorted

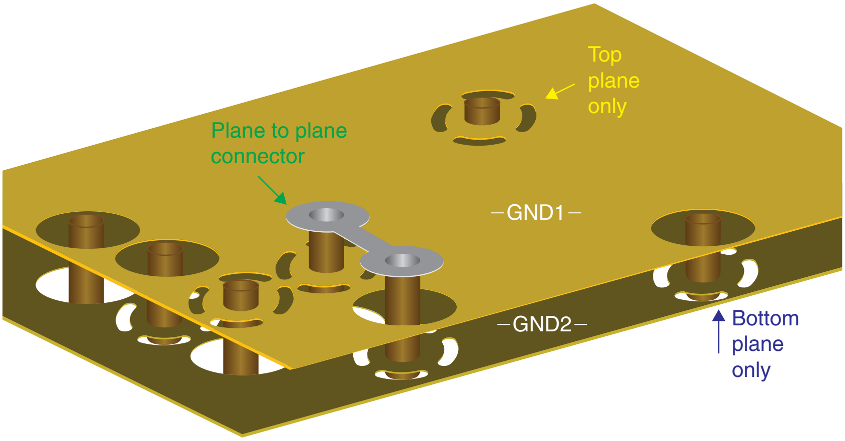


Figure 9-91 A shorting strip used as a plane-to-plane connector.

together with a copper strip (a free track). To use the shorting strip a Capture part must be made that has two pins but no electrical connection between them. The Layout footprint (with shorted pins) is assigned to the Capture part (with insulated pins). This method is demonstrated in the example below.

Note

- *The shorting strip can be replaced with a jumper wire or ferrite bead soldered into the footprint padstacks. The copper strip method is demonstrated in the example since it is mentioned in the Layout User's Guide.*

The second method uses a specialized padstack that forces the planes to be connected together through thermal reliefs as shown in Fig. 9-92. Normally clearances are specified on plane layers, and if the netlist specifies a connection to the plane layer Layout knows to insert a thermal relief in place of the clearance. However, if you explicitly specify thermals on plane layers the padstack will always be connected to the plane even if the netlist does not indicate a connection to it. If you force a connection to a plane layer with a thermal, Layout will not generate a DRC error because it assumes you intended to make the connection. This method will also be demonstrated in the example below.

The stack-up in this example demonstrates how to use Layout to implement one method of EMI and cross talk reduction. A 10-layer board and blind vias are required. The layer stack-up is shown in Fig. 9-93.

Project setup for PSpice simulation and Layout

Setting up a Capture project for Layout and PSpice at the same time has not been widely covered in the literature, so this example addresses that point. Extensive coverage of PSpice

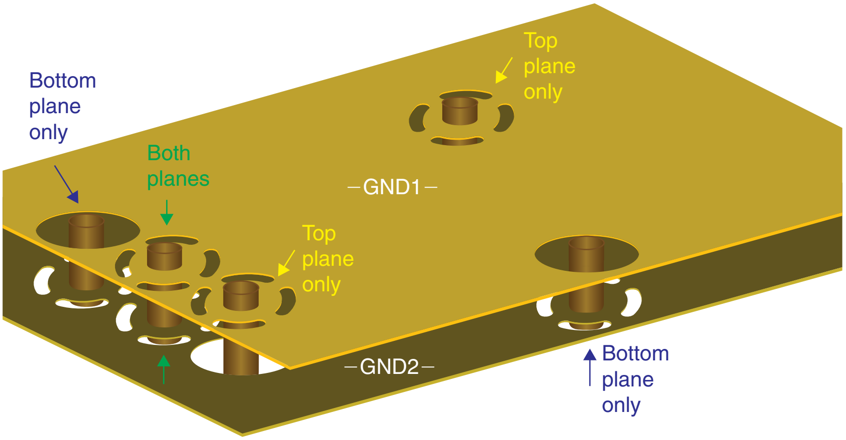
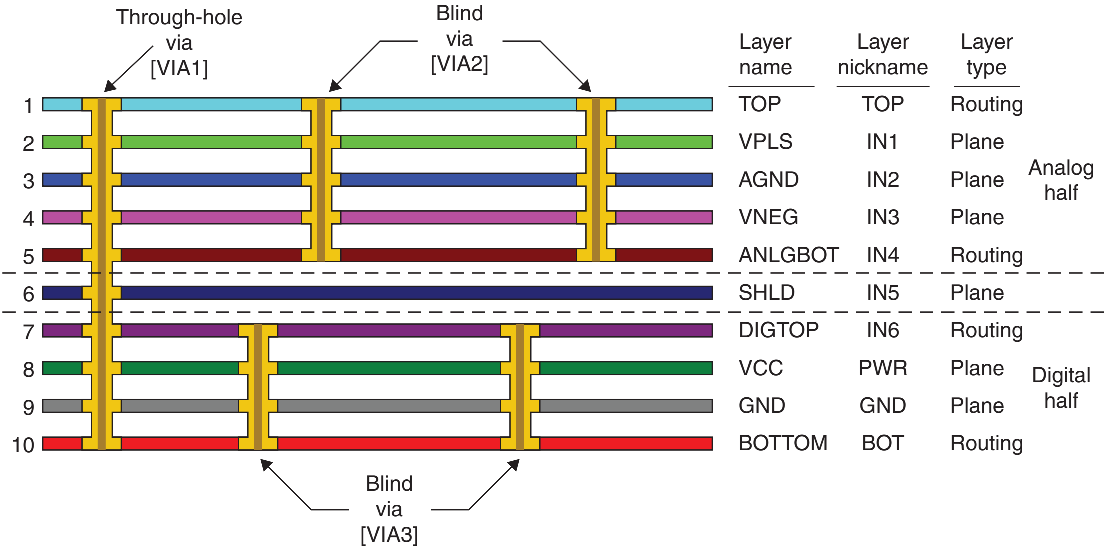

Bottom plane only
Both planes
Top plane only
Top plane only
−GND1−
−GND2−
Bottom plane only

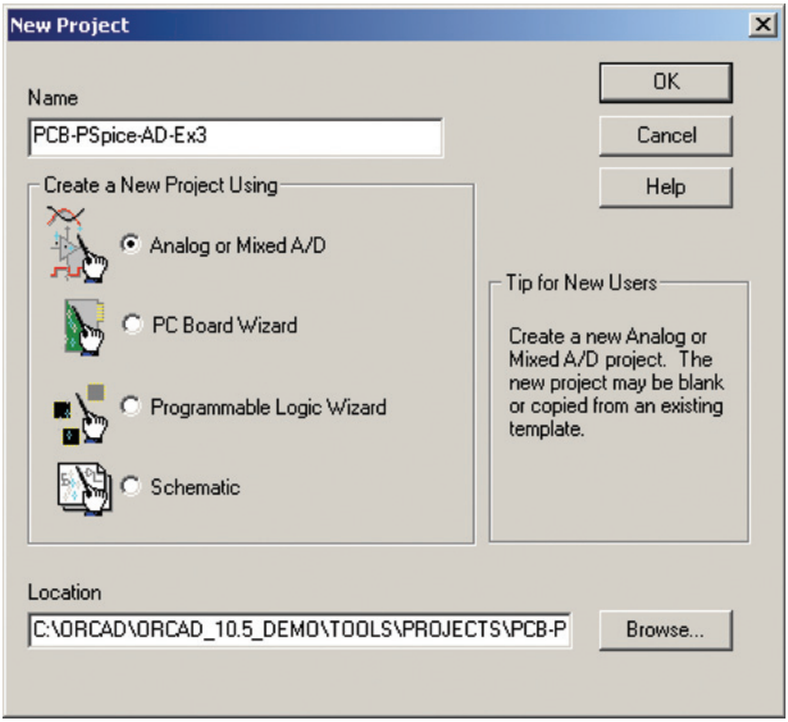
Figure 9-92 A specialized padstack used as a plane-to-plane connector.


Through-hole via [VIA1]
Blind via [VIA2]
Blind via [VIA3]

	Layer name	Layer nickname	Layer type	
1	TOP	TOP	Routing	
2	VPLS	IN1	Plane	Analog half
3	AGND	IN2	Plane	
4	VNEG	IN3	Plane	
5	ANLGBOT	IN4	Routing	
6	SHLD	IN5	Plane	
7	DIGTOP	IN6	Routing	
8	VCC	PWR	Plane	Digital half
9	GND	GND	Plane	
10	BOTTOM	BOT	Routing	

Figure 9-93 Layer stack-up for shielded dual-plane example with blind vias.

simulations in general is not provided in the example, but the process of setting up a project that allows PSpice simulations and the result of a basic simulation are included. To begin a PCB design project that can be simulated with PSpice, start Capture, and from the File menu select New → Project. When the New Project dialog box is displayed select the Analog or Mixed A/D option as shown in Fig. 9-94. Enter a name for the project, use the Browse... button to set up a new folder for the project, and click OK.


New Project
OK
Cancel
Help
Create a New Project Using
Analog or Mixed A/D
PC Board Wizard
Programmable Logic Wizard
Schematic
Tip for New Users
Location
Browse...

Name: PCB-PSpice-AD-Ex3

● Analog or Mixed A/D

Create a new Analog or Mixed A/D project. The new project may be blank or copied from an existing template.

Location: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\PCB-P

Figure 9-94 Beginning a new project for PCB design plus simulation.

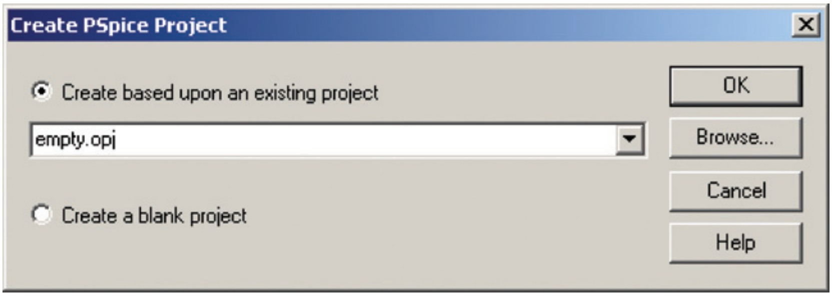
Note

- *The PC Board Wizard could also be used with the **Simulation Enabled** option but it is not functional in the Demo version.*

When the Create PSpice Project dialog box is displayed, select the Create based upon an existing project radio button and select the empty.opj project template as shown in Fig. 9-95. Click OK.

Adding schematic pages to the design

Three schematic pages will be needed for this project: one for analog circuitry, one for digital circuitry, and one for PSpice simulation sources. A new project initially contains one schematic page, Page1. This page will be renamed, and two more pages will be added. **To change the name of an existing schematic page**, select the Schematic Page icon, right click, and select Rename from the pop-up. Enter the name Analog in the dialog box and click OK. **To add a schematic page to a schematic folder** select the SCHEMATIC1 folder, right click, and select New Page from the pop-up menu (see Fig. 9-96(a)). Enter a name for the schematic



Create PSpice Project

● Create based upon an existing project

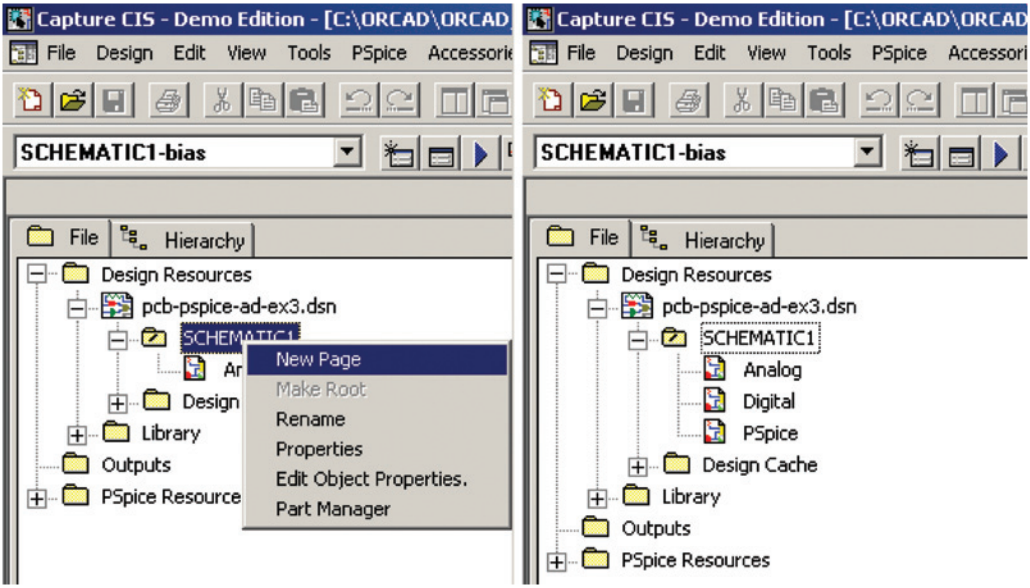
empty.opj

○ Create a blank project

OK
Browse...
Cancel
Help

Figure 9-95 Selecting a PSpice project template.

(e.g., Digital) and click OK. Add another schematic page to the SCHEMATIC1 folder and name it PSpice. The final schematic page structure is shown in Fig. 9-96(b).



Capture CIS - Demo Edition - [C:\ORCAD\ORCAD
File
Design
Edit
View
Tools
PSpice
Accessorie
SCHEMATIC1-bias
File
Hierarchy
Design Resources
pcb-pspice-ad-ex3.dsn
SCHEMATIC1
An
Design
Library
Outputs
PSpice Resource
New Page
Make Root
Rename
Properties
Edit Object Properties.
Part Manager
Capture CIS - Demo Edition - [C:\ORCAD\ORCAD
File
Design
Edit
View
Tools
PSpice
Accessori
SCHEMATIC1-bias
File
Hierarchy
Design Resources
pcb-pspice-ad-ex3.dsn
SCHEMATIC1
Analog
Digital
PSpice
Design Cache
Library
Outputs
PSpice Resources

Figure 9-96 Setting up a multipage project in Capture.

Begin by adding parts to the analog page. To display the analog page, double click the Analog Page icon in the Project Manager or select the analog page from the Window menu on the Capture toolbar. The analog page is shown in Fig. 9-97 and includes the analog components (U1, U2) and the connector (J1) from the previous example. The digital components are placed on the digital schematic page (see Fig. 9-100). New items in this project include off-page connectors and multiple ground symbols.

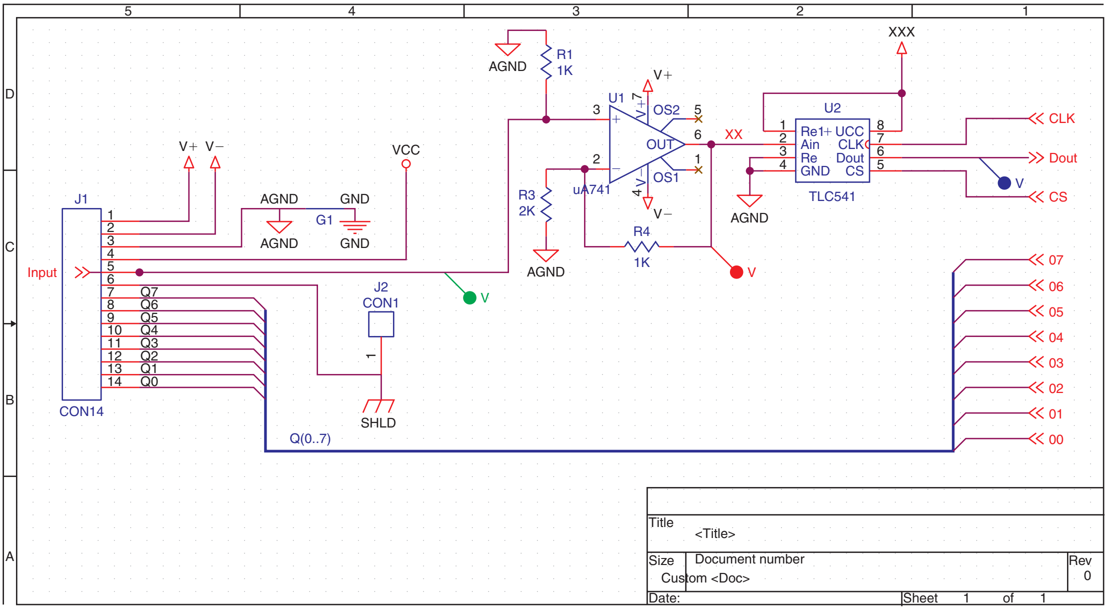

5
4
3
2
1
D
C
B
A
AGND
R1
1K
XXX
V+
U1
V+ 7
OS2
5
3
6
OUT
XX
U2
Re1+ UCC
Ain CLK
Re Dout
GND CS
TLC541
CLK
Dout
CS
V
V+ V−
VCC
J1
AGND
GND
G1
AGND
GND
R3
2K
uA741
4 V−
OS1
V−
R4
1K
AGND
Input
V
V
J2
CON1
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
SHLD
CON14
Q(0..7)
07
06
05
04
03
02
01
00
Title
<Title>
Size
Custom
Document number
<Doc>
Rev
0
Date:
Sheet 1 of 1

Figure 9-97 The analog schematic page.

Using off-page connectors with wires

Generally speaking, off-page connectors are used to continue signal nets across page boundaries. Off-page connectors are used in this example to connect signal lines between the ADC (on the analog page) and the microcontroller (which is on the digital page) and from the shift register (on the digital page) back to the connector (on the analog page). The off-page connectors are also used here to inject a PSpice signal originating from the PSpice page onto the analog input line (Input net as shown in Fig. 9-101 and described below).

Note that the off-page connector to pin 5 on U2 (chip select) does not contain the overbar (e.g., $\overline{CS}$, indicating an active low line) as does the pin name. Overbars can be generated on Capture schematic parts for nonpower-type pins, but do not use overbars on off-page connectors or power symbols as this will produce invalid netlist names.

Off-page connectors cannot be used with power symbols since they are already global and known by all pages within the design. If you connect a power symbol to an off-page connector, the connected power symbol will be isolated from the global net and given a default name (such as GND_101924). This extra GND will show up in Layout as a dark yellow (instead of bright yellow) rat's nest line and cell in the Nets spreadsheet. When this default net is routed in Layout it will *not* be connected to the rest of the power or ground system.

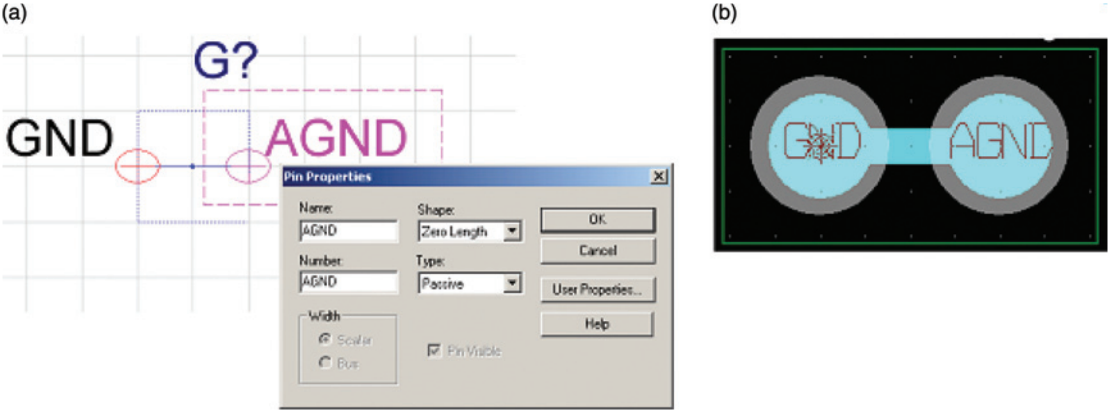
To place off-page connectors, select the Place Off-Page Connector tool button, ≪C on the schematic page toolbar or select Off-Page Connector... from the Place menu. In the Place Off-Page Connector... dialog box select one of the off-page connector symbols and enter the name that the connector will be attached to in the Name: text box; click OK and place the off-page connector on the schematic page. You can change the name of an off-page connector after it has been placed on the schematic. **To change the name of an off-page connector** double click the name; enter the new name in the Display Properties dialog box.

Using off-page connectors with busses

Both nets and busses can be connected across page boundaries with off-page connectors. If nets belonging to busses cross page boundaries by off-page connectors, net aliases (using the N1 button) are not required on the nets because the off-page connectors produce the aliases, otherwise net aliases are required to connect nets to the bus. For example, the nets connected to board connector J1 require aliases in order to be connected to the bus.

Setting up multiple-ground systems

Another difference between this design example and the previous one is the way the ground connections are made. In the previous example there were two ground symbols (AGND and GND) but only one actual ground net (GND). In that design the grounds were separated on the board using a split plane. In this example there are three ground symbols and three distinct ground nets (AGND, GND, and SHLD). The shield ground is indicated by a GND_EARTH symbol (renamed SHLD); it is connected to J1.6 by itself, and it will be the only connection the plane layer called SHLD. In Fig. 9-97 AGND and GND appear to be jointly connected to J1.3 but are actually separated by the special Capture part symbol (G1), which has a Layout footprint (GNDAGND), as shown in Fig. 9-98 along with the pin properties. The part (G1) and its footprint are custom parts and are not included with the standard OrCAD libraries but are included in the GNDJCT.OLB and PCB-PSPICE_EX.LLB files on the CD if you care to see them. G1 contains two pins that are graphically connected in the library part but are not connected as far as the netlist is concerned. The purpose of G1 is to indicate on the schematic that the grounds are connected, while allowing the grounds to remain separate nets in the netlist.

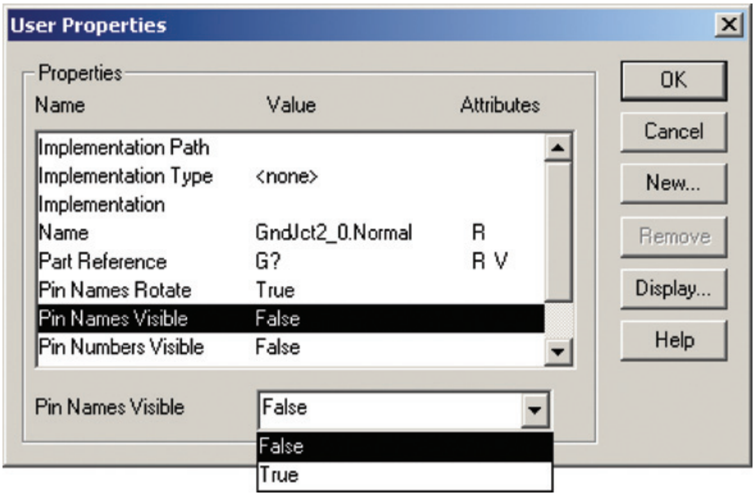


Name: AGND
Number: AGND
Shape: Zero Length
Type: Passive
Width
● Scalar
○ Bus
☑ Pin Visible

Figure 9-98 Multiground net connector. (a) Capture part. (b) Layout footprint.

After the connector has been placed on the board and wired to the appropriate ground nets you can turn off the part reference (G1) by selecting Do Not Display in the Display Properties dialog box (double click the part to show the dialog box).

You can also make the pin names invisible to make the part look like a wire. **To turn off the pin names** select the part, right click, and select Edit Part from the pop-up. From the Part Editor menu bar select Part Properties from the Options menu. At the User Properties dialog box (Fig. 9-99) select the Pin Names (Numbers) Visible option(s) and select False from the selection list.



Name	Value	Attributes
Implementation Path		
Implementation Type	<none>	
Implementation		
Name	GndJct2_0.Normal	R
Part Reference	G?	R V
Pin Names Rotate	True	
Pin Names Visible	False	
Pin Numbers Visible	False	

Pin Names Visible: False

False
True

Figure 9-99 Making pin names and numbers invisible.

Note from Fig. 9-97 that a connector, J2, is used with the chassis ground symbol. J2 is a single pin connector with a single padstack footprint that is used to connect the buried shield to the chassis enclosure. When we begin working in Layout you will see how the three ground connections will be made on the board.

Figure 9-100 shows the digital schematic page. Off-page connectors are used as described earlier. Unlike on the analog page, where each net in the bus had its own off-page connector, here the bus itself (and all the nets it contains) is attached to a single off-page connector that has the same name as the bus (e.g., Q[0..7]). Note also that off-page connectors are not used with the power and ground symbols as they are global and known by all schematic pages in the design.

Setting up PSpice sources

Figure 9-101 shows the PSpice page. Sources are VDC and VSIN, which can be found in the SOURCES.OLB library located in the Capture/Library/PSpice folder. Set the VDC and the VSIN source values as shown in the figure.

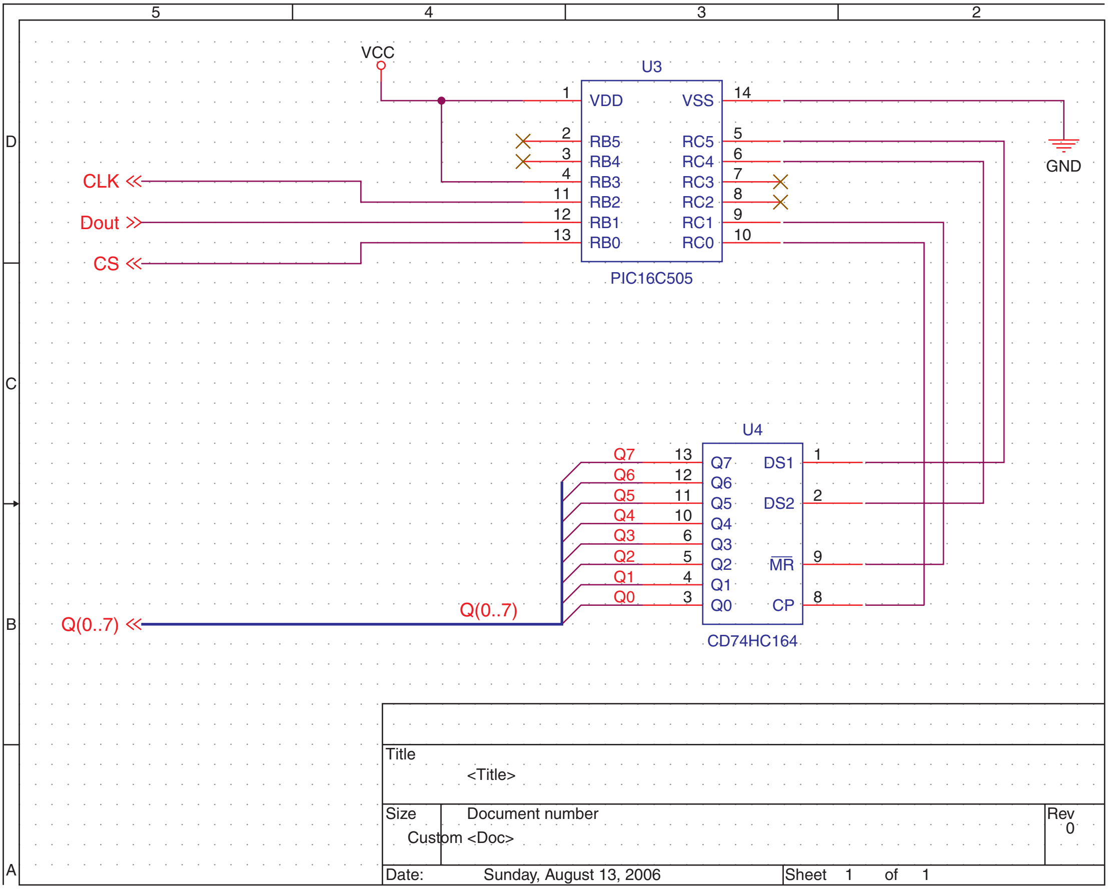

5
4
3
2
D
C
B
A
VCC
U3
VDD
VSS
RB5
RB4
RB3
RB2
RB1
RB0
RC5
RC4
RC3
RC2
RC1
RC0
1
2
3
4
11
12
13
14
5
6
7
8
9
10
PIC16C505
GND
CLK
Dout
CS
U4
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
DS1
DS2
MR
CP
CD74HC164
Q(0..7)
Title
<Title>
Size
Custom
Document number
<Doc>
Rev
0
Date:
Sunday, August 13, 2006
Sheet 1 of 1

Figure 9-100 The digital schematic page.

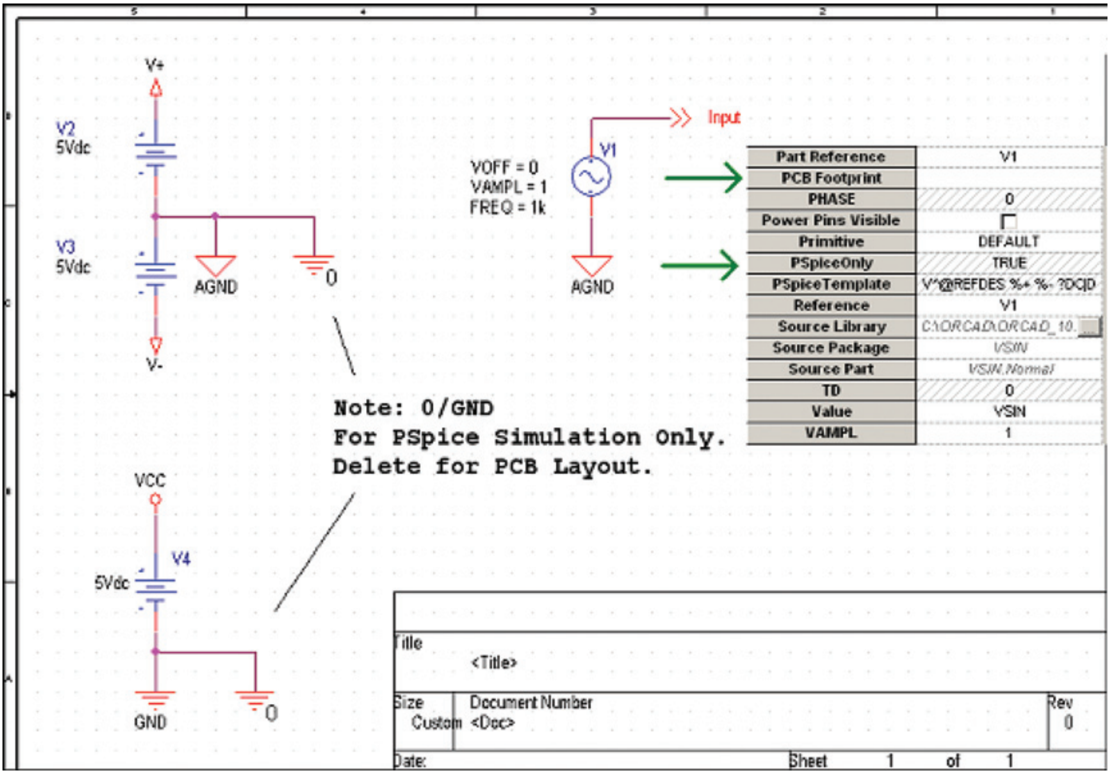
For all PSpice simulations there must be a 0/GND symbol that all sources can be referenced to. The 0/GND symbol is connected to both the analog and the digital grounds only during the simulation. After the circuit has been satisfactorily simulated, the 0/GND symbol is deleted. The 0/GND symbol is included with the other GND symbols in the CAPSYM library.

So that no footprints are added for the PSpice parts, make sure all PSpice parts are PSpiceOnly = TRUE and that the PCB Footprint cell is blank. To check these features double click a part to display the Part Properties spreadsheet. A partial spreadsheet is shown in Fig. 9-101.

Any parts that do not have PSpice templates will not be simulated. Parts U3 and U4, and all of the connectors, do not have PSpice templates. When the simulation is run they will be marked with a green dot and ignored.

Performing PSpice simulations

Once the circuit is made a PSpice simulation profile needs to be established. A default simulation profile is included with the project because the Analog or Mixed A/D... radio button



Part Reference	V1
PCB Footprint	
PHASE	0
Power Pins Visible	☐
Primitive	DEFAULT
PSpiceOnly	TRUE
PSpiceTemplate	V^@REFDES %+ %- ?DC|D
Reference	V1
Source Library	C:\ORCAD\ORCAD_10.
Source Package	VSIN
Source Part	VSIN.Normal
TD	0
Value	VSIN
VAMPL	1

Note: 0/GND
For PSpice Simulation Only.
Delete for PCB Layout.

Title <Title>
Size Custom
Document Number <Doc>
Rev 0
Date:
Sheet 1 of 1

Figure 9-101 The PSpice simulation page.

was chosen during the project setup. All that needs to be done is to edit it for this design. **To edit the PSpice simulation profile** select Edit Simulation Profile from the PSpice menu as shown in Fig. 9-102.

At the Simulation Settings dialog box (Fig. 9-103) select Time Domain (Transient) from the Analysis type: list as shown in Fig. 9-103. Enter a value in the Run to time: box to display three or so complete cycles of the waveform (3–5 ms for a 1-kHz signal). You can specify a value in the Maximum step size: box also, but this is optional. A value that is about 1/1000 the run time produces very smooth waveforms but takes longer to run. Click OK when you are finished.

To run the PSpice simulation click the Run PSpice button (blue triangle button) located on the schematic page toolbar (shown in Fig. 9-104).

The PSpice results are shown in Fig. 9-105. Three voltage markers (probes) were placed on the design, but only two waveforms are displayed in the probe window because not all of the parts in the design had PSpice models (templates) attached to them. PSpice will inform you that not all data were displayed by telling you, “No simulation data for marker ‘V(DOUT)’,” as is indicated by the blue arrow in Fig. 9-105.

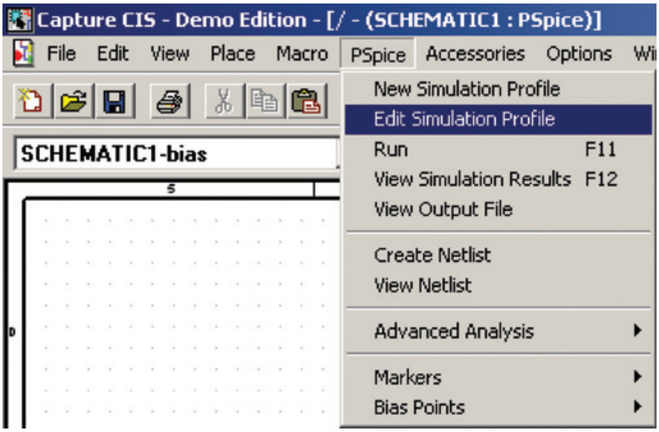
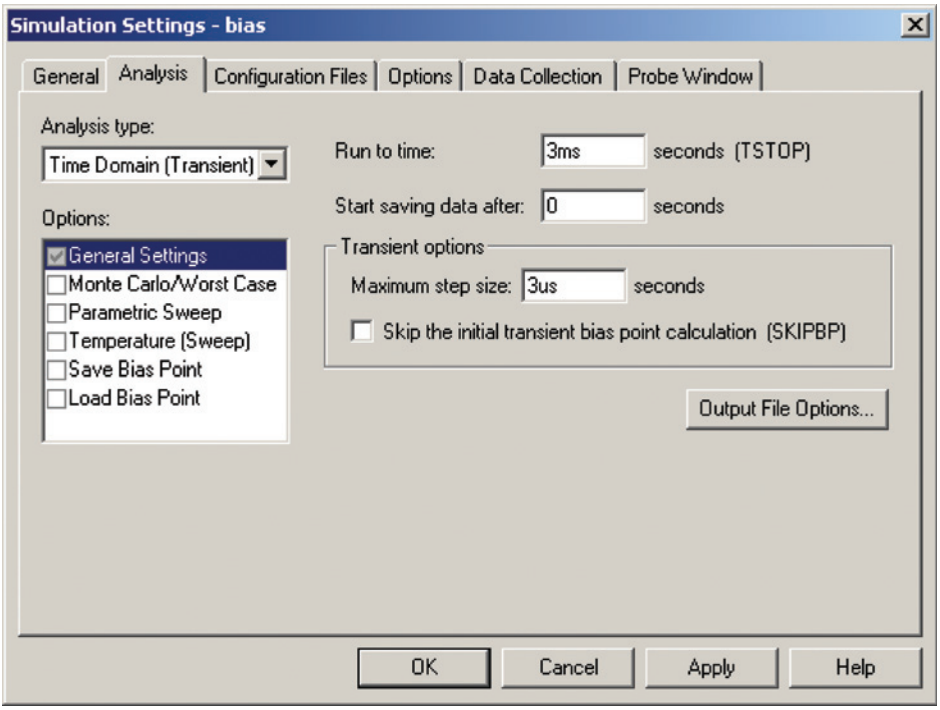

Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PSpice)]
File
Edit
View
Place
Macro
PSpice
Accessories
Options
Wi
SCHEMATIC1-bias
New Simulation Profile
Edit Simulation Profile
Run F11
View Simulation Results F12
View Output File
Create Netlist
View Netlist
Advanced Analysis
Markers
Bias Points

Figure 9-102 Editing the PSpice simulation profile.


Simulation Settings - bias
General
Analysis
Configuration Files
Options
Data Collection
Probe Window
Output File Options...
OK
Cancel
Apply
Help

Analysis type: Time Domain (Transient)

Options:
☑ General Settings
☐ Monte Carlo/Worst Case
☐ Parametric Sweep
☐ Temperature (Sweep)
☐ Save Bias Point
☐ Load Bias Point

Run to time: 3ms seconds (TSTOP)

Start saving data after: 0 seconds

Transient options

Maximum step size: 3us seconds

☐ Skip the initial transient bias point calculation (SKIPBP)

Figure 9-103 Setup for time domain analysis.

To perform time domain simulations use the VSIN source; to perform frequency domain simulations use the VAC source and select AC Sweep/Noise in the Simulation Settings dialog box (Fig. 9-103). There are many other types of sources that can be used to perform simulations. You can even create specialized stimulus files (including noise signals) using

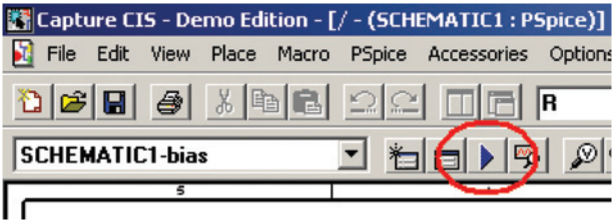
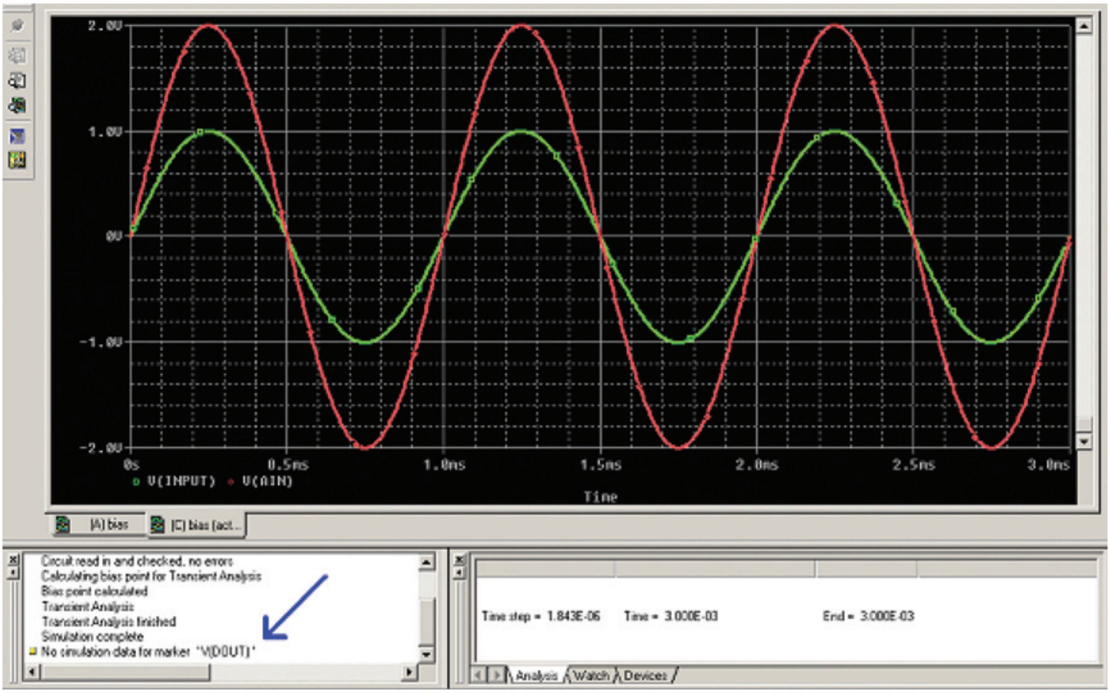

Capture CIS - Demo Edition - [/ - (SCHEMATIC1 : PSpice)]
File
Edit
View
Place
Macro
PSpice
Accessories
Options
R
SCHEMATIC1-bias

Figure 9-104 Run PSpice.


2.0V
1.0V
0V
-1.0V
-2.0V
0s
0.5ms
1.0ms
1.5ms
2.0ms
2.5ms
3.0ms
V(INPUT)
V(AIN)
Time
(A) bias
(C) bias (act...
Analysis
Watch
Devices

```
Circuit read in and checked, no errors
Calculating bias point for Transient Analysis
Bias point calculated
Transient Analysis
Transient Analysis finished
Simulation complete
No simulation data for marker "V(DOUT)"
```

```
Time step = 1.843E-06     Time = 3.000E-03          End = 3.000E-03
```

Figure 9-105 PSpice simulation results using a VSIN stimulus.

one of the VPWL_FILE sources. To see how to use these other sources see the *PSpice User's Guide* (pspug.pdf—search for "stimulus files") included in the OrCAD documents folder, or see one of the many texts that specialize in PSpice simulations.

Preparing the simulated project for Layout

Once the PSpice simulations are complete and the circuit has been verified the design is ready to be prepared for Layout. One of the first tasks is to assign (or verify) footprint assignments for all parts. As described in the previous examples a custom BOM can be generated to list the footprints to make it easier to identify missing or incorrect footprints (see the previous examples and Chap. 11 for details). A sample BOM for this design is shown in Table 9-8.

Reference	Part	Part library	Footprint
G1	GndJct2	GNDJCT.OLB	GNDAGND
J1	CON14	..CAPTURE\LIBRARY\CONNECTOR.OLB	BLKCON.100/VH/TM1 SQ/W.100/14
J2	CON1	..CAPTURE\LIBRARY\CONNECTOR.OLB	BLKCON.100/VH/TM1R/W.100/1
R1,R4	1k	..CAPTURE\LIBRARY\DISCRETE.OLB	SM/R 1210
R2,R3	2k	..CAPTURE\LIBRARY\DISCRETE.OLB	SM/R 1210
U1	uA741	..CAPTURE\LIBRARY\PSPICE\EVAL.OLB	SOG.050/8/WG.244/L225
U2	TLC548	CHAPTER9.OLB	SOG.050/8/WG.244/L225
U3	PIC16C505	CHAPTER9.OLB	DIP.100/14/W.300/L 800
U4	CD74HC164	CHAPTER9.OLB	SOG.050/14/WG.244/L350

Table 9-8 BOM footprint list for dual-page plane example

The remaining tasks were described above in the preceding text or in earlier examples and are listed here without details.

- Remove 0/GND symbols used for PSpice simulations.
- Perform an annotation to clean up numbering.
- Make sure that global power nets are properly utilized.
- Perform a DRC in Capture to verify that the circuit design has no issues. Correct any errors and reperform the DRC as needed.
- Use Capture to generate the .MNL netlist for Layout.

Assigning a new technology file

As described in the previous example the board design is set up by starting Layout and selecting a technology file. From the main session window select File → New to display the AutoECO dialog box. For this example use the 3bet_any.tch file. Load the .MNL file generated from Capture and create the .MAX file by clicking the Apply ECO button.

As described above, use the Obstacle tool to draw the board outline. A 2 × 1.25-in. board is sufficient for this design. Use part search tools to find parts and place them inside the board outline. Place digital parts on the bottom side of the board as shown in Fig. 9-106.

Placing parts on the bottom (back) of a board

To place parts on the bottom side of a board, use the Component Selection tool to select a part (or parts), right click, and select Opposite from the pop-up (or hit the T key on your keyboard). Right click again and select End Command to complete the action. Perform a DRC to check for footprint and placement problems prior to doing anything else.

Layer stack-up for a multiground system

The layer stack-up shown in Fig. 9-93 will be used in this design. Set up power, ground, and shield planes and the analog and digital routing layers as shown in the Layers spreadsheet in Fig. 9-107. To modify a layer double click the layer name to display the Edit Layer dialog box. Modify the layer names and types as necessary. Remember to change the Layer

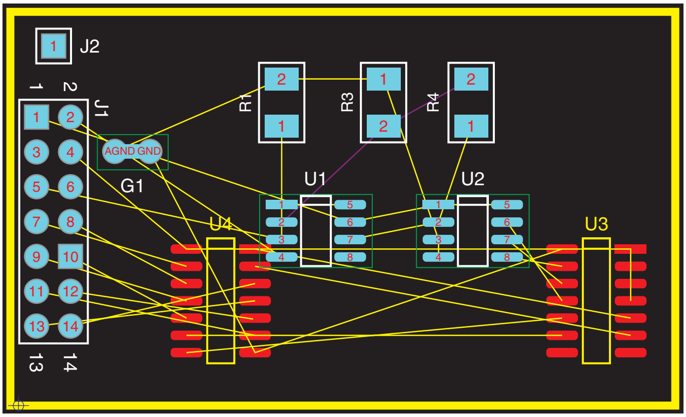


Figure 9-106 Initial part placement for Example 3.

Layer Name	Layer Hotkey	Layer NickName	Layer Type	Mirror Layer
TOP	1	TOP	Routing	BOTTOM
BOTTOM	2	BOT	Routing	TOP
GND	3	GND	Plane	[None]
VCC	4	PWR	Plane	[None]
VPLS	5	IN1	Plane	[None]
AGND	6	IN2	Plane	[None]
VNEG	7	IN3	Plane	[None]
ANLGBOT	8	IN4	Routing	[None]
SHLD	9	IN5	Plane	[None]
DIGTOP	Ctrl + 0	IN6	Routing	[None]
INNER7	Ctrl + 1	IN7	Unused	[None]
INNER8	Ctrl + 2	IN8	Unused	[None]
INNER9	Ctrl + 3	IN9	Unused	[None]
INNER10	Ctrl + 4	I10	Unused	[None]
INNER11	Ctrl + 5	I11	Unused	[None]
INNER12	Ctrl + 6	I12	Unused	[None]
SMTOP	Ctrl + 7	SMT	Doc	SMBOT
SMBOT	Ctrl + 8	SMB	Doc	SMTOP
SPTOP	Ctrl + 9	SPT	Doc	SPBOT
SPBOT	Shift + 0	SPB	Doc	SPTOP
SSTOP	Shift + 1	SST	Doc	SSBOT
SSBOT	Shift + 2	SSB	Doc	SSTOP
ASYTOP	Shift + 3	AST	Doc	ASYBOT
ASYBOT	Shift + 4	ASB	Doc	ASYTOP
DRLDWG	Shift + 5	DRD	Doc	[None]
DRILL	Shift + 6	DRL	Drill	[None]
FABDWG	Shift + 7	FAB	Doc	[None]
NOTES	Shift + 8	NOT	Doc	[None]

Figure 9-107 Layer setup in Layout.

LibName and Layer Type for the new plane layers. See the previous examples for more details on editing layers.

Net layer assignments

The next step is to assign nets to the proper layers. The net layer assignments are shown in Table 9-9. **To make net layer assignments**, open the Nets spreadsheet. Double click a net to display the Edit Net dialog box. Click the Net Layers... button to display the Layers Enabled for Routing dialog box. Select the appropriate layers per Table 9-9.

Net	Routing	Plane	Via
Vpls	TOP	VPLS	VIA2
AGND	TOP	AGND	VIA2
Vneg	TOP	VNEG	VIA2
Analog nets	TOP, ANLGBOT	—	VIA2
SHLD	—	SHLD	(VIA1)
VCC	BOTTOM	PWR	VIA3
GND	BOTTOM	GND	VIA3
Digital nets	DIGTOP, BOTTOM	—	VIA3

Table 9-9 Net assignments

Through-hole and blind via setup

As indicated in Fig. 9-93 blind vias will be required for this design. Set up/select vias and thermal reliefs as shown in Table 9-10 (all dimensions are in mils).

To define via parameters select the View Spreadsheets button on the toolbar and select Padstacks from the pop-up menu. Scroll through the padstack list until you find the desired padstack. Double click the layer names to display Edit Padstack Layer dialog box. Change the pad shapes, widths, and heights as shown in Table 9-10. You can also change the names of the vias to make them easier to remember their functions.

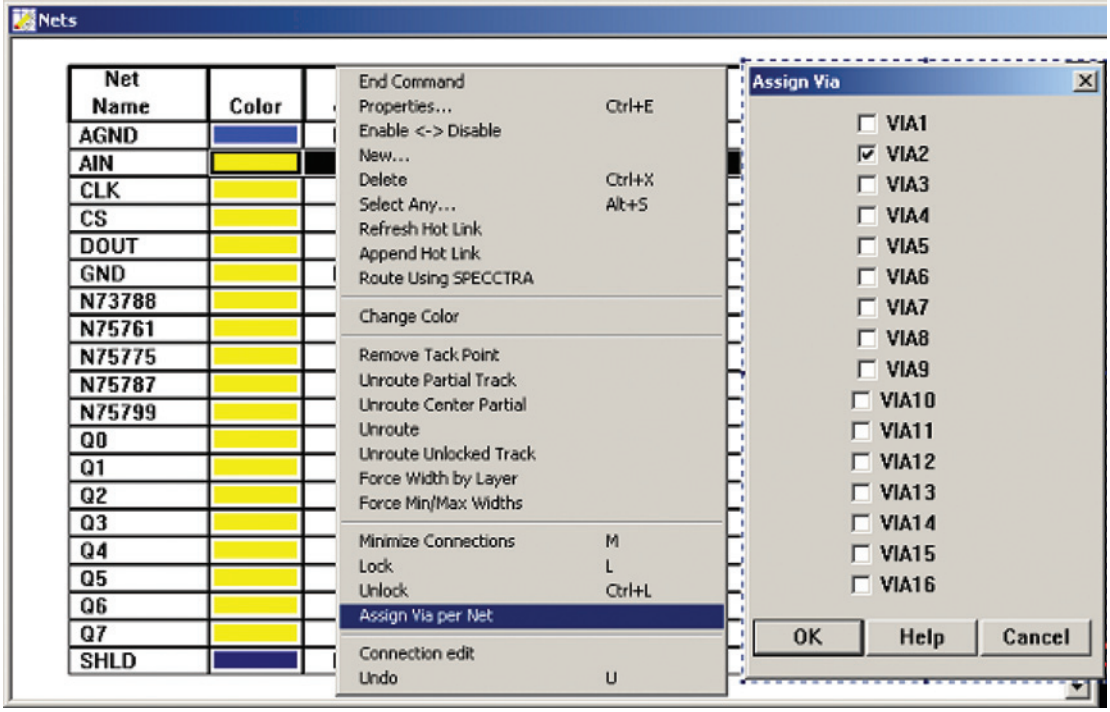
Note that the digital nets are assigned VIA3 except for the CLK, CS, and DATA nets. The exceptions are assigned VIA1 so that connections can be made through the SHLD when going from the TOP (analog-to-digital IC) to the BOTTOM (microcontroller IC). **To assign a specific via to a net** open the Nets spreadsheet. Left click a net name to select it and then right click and select Assign Via per Net from the pop-up (see Fig. 9-108). At the Assign Via selection box select the desired via per Table 9-10. Via assignments need to be completed for each net.

Fanning out a board with multiple vias

Since the analog and digital systems have unique vias for the power and ground planes the fanout must be done individually for each one. We will begin by fanning out the analog

	VIA1		VIA2		VIA3	
Pad type	**Dim.**	**Layers**	**Dim.**	**Layers**	**Dim.**	**Layers**
Routing	40	TOP, BOTTOM, all INNER	35	TOP, ANLGBOT	35	DIGTOP, BOTTOM
Clearance	70	GND, VCC, VPLS, AGND, VNEG, SHLD	65	VPLS, VNEG, AGND	65	VCC, GND
DrilL	20	DRLDWC, DRILL	15	DRLDWC, DRILL	15	DRLDWC, DRILL
SM	45	SMTOP, SMBOT	40	SMTOP	40	SMBOT
Undefined	n/a	None	n/a	All digital layers, SHLD	n/a	All analog layers, SHLD
Circuit		Either (through PCB)		Analog (top of PCB)		Digital (bottom of PCB)

Table 9-10 Through-hole and Blind Via Definitions

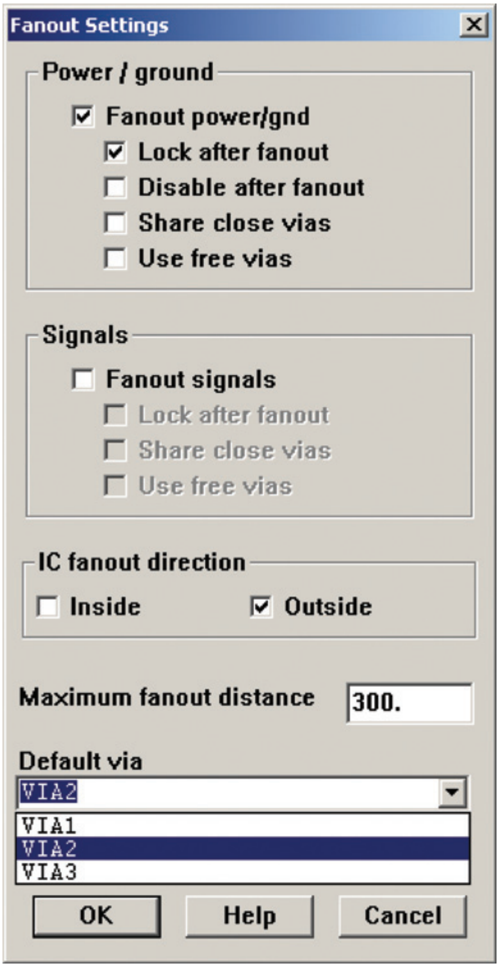

Nets
End Command
Properties... Ctrl+E
Enable <-> Disable
New...
Delete Ctrl+X
Select Any... Alt+S
Refresh Hot Link
Append Hot Link
Route Using SPECCTRA
Change Color
Remove Tack Point
Unroute Partial Track
Unroute Center Partial
Unroute
Unroute Unlocked Track
Force Width by Layer
Force Min/Max Widths
Minimize Connections M
Lock L
Unlock Ctrl+L
Assign Via per Net
Connection edit
Undo U
Assign Via
OK
Help
Cancel

Net Name	Color
AGND	🟦
AIN	🟨
CLK	🟨
CS	🟨
DOUT	🟨
GND	🟨
N73788	🟨
N75761	🟨
N75775	🟨
N75787	🟨
N75799	🟨
Q0	🟨
Q1	🟨
Q2	🟨
Q3	🟨
Q4	🟨
Q5	🟨
Q6	🟨
Q7	🟨
SHLD	🟦

☐ VIA1
☑ VIA2
☐ VIA3
☐ VIA4
☐ VIA5
☐ VIA6
☐ VIA7
☐ VIA8
☐ VIA9
☐ VIA10
☐ VIA11
☐ VIA12
☐ VIA13
☐ VIA14
☐ VIA15
☐ VIA16

Figure 9-108 Assigning specific vias to nets.

circuit. Use the Nets spreadsheet to disable all nets but analog power and ground. Assign VIA2 to the fanouts. **To assign a via for fanouts** select Fanout Settings... from the Options menu. The Fanout Settings dialog box (Fig. 9-109) will be displayed. Select VIA2 from the Default via selection list and click OK. To begin the fanout navigate to Auto → Fanout → Board from the menu bar. When satisfied with the fanout disable and lock the



Power / ground

☑ Fanout power/gnd
☑ Lock after fanout
☐ Disable after fanout
☐ Share close vias
☐ Use free vias

Signals

☐ Fanout signals
☐ Lock after fanout
☐ Share close vias
☐ Use free vias

IC fanout direction

☐ Inside ☑ Outside

Maximum fanout distance 300.

Default via

VIA2

VIA1
VIA2
VIA3

Figure 9-109 Assigning specific fanout vias.

analog power/ground nets. Then enable the digital power and ground nets. Assign VIA3 to the fanouts and perform Auto → Fanout → Board again. When satisfied with the fanout disable and lock the digital power/ground nets.

Use the Refresh All button and cycle through the plane layers to verify the fanouts. As you cycle through the layers to view each one, you should notice that the blind vias do not show up on all of the layers (for example, the BOTTOM color does not show up on VIA3, etc.).

Run a DRC to check for errors. A minimum of two errors will result (Pad Spacing Errors). This is a side effect of using the copper strip method to connect the planes. Since we know what the cause is (and it is intentional) we can get around the error by telling Layout to ignore it.

Overriding known errors in Layout

To override a known error open the Error Markers spreadsheet using the View Spreadsheet button and selecting the Error Markers option. Select the two pad spacing errors related to the copper strip obstacle and the two ground pins, right click, and select Mark as Good DRC from the pop-up. The error markers will be colored pink; they are not actually eliminated, but they will not prevent the postprocessor from creating the Gerber files (errors will normally stop the postprocessor in its tracks).

With the power and ground fanouts complete we move onto the next task: routing the nets running from the ADC to the microcontroller (CLK, CS, DOUT). Since they must go from the top side of the board to the bottom side and must pass through the shield plane these nets must use VIA1. Using the procedure described above (see Fig. 9-109) set VIA1 as the default via. Since there are only three nets enabled you can either route the nets manually or use the Autopath Route Mode to make the autorouter route the three traces or have the autorouter route the traces with the DRC box.

Autorouting with the DRC/route box

When using the DRC route box the autorouter will route only traces within the boundary of the route box. Since you can control the size of the route box you can control how much of the board the autorouter will route at one time. **To change the size of the route box** select Zoom DCR/Route Box from the View menu (see Fig. 9-110), or press the B key on the

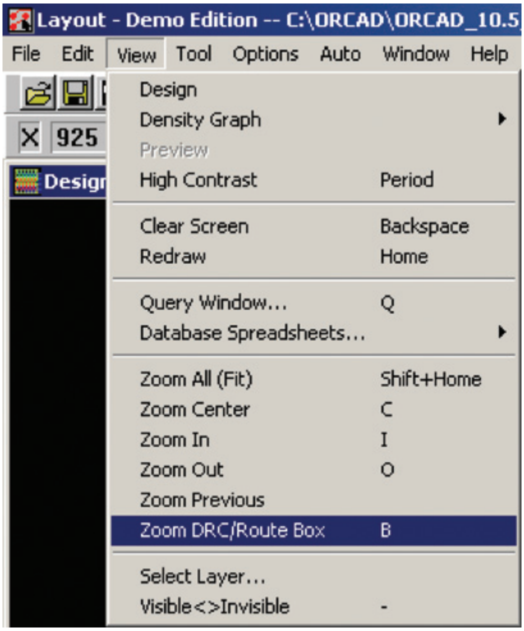

Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5
File
Edit
View
Tool
Options
Auto
Window
Help
925
Design
Design
Density Graph
Preview
High Contrast	Period
Clear Screen	Backspace
Redraw	Home
Query Window...	Q
Database Spreadsheets...
Zoom All (Fit)	Shift+Home
Zoom Center	C
Zoom In	I
Zoom Out	O
Zoom Previous
Zoom DRC/Route Box	B
Select Layer...
Visible<>Invisible	-

Figure 9-110 Using the Zoom DRC to set the route box.

keyboard. The "zoom" cursor will be displayed. Drag a box with the left mouse button around the area you want to route. Layout will zoom the view to the area defined by the new route box. Zoom out (press the O key) to see the route box. Figure 9-111 shows a route box defined around the analog-to-digital converter and microcontroller.

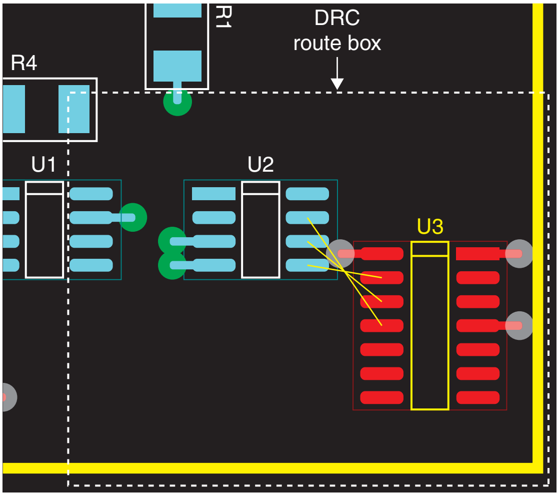


Figure 9-111 A resized route box.

Once the route box is set you can have the autorouter route enabled traces inside the route box. **To autoroute traces using the DRC route box** select Autoroute → DRC/Route Box from the Auto menu. Figure 9-112 shows the three digital nets routed by the route box (traces marked with *) as well as the three types of vias used in the design.

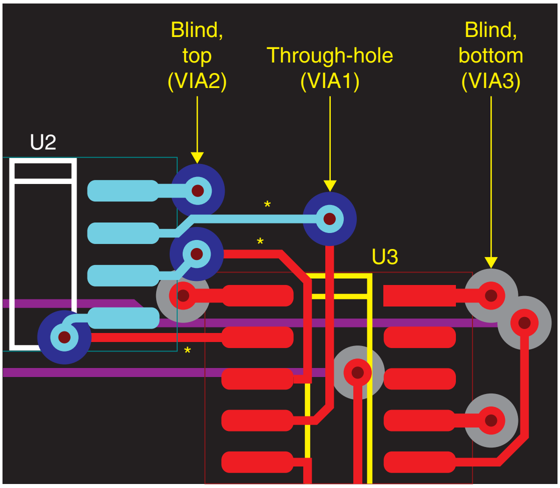


Figure 9-112 Routing with blind vias and through-holes.

After fanning out power and ground and prerouting traces, perform a DRC prior to running the autorouter to catch any errors. Next, disable all power and ground nets and any prerouted nets. Enable all of the other nets and run the autorouter by selecting Autoroute → Board from the Auto menu. The final board design is shown in Fig. 9-113.

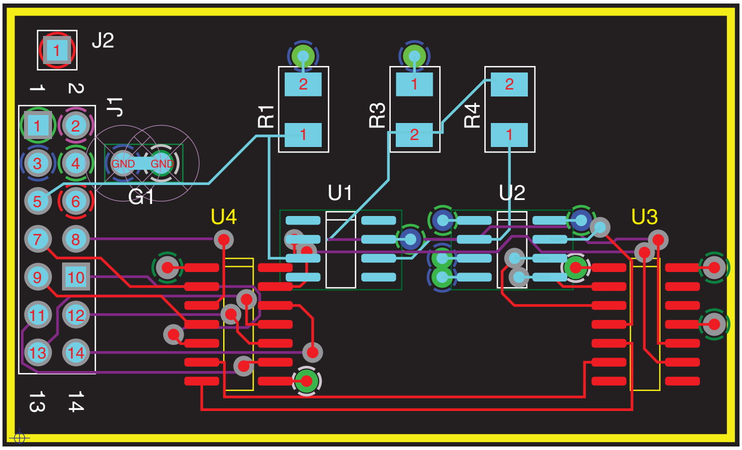


Figure 9-113 Final multiground plane board layout.

Using forced thermals to connect ground planes

Rather than take up space on the board using a dedicated footprint and having to put up with the two DRC errors, you can instead modify one of the connector pins (padstack J1.3, for example) that is attached to one of the ground planes so that it is attached to both ground planes at the same time. You can also do this with a modified free via. We will make a new padstack based on the properties of the existing J1.3 and then assign the *modified* padstack to J1.3.

When using this approach the special part (G1) in Capture is not used. Instead a small segment of a graphical line—using the Place Line tool instead of the Place Wire tool—is used to indicate that the two grounds are connected at the header pin. This will eliminate the footprint in Layout, which in turn will eliminate the two DRC errors or eliminate having to solder a jumper wire to the board to make the connection.

To use the thermal relief method of connecting isolated planes instead of the copper strip method, delete part G1 in Capture. Use the Place Line tool to make the AGND and GND nets look like they are connected as shown in Fig. 9-114. Perform an AutoECO to forward annotate the changes to Layout.

Using the AutoECO to update a board from Capture

Run the AutoECO tool from Capture to update the PCB in Layout. The process is the same as when you initially performed the AutoECO with one exception. **To run an AutoECO to update an existing board** with new information from Capture, navigate to the Project

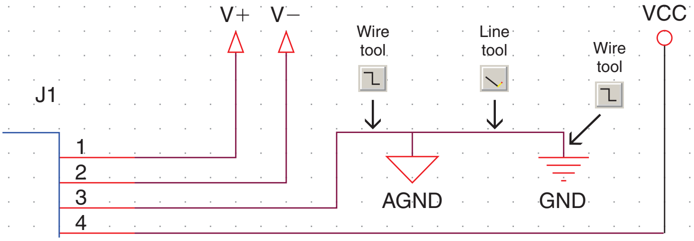
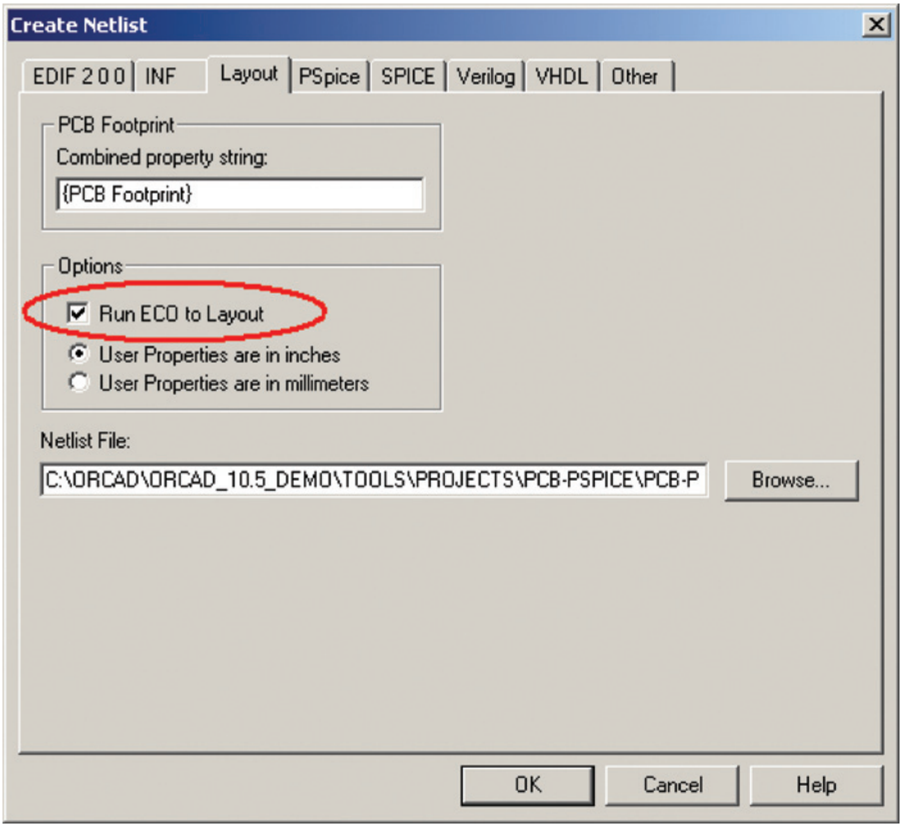

V+
V−
VCC
Wire
tool
Line
tool
Wire
tool
J1
1
2
3
4
AGND
GND

Figure 9-114 New ground connection using the Line tool.

Manager and select the **Design** icon. From the **Tools** menu select **Create Netlist....** At the **Create Netlist** dialog box select the **Run ECO to Layout** box as shown in Fig. 9-115. Make sure too that the .MNL file is the same as it was when you set up the board initially. Unless you made any changes to it during the design process, it will be the same. If you are not sure what the original .MNL file was you can check by looking at the .MNL icon in the **Outputs**


Create Netlist
EDIF 2 0 0
INF
Layout
PSpice
SPICE
Verilog
VHDL
Other
PCB Footprint
Options
Browse...
OK
Cancel
Help

Combined property string: {PCB Footprint}

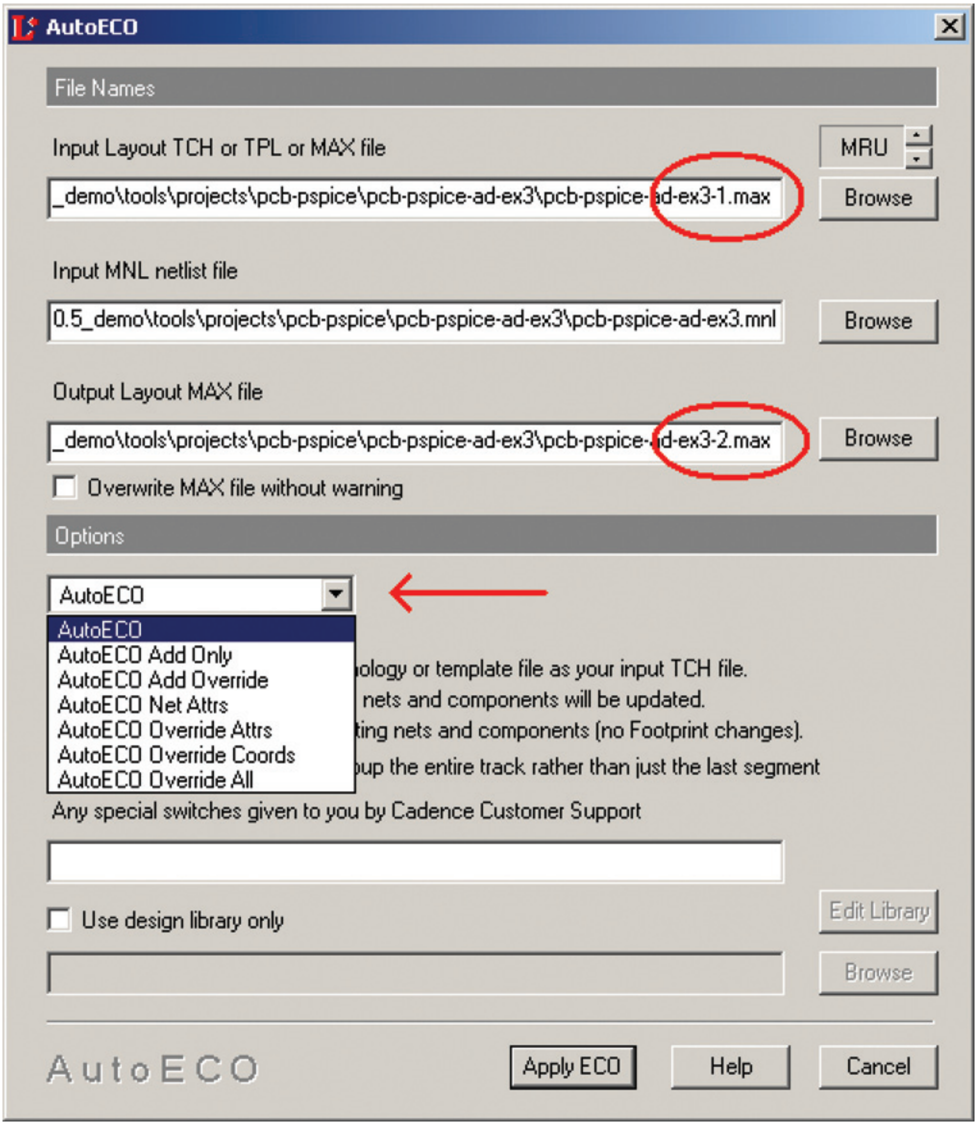
☑ Run ECO to Layout
● User Properties are in inches
○ User Properties are in millimeters

Netlist File: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\PCB-PSPICE\PCB-P

Figure 9-115 Using the AutoECO to update the PCB from changes in Capture.

folder in the Project Manager window in Capture. Make sure the name in the Netlist File: box matches the .MNL file (icon) in the Project Manager. Click the OK button to run the ECO.

When you make the Layout design window active again Layout will display the message, “This job’s netlist has changed, Update C:\...*name*.MAX?” Click Yes. The AutoECO dialog box will be displayed (Fig. 9-116). Notice from the figure that the input file is automatically filled in this time, and it is the current board file (.MAX) rather than a technology file (.TCH). The netlist file is also filled in with the current .MNL file. The output file is also automatically



AutoECO

File Names

Input Layout TCH or TPL or MAX file: _demo\tools\projects\pcb-pspice\pcb-pspice-ad-ex3\pcb-pspice-ad-ex3-1.max

Input MNL netlist file: 0.5_demo\tools\projects\pcb-pspice\pcb-pspice-ad-ex3\pcb-pspice-ad-ex3.mnl

Output Layout MAX file: _demo\tools\projects\pcb-pspice\pcb-pspice-ad-ex3\pcb-pspice-ad-ex3-2.max

☐ Overwrite MAX file without warning

Options

AutoECO

ology or template file as your input TCH file.
nets and components will be updated.
ting nets and components (no Footprint changes).
up the entire track rather than just the last segment

Any special switches given to you by Cadence Customer Support

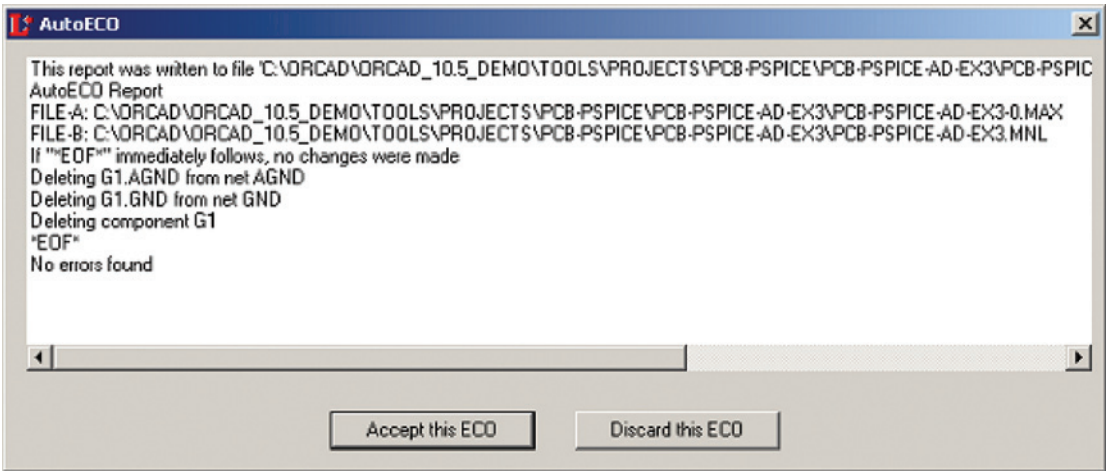
☐ Use design library only

MRU
Browse
Browse
Browse
AutoECO
AutoECO Add Only
AutoECO Add Override
AutoECO Net Attrs
AutoECO Override Attrs
AutoECO Override Coords
AutoECO Override All
Edit Library
Browse
AutoECO
Apply ECO
Help
Cancel

Figure 9-116 Using the AutoECO to update changes from Capture to Layout.

filled in and is given the same name as the current file except that the revision number is automatically incremented by 1. From the Options list you can select the type of ECO you want to run (see Tables 9-15 and 9-16). To update the design in this example the default, AutoECO, can be selected since a component is being deleted and we want the board to match the schematic. Click the Apply ECO button to update the board. See the AutoECO section at the end of this chapter for more information on the different types of ECOs.

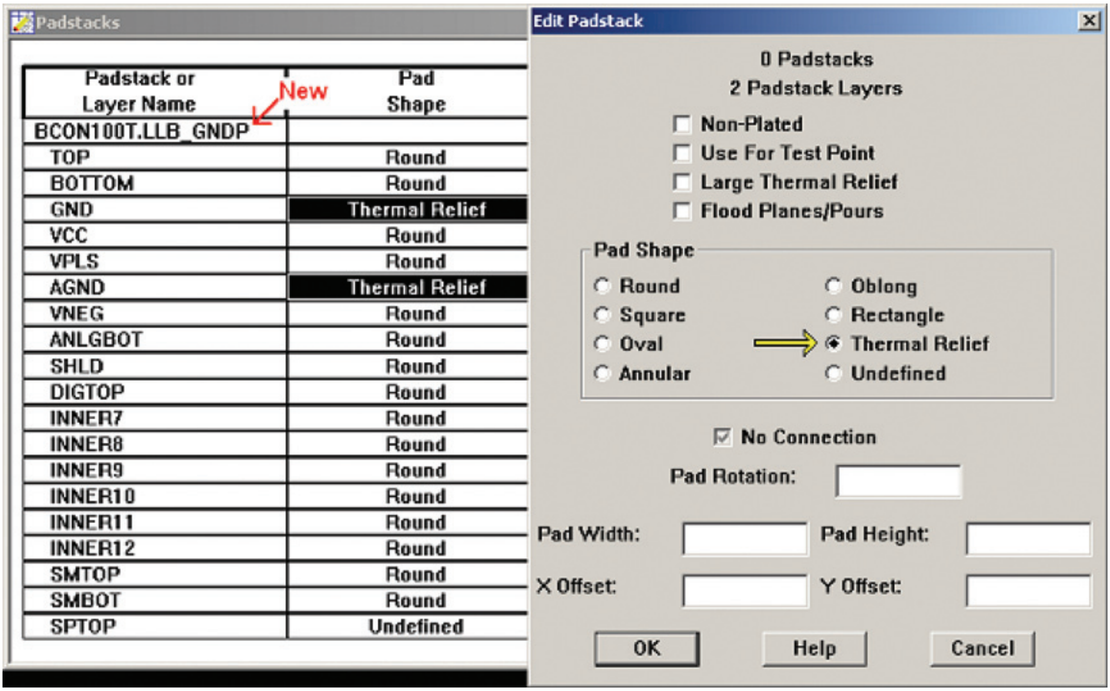
After the ECO has been run, Layout will display an AutoECO report (Fig, 9-117). If the actions taken are correct, click the Accept this ECO button. Click OK when the Processing Completed information box is displayed.



```
This report was written to file 'C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\PCB-PSPICE\PCB-PSPICE-AD-EX3\PCB-PSPIC
AutoECO Report
FILE-A: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\PCB-PSPICE\PCB-PSPICE-AD-EX3\PCB-PSPICE-AD-EX3-0.MAX
FILE-B: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\PCB-PSPICE\PCB-PSPICE-AD-EX3\PCB-PSPICE-AD-EX3.MNL
If "*EOF*" immediately follows, no changes were made
Deleting G1.AGND from net AGND
Deleting G1.GND from net GND
Deleting component G1
*EOF*
No errors found
```

Figure 9-117 The AutoECO report.

Once the ECO is complete, the connections can be made between the AGND plane and the GND plane by shorting them together at pin J1.3. To modify the J1 footprint use Enable Editing of Footprints (from Options → User Preferences menu). Find out the characteristics of the existing pin by selecting J1.3 using the Pin tool, ① open the Padstacks spreadsheet, and BCON100T.LLB_PAD1 will be highlighted (since that is what J1.3 is). With BCON100T.LLB_PAD1 selected, right click, and select New... from the pop-up. A new padstack is created with the default name BCON100T.LLB_PAD3 (BCON100T.LLB_PAD2 is for the square ones J1.1 and J1.10). Select the BCON100T.LLB_PAD3 cell, right click, and select Properties... from the pop-up. Change the name to something like BCON100T.LLB_GNDP (for ground post) and click OK. On the spreadsheet select the GND and AGND cells, right click, and select Properties...from the pop-up. Change the Pad Shape to Thermal Relief as shown in Fig. 9-118. Click OK and close the spreadsheet. Assigning the thermal reliefs to the pads on the layers used as ground plane will short them together regardless of what the netlist says. Since Layout assumes you are doing this on purpose it will not generate a DRC error (even if you inadvertently short the wrong planes together).



Padstack or Layer Name	Pad Shape
BCON100T.LLB_GNDP	
TOP	Round
BOTTOM	Round
GND	Thermal Relief
VCC	Round
VPLS	Round
AGND	Thermal Relief
VNEG	Round
ANLGBOT	Round
SHLD	Round
DIGTOP	Round
INNER7	Round
INNER8	Round
INNER9	Round
INNER10	Round
INNER11	Round
INNER12	Round
SMTOP	Round
SMBOT	Round
SPTOP	Undefined

Edit Padstack

0 Padstacks
2 Padstack Layers

☐ Non-Plated
☐ Use For Test Point
☐ Large Thermal Relief
☐ Flood Planes/Pours

Pad Shape
○ Round
○ Square
○ Oval
○ Annular
○ Oblong
○ Rectangle
● Thermal Relief
○ Undefined

☑ No Connection

Pad Rotation:
Pad Width:
Pad Height:
X Offset:
Y Offset:

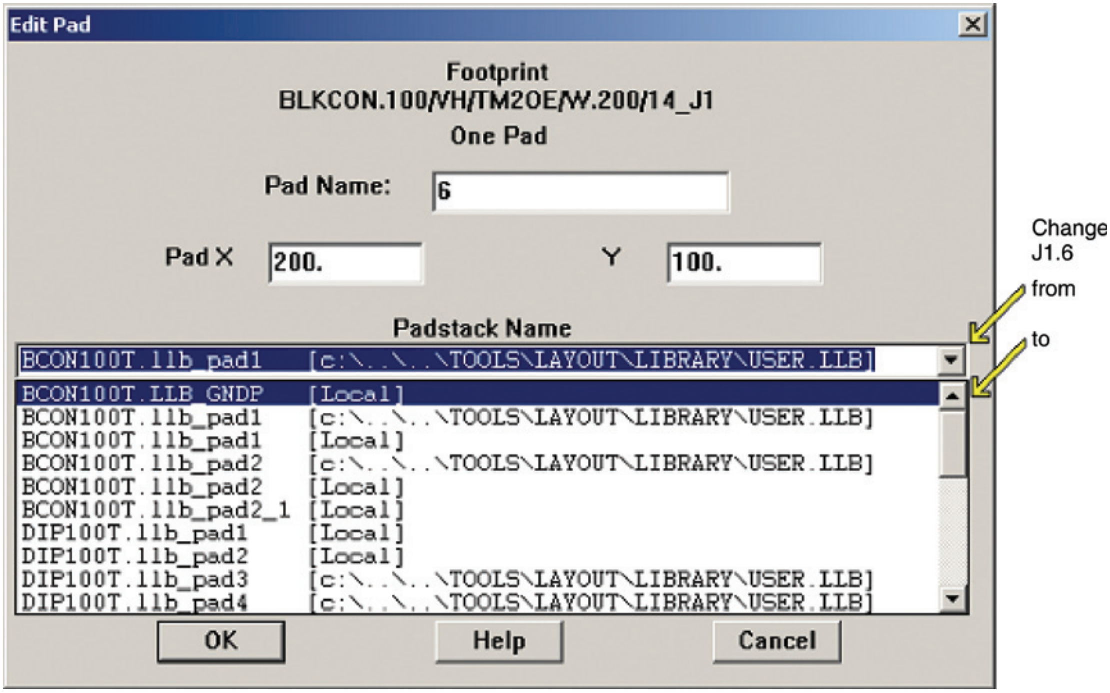
Figure 9-118 Forcing a padstack to connect the GND and AGND planes.

Once the new padstack is made and modified, assign it to J1.3. Select J1.3 again using the Pin tool, right click, and select Properties... from the pop-up. In the Edit Pad dialog box select the new BCON100T.LLB_GNDP padstack instead of the BCON100T.LLB_PAD1 from the Padstack Name list as shown in Fig. 9-119. Click OK and then right click and select End Command to enact the change.

Pin J1.3 is now connected to both the GND and the AGND planes through the plating and the thermal reliefs. To verify the connection to the AGND layer, make the AGND layer active (hit the 6 key on your keyboard or select IN2 from the layer selection list). You should see the blue thermal relief around J1.3 as shown in Fig. 9-120(a). To verify the connection to the GND layer, make the GND layer active (hit the 3 key on your keyboard or use the layer selection list and select the GND layer). You should see a gray (or whichever color you chose) thermal relief around J1.3 as shown in Fig. 9-120(b). The final board design is shown in Fig. 9-121.

Example 4: High-Speed Digital Design

This example demonstrates how to stack up the layers and design transmission lines for a high-speed digital PCB. The example also demonstrates how to create a moated ground area with a bridge around a high-frequency crystal oscillator, how to perform pin/gate swapping, and how to create a heat spreader using free vias to the ground plane. The example circuit is shown in Fig. 9-122.



Footprint
BLKCON.100/VH/TM2OE/W.200/14_J1
One Pad

Pad Name: 6

Pad X 200. Y 100.

Padstack Name

```
BCON100T.llb_pad1    [c:\..\..\TOOLS\LAYOUT\LIBRARY\USER.LLB]

BCON100T.LLB_GNDP    [Local]
BCON100T.llb_pad1    [c:\..\..\TOOLS\LAYOUT\LIBRARY\USER.LLB]
BCON100T.llb_pad1    [Local]
BCON100T.llb_pad2    [c:\..\..\TOOLS\LAYOUT\LIBRARY\USER.LLB]
BCON100T.llb_pad2    [Local]
BCON100T.llb_pad2_1  [Local]
DIP100T.llb_pad1     [Local]
DIP100T.llb_pad2     [Local]
DIP100T.llb_pad3     [c:\..\..\TOOLS\LAYOUT\LIBRARY\USER.LLB]
DIP100T.llb_pad4     [c:\..\..\TOOLS\LAYOUT\LIBRARY\USER.LLB]
```

Figure 9-119 Changing a pin's padstack type (for Example 3).

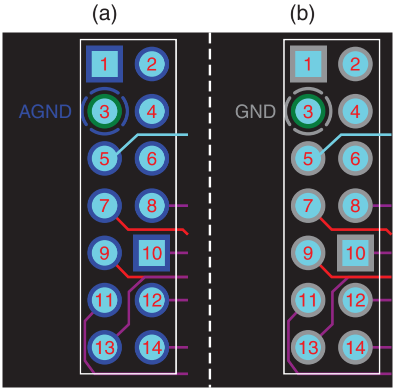


Figure 9-120 Verifying the connection to the two ground planes. (a) J1.3 to AGND. (b) J1.3 to GND.

The BOM for this example is shown in Table 9-11. The circuit consists of a (fictional) high-speed, low-pin-count microcontroller/digital signal processor (uP-EXD10) driven by a 66-MHz clock (X1), a digital to fiber optic interface IC (FO-TX, which mimics an ADN2530 but with fewer pins), a fiber optic laser diode (LD1), and a couple of 54ALS00 NAND gates used for I/O decoding. The digital signals have rise and fall times from 200 ps to 1.9 ns and

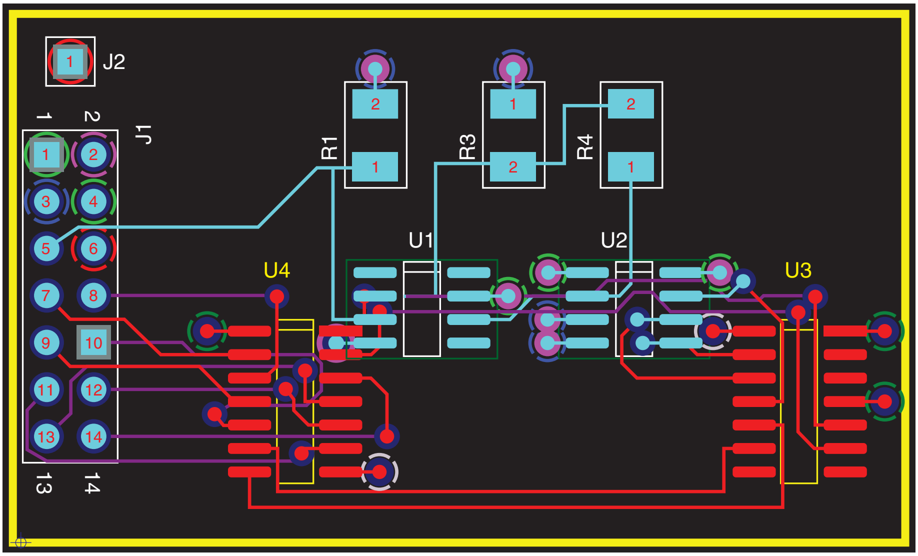

J2
1
J1
1
2
13
14
R1
R3
R4
U1
U2
U3
U4
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 9-121 The final, altered board design (for Example 3).

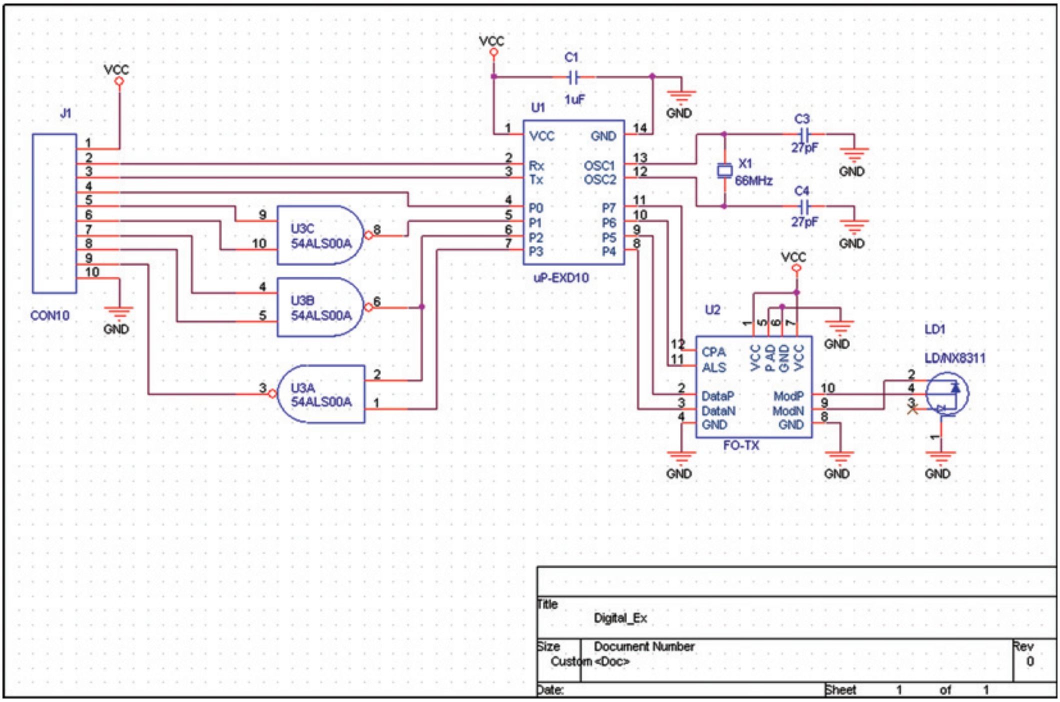

VCC
J1
CON10
GND
VCC
C1
1uF
U1
VCC
GND
Rx
Tx
OSC1
OSC2
P0
P1
P2
P3
P7
P6
P5
P4
uP-EXD10
U3C
54ALS00A
U3B
54ALS00A
U3A
54ALS00A
X1
66MHz
C3
27pF
C4
27pF
GND
VCC
U2
CPA
ALS
DataP
DataN
GND
ModP
ModN
GND
VCC
PAD
GND
VCC
FO-TX
LD1
LD/NX8311
Title
Digital_Ex
Size
Custom
Document Number
<Doc>
Rev
0
Date:
Sheet
1
of
1

Figure 9-122 High-speed digital circuit schematic.

Item	Reference	Part	Nomenclature	Footprint
1	C1,C2	1 µF	Bypass capacitor	SM/C_0805X
2	C3,C4	27pF	OSC capacitor	SM/C_0805X
3	J1	CON10	10-pin connector	BLKCON.100/VH/TM1SQ/W.100/10
4	LD1	LD/NX8311	Fiber optic laser diode, connector	LD/NX8311
5	U1	uP-EXD10	Microcontroller/signal processor	SOG.050/14/WG.244/L.350
6	U2	FO-TX	Digital to fiber interface IC	QFN50P300X300X100-12/1
7	U3	54ALS00	NAND logic gate	SOG.050/14/WG. 244/L.350
8	X1	XTAL	66 MHz crystal/oscillator	XCM39

Table 9-11 Bill of materials for the digital design example

require controlled impedance traces (see the Analog Devices ADN2530 data sheet for an example application). In a real design more bypass capacitors would be used on the circuit, but the design is scaled down to fewer than 10 parts and fewer than or equal to 14 pins per part to allow the use of the Demo version. The parts and footprints are located on the CD (in the Digital_Ex folder) included with the book.

Using the procedures described in the earlier examples start a new project, and place and connect the parts as shown in Fig. 9-122. After completing the schematic, make sure all footprints are assigned to the parts and then create the Digital-EX.MNL netlist for Layout.

Open Layout and start a new board project using the procedures described in the previous examples. You can use any of the technology files, but the 3bet-any.TCH technology file was used during the development of this board design (also included on the CD). The reason that it was chosen was that the default trace widths are 6 mils, which made it easy to route traces to the small pads on U2. No matter which file is chosen, some modifications will be required to complete the design.

As in the previous examples the first step is to make a board outline and place the parts inside the boundary. The initial board layout is shown in Fig. 9-123. Signal flow is from left to right, with the highest frequency components located close together near the laser diode connector on the right side of the board.

The next few steps were covered in detail in the previous examples. The following tables and figures show the design parameters for this example, but step-by-step instructions are not repeated here. The required steps are: (1) define the layer stack-up and enable the appropriate layers using the Layers spreadsheet, (2) make net-to-layer assignments using the Nets spreadsheet and Edit Net dialog box, (3) define two vias in addition to the default VIA1 using the Padstack spreadsheet and Edit Padstack dialog boxes, and (4) fan out power and ground for the surface-mounted components.

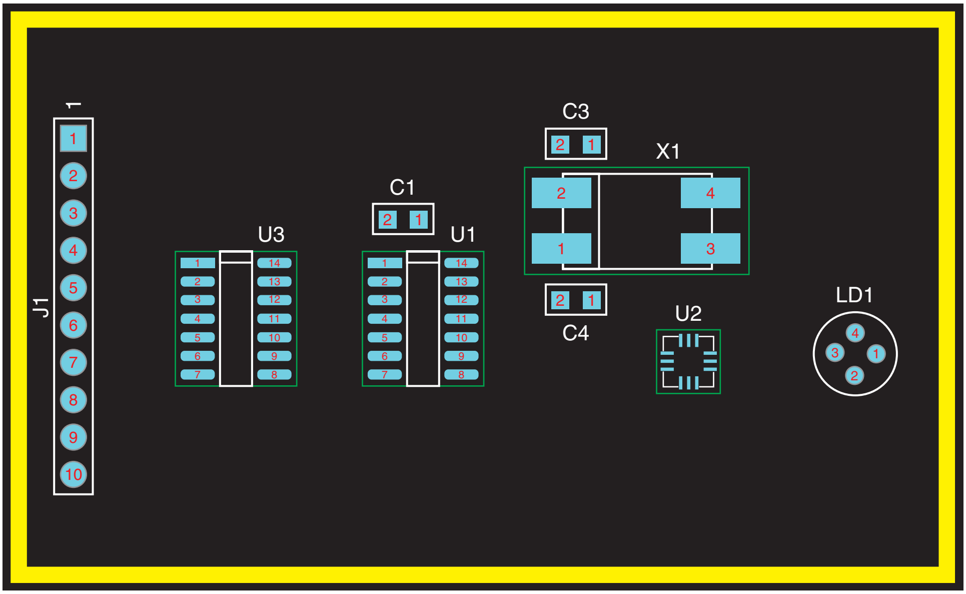
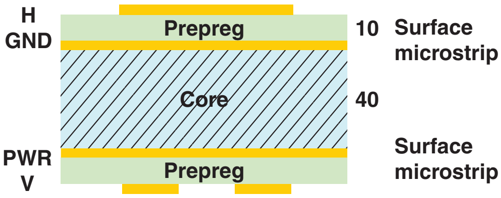


Figure 9-123 Initial board layout for digital design example.

Layer setup for microstrip transmission lines

Since there are so few parts a simple four-layer board design is used. The layer stack-up and net assignments are shown in Fig. 9-124. The layer thicknesses depend on the board manufacturer; the values (units in mils) shown in the figure are typical. The top layer and ground plane will be used to route surface-type microstrip transmission lines and most of the lower speed digital traces. Only low-speed traces that cannot be routed on the top will be routed on the bottom layer.



Layer name	Layer type	Used by nets:
Top (TOP)	Routing	Any/All
Power (PWR)	Plane	VCC
Ground (GND)	Plane	GND
INNER (IN1-I12)	Unused	None
Bottom (BOT)	Routing	Any/All

Figure 9-124 Layer stack-up for the digital example.

Three via types are used in this example (Table 9-12).. VIA1 is the default via included with the technology file. VIA2 and VIA3 are custom vias that are smaller in size and are tented (i.e., the padstack contains no soldermask definitions). VIA2 is used for fanouts where the smaller pad size allows greater population density. Multiple VIA3's will be used as heat pipes

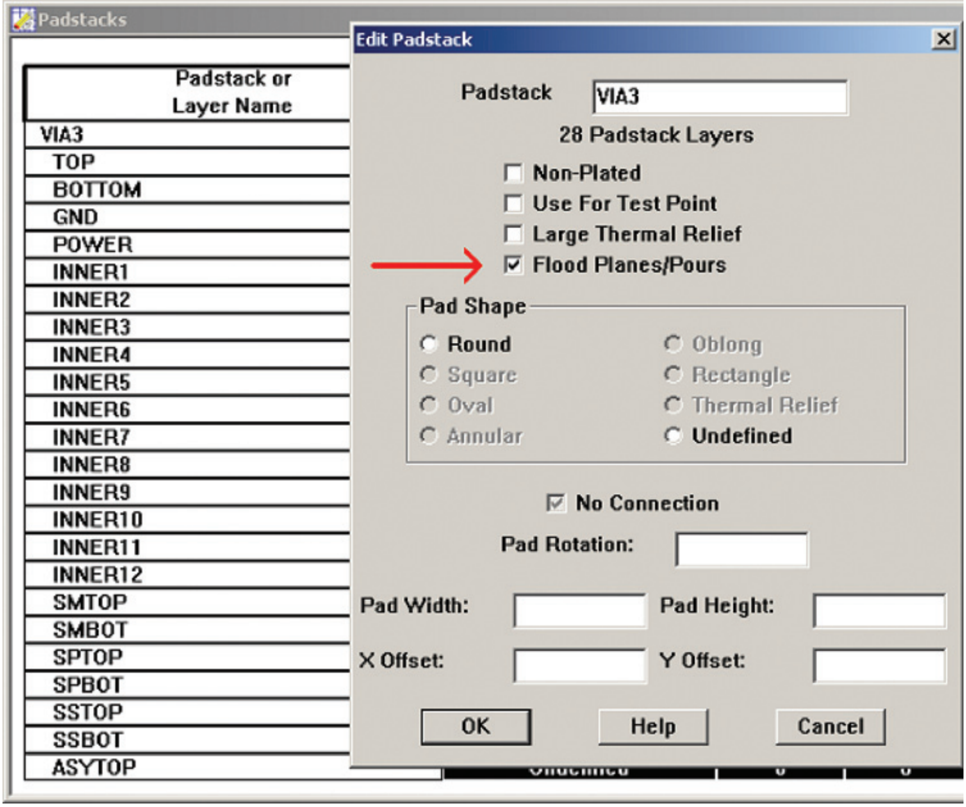
Via name	Function	Pads	Clearance	Drills	Connection to plane
VIA1	Default	36	70	20	Thermal relief
VIA2	PWR/GND fanouts	20	30	10	Thermal relief
VIA3	Heat pipes	20	25	10	Flood planes/pours

Table 9-12 List of vias used in the digital example

to connect a thermal pad (a copper area obstacle) beneath U2 to the ground plane and function as a heat spreader.

Via design for heat spreaders

To make VIA3 efficient at conducting heat, solid connections to the plane are used rather than thermal reliefs. **To assign Flood Planes/Pours to vias** instead of thermal reliefs open the Padstack spreadsheet and double click the via's name to display the Edit Padstack dialog box (Fig. 9-125); select the Flood Planes/Pours option.


Padstacks
Padstack or Layer Name
VIA3
TOP
BOTTOM
GND
POWER
INNER1
INNER2
INNER3
INNER4
INNER5
INNER6
INNER7
INNER8
INNER9
INNER10
INNER11
INNER12
SMTOP
SMBOT
SPTOP
SPBOT
SSTOP
SSBOT
ASYTOP
Edit Padstack
OK
Help
Cancel

Padstack: VIA3

28 Padstack Layers

☐ Non-Plated
☐ Use For Test Point
☐ Large Thermal Relief
☑ Flood Planes/Pours

Pad Shape

○ Round
○ Square
○ Oval
○ Annular
○ Oblong
○ Rectangle
○ Thermal Relief
○ Undefined

☑ No Connection

Pad Rotation:

Pad Width:

Pad Height:

X Offset:

Y Offset:

Figure 9-125 Assigning via connections to planes.

Constructing a heat spreader with copper area obstacles

The design of heat spreaders on PCBs depends significantly on the type of device and how it is attached to the board. For design examples and thermal management calculations see the application notes references listed in Appendix F. The heat spreader demonstrated here is based on the design suggestions for the ADN2530.

Before the board is fanned out or any traces are routed, the heat spreader will be put into place so that Layout avoids that area, thereby preventing having to rip up and reroute the fanouts or traces. A functional diagram of one type of heat spreader is shown in Fig. 9-126. The silicon die inside the component is thermally bonded to a metal pad on the bottom of a specially designed package. The pad is in turn thermally bonded (either by soldering or thermal compound) to a copper area on the top layer of the PCB. The copper area has an opening in the soldermask and multiple vias used to connect it to a plane layer (either ground or power depending on the chip design). The vias function as thermal conductors (heat pipes) that allow heat to flow away from the component. If a component dissipates excessive heat the plane layer can be mechanically (and thermally) connected to a larger heat sink or other mounting hardware to help dissipate the heat.

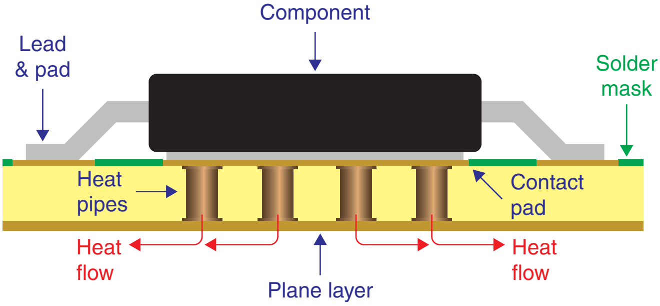


Figure 9-126 Functional diagram of a heat spreader.

Using free vias as heat pipes

The heat spreader consists of free vias and a copper area obstacle, both of which can be connected to any plane or net or left isolated from all nets. There are three methods to add free vias to a PCB.

The first method is used only while routing traces with one of the manual routing tools. **To add a free via with a routing tool** select the net to be routed and place at least one vertex on the board, right click, and select Change Via Type from the pop-up. The Via Selection box (Fig. 9-127) will be displayed; select the desired via and click OK. Right click again and select Add Free Via from the pop-up. The free via will automatically be placed at the vertex.

The second method uses the Add Free Via dialog box to select and place the via. **To add a free via using the Add Free Via dialog box** click the Tool menu and select Via → New... from the dropdown menu. At the Add Free Via dialog box (Fig. 9-128) select the desired via

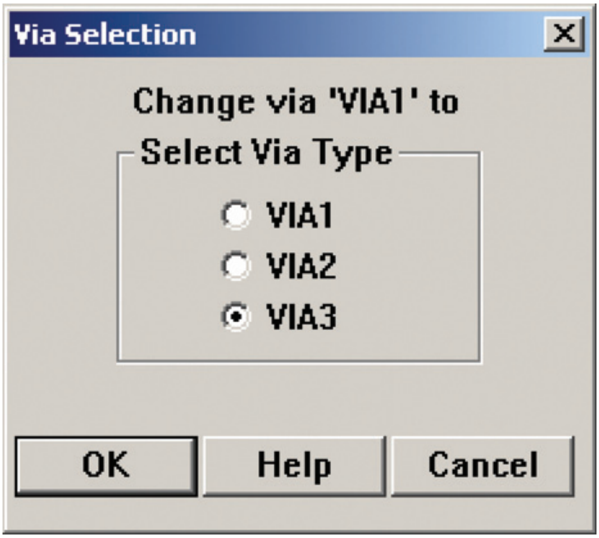


Figure 9-127 ***Via Selection*** *dialog box.*

to use and the net connection (if any). Enter the location if known, or delete the *x*/*y* coordinates to place the via manually. Click OK.

• •

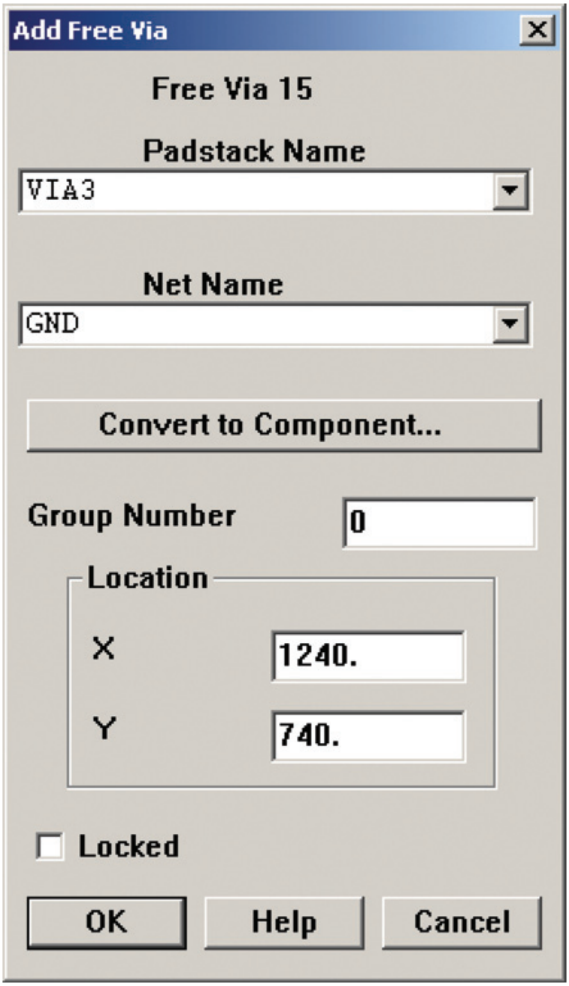
Note

- *A free via is actually a type of component/net hybrid, so if you are using the Demo version and have 10 components on the board Layout will not display the dialog box. Also, if you unroute a trace, a free via will not be deleted.* ***To delete a free via*** *choose one of the manual routing tools, select the free via, and hit the* ***Delete*** *key on your keyboard because the* ***Unroute*** *command does not work on free vias.* ***To move a free*** **via** *choose the* ***Edit Segment Mode*** *route tool.*

• •

The third method of placing free vias is to use the Free Via Matrix tool, which allows you to place multiple, evenly spaced vias on the PCB with one command. This is a good way to place the multiple vias required for the heat spreader and will be used as such here. **To place free vias using the Free Via Matrix tool** select Free Via Matrix Settings... from the Options menu (see Fig. 9-129). In the Free Via Matrix Settings dialog box select the desired via and net connection and enter the vertical and horizontal spacing between vias.

The Add/Edit Route Mode routing tool will be used to draw a box that defines the matrix location. Set the resolution of the routing grid high enough so that you can more precisely place the box in the desired location. Set the routing grid (Options → System Settings) to 5 mils for this example.



Add Free Via

Free Via 15

Padstack Name: VIA3

Net Name: GND

Group Number: 0

Location

X: 1240.

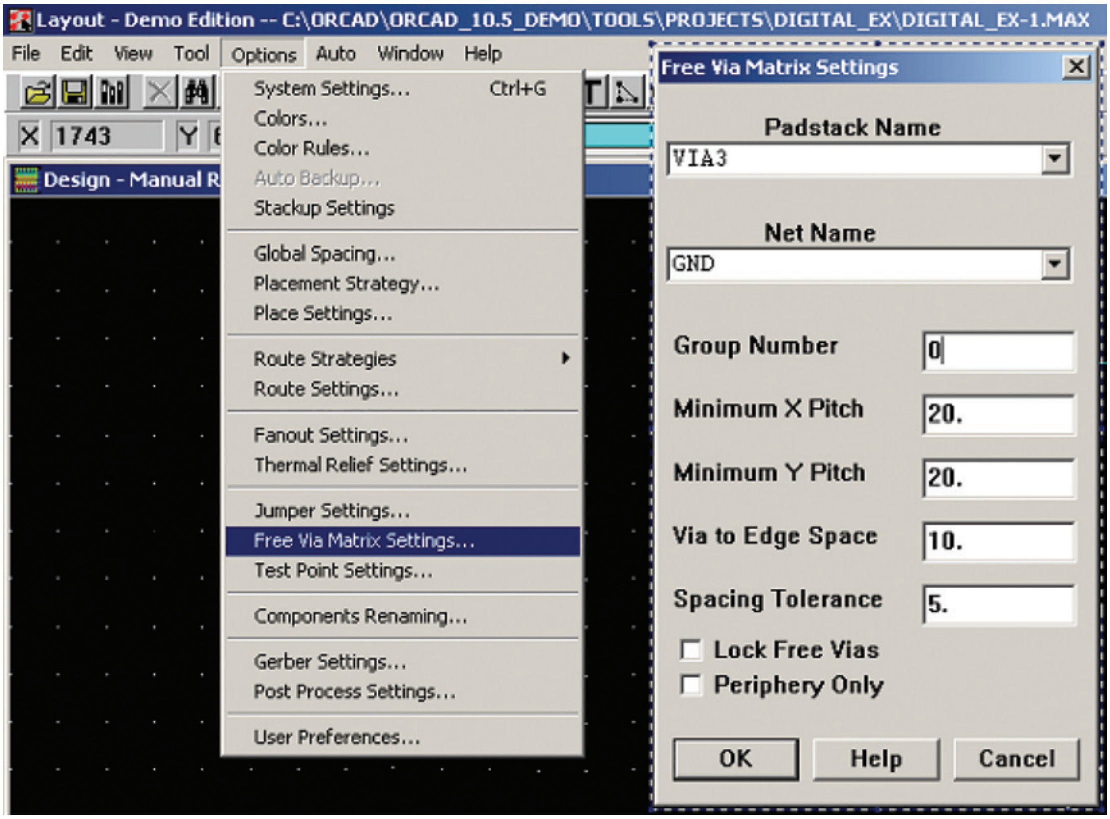
Y: 740.

☐ Locked

*Figure 9-128 The **Add Free Via** dialog box.*

Choose the **Add/Edit Route Mode** routing tool and draw a selection box inside the footprint of U2 as shown in Fig. 9-130. To draw the box left click and hold in one corner; drag to and release in the opposite corner. Finally select **Auto** → **Place** → **Free Via Matrix** from the menu bar. Layout will place as many vias within the boundary of the selection box as it can without violating any rules.

If the free vias are not placed in exactly the right spot you can move them using one of the manual routing tools. Figure 9-131(a) shows the results of placing a free via matrix and moving (slightly) the vias to the required locations (the drill layer and GND layers were selected sequentially to show the holes).


Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\DIGITAL_EX\DIGITAL_EX-1.MAX
File
Edit
View
Tool
Options
Auto
Window
Help
X 1743
Y
Design - Manual R
System Settings... Ctrl+G
Colors...
Color Rules...
Auto Backup...
Stackup Settings
Global Spacing...
Placement Strategy...
Place Settings...
Route Strategies
Route Settings...
Fanout Settings...
Thermal Relief Settings...
Jumper Settings...
Free Via Matrix Settings...
Test Point Settings...
Components Renaming...
Gerber Settings...
Post Process Settings...
User Preferences...
Free Via Matrix Settings
OK
Help
Cancel

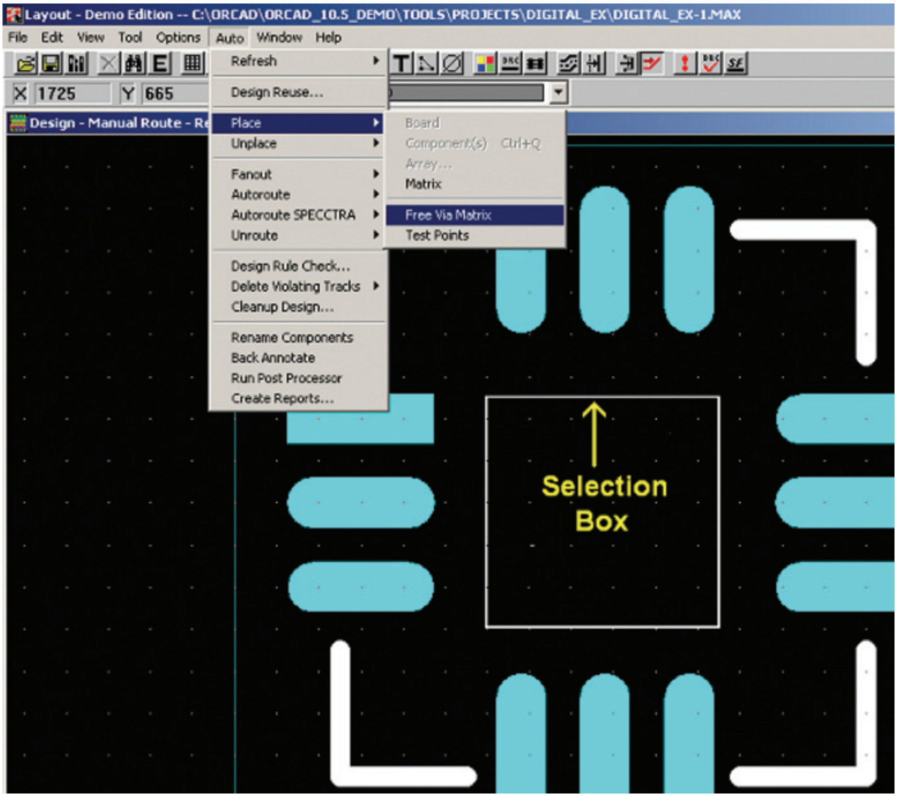
Padstack Name: VIA3
Net Name: GND
Group Number: 0
Minimum X Pitch: 20.
Minimum Y Pitch: 20.
Via to Edge Space: 10.
Spacing Tolerance: 5.
☐ Lock Free Vias
☐ Periphery Only

Figure 9-129 Setting up a free via matrix.

The next step is to place a copper area over the vias. **To place the copper heat spreader** select the Obstacle tool, right click, and select New from the pop-up. In the Edit Obstacle dialog box select Copper area as the obstacle type, 5 as the width, TOP as the obstacle layer, and GND as the net attachment. Click OK. Draw a box around the free vias to define the outline of the heat spreader. Once the last corner is placed, right click, and select Finish from the pop-up. The heat spreader is shown in Fig. 9-131(b).

Click the DRC button to check for errors. Since no fanouts were performed you will get “No connection to plane” errors, which you can ignore for the moment. If you get errors related to the free via location or spacing or the obstacle spacing, use the manual routing tools to move the vias and the Obstacle tool to resize the obstacle (you may have to make the obstacle grid smaller—such as 1 mil—to fix the errors).

In order for a good thermal connection to occur between the package and the heat spreader an opening needs to be made in the soldermask. **To make an opening in the soldermask** select the Obstacle tool, right click and select New from the pop-up, right click again and select Properties to display the Edit Obstacle dialog box. In the Edit Obstacle dialog box select


Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\DIGITAL_EX\DIGITAL_EX-1.MAX
File
Edit
View
Tool
Options
Auto
Window
Help
Design - Manual Route - Re
Refresh
Design Reuse...
Place
Unplace
Fanout
Autoroute
Autoroute SPECCTRA
Unroute
Design Rule Check...
Delete Violating Tracks
Cleanup Design...
Rename Components
Back Annotate
Run Post Processor
Create Reports...
Board
Component(s) Ctrl+Q
Array...
Matrix
Free Via Matrix
Test Points
Selection Box

X 1725 Y 665

Figure 9-130 Placing a free via matrix.

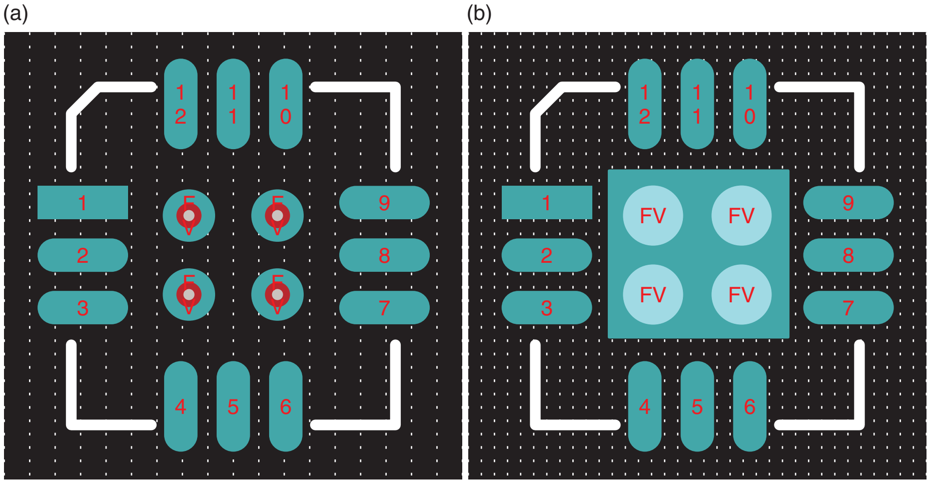

(a)
(b)
12
11
10
1
2
3
9
8
7
4
5
6
FV
FV
FV
FV

Figure 9-131 Construction of a heat spreader. (a) Placement of the heat pipes. (b) Placement of the copper area obstacle.

Copper area as the obstacle type, 5 as the width, SMTOP as the obstacle layer, and “-” as the net attachment. Click OK. Draw a box on top of the heat spreader. If the thermal bond will be made by soldering, repeat the above steps with a new copper area obstacle except specify the obstacle layer as SPTOP.

The next step is to fan out the board. Select VIA2 for the fanouts by selecting VIA2 from the Default Via: list in the Fanout Settings dialog box (Options → Fanout Settings…). Enable the GND and PWR nets (from the Nets spreadsheet) and then select Fanout → Board from the Auto menu.

Determining critical trace length of transmission lines

Since the controlled impedance traces are critical they will be routed next. The first step is to determine which traces need to be handled as transmission lines and which ones do not. As mentioned above the digital-to-fiber interface IC, FO-TX (U2), was modeled after the Analog Devices ADN2530. In the data sheet the digital signal lines going to the part and the modulation signals leaving the part (going to the laser diode) are to be handled as transmission lines. The digital control lines going to U2 do not have to be handled as transmission lines. The only traces left to consider are the ones related to the crystal oscillator and the NAND gates.

The literature states that the propagation time, PT, should be less than one-half of the rise time, RT (or fall time, FT), that is PT <½RT. If possible it is better yet if PT <¼RT (see Chap. 6 for more details). So we need to calculate PT for this board layout and lookup RT and FT for the oscillator and the NAND gates. Since the crystal is a fictional part here, let us assume that RT = FT = pulse width = ¼ the total period of a 66-MHz square wave. Under that assumption RT = 3.8 ns for the oscillator. The typical RT for ALS family logic is 1.9 ns.

The critical maximum length can be calculated using Eq. 1,

$$\text{Length}_{\text{trace}} < \frac{\text{RT}}{k \cdot t_{\text{PD}}}, \tag{1}$$

where $\text{Length}_{\text{trace}}$ is the maximum allowed trace length in inches, RT is the signal rise time in ps, k is the safety factor ($k = 2$ minimum), and t_{PD} is the propagation delay of the board material in ps/in.

The propagation delay for the surface microstrip (see Table 6-6 in Chap. 6) is

$$t_{\text{PD}} = 85\sqrt{0.457\varepsilon_r + 0.67}\ \text{ps/in.}, \tag{2}$$

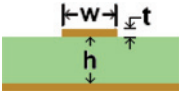
using $\varepsilon_r = 4.2$ for FR4, $t_{\text{PD}} = 137$ ps/in., and the critical trace lengths are given in Table 9-13 for various values of k. As indicated, there is no way that the ADN2530 traces can be treated other than as transmission lines but as long as none of the other traces are longer than 3.5 in. they do not have to be treated as transmission lines. Note that we are neglecting the length of the cables leaving the board through connector J1, but that is beyond the scope of the example.

		Maximum Length$_{trace}$ (in.)		
	RT (ns)	**k = 2**	**k = 3**	**k = 4**
66 MHz OSC	3.8	13.9	9.26	6.95
ALS logic	1.9	6.95	4.63	3.47
ADN2530	0.026	0.095	0.063	0.048

Table 9-13 Maximum safe trace lengths

Routing controlled impedance traces

The objective is to design surface microstrip transmission lines with a characteristic impedance of $Z_0 = 50\ \Omega$. Using the design equations from Chap. 6 (repeated here in Eq. 3) the width of the trace is calculated as



$$w = 7.47h \cdot e^{\left(\frac{-Z_0\sqrt{\varepsilon_r + 1.41}}{k}\right)} - 1.25t, \tag{3}$$

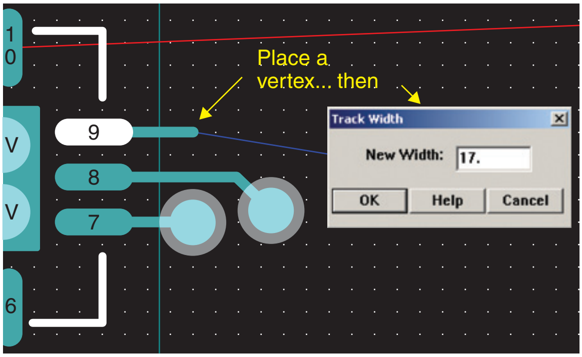
where, from Fig. 9-124, $t = 1.35$ mils (1 oz copper), $h = 10$ mils, $k = 87$ for $15 < w < 25$ mils (most references use this number—87 is used here), $k = 79$ for $5 < w < 15$ mils (Montrose offers this option), $Z_0 = 50\ \Omega$ (the design goal), and the desired trace width in mils $w = 17.5$ mils (17 mils $= 50.9\ \Omega$).

To specify the width of a net, open the **Nets** spreadsheet. The first step is to set the minimum and maximum widths allowed in the **Nets** spreadsheet. Use the intertool communications capability to find the net. Go to the schematic in Capture and select the net. Go back to the **Nets** spreadsheet in Layout; the net will be highlighted. Double click the net name to display the **Edit Net** dialog box. Set the trace widths as shown in Table 9-14 (you can set the colors to your preference). With these settings the traces will be 6 mils by default (good for the small surface-mount pads), but anywhere from 6 to 20 mils is allowed (which is needed for the 17-mil transmission lines).

		Width			Routing
Net name	**Color**	**Min**	**Con**	**Max**	**enabled**
N190204	🟥	6	6	20	Yes
N190208	🟦	6	6	20	Yes
N190234	🟦	6	6	20	Yes
N190238	🟥	6	6	20	Yes

Table 9-14 Net route settings from the nets spread sheet

Next the transmission lines are routed manually. Choose the **Add/Edit Route Mode** routing tool. Select a net on U2 at a point close to the pad to begin routing (see Fig. 9-132). Place a vertex just outside the place outline by left clicking once (this allows a short thermal relief



New Width: 17.

Figure 9-132 Routing a transmission line.

during reflow but is too short to interfere with the trace impedance). Right click and select Change Width from the pop-up (or hit W on the keyboard). Change the width to 17 mils and click OK. Continue routing the rest of the trace.

Begin the second trace starting at U2 and continue the trace to the laser diode. Figure 9-133 shows the completed transmission line. Note that, because of the pin-out of the component and the lead spacing of the diode, the lengths of the traces may not be equal (which is recommended in the data sheet). You can use the dimension tool (Tool → Dimension → New...) to measure the traces and use a little trigonometry to determine the complete trace lengths. If one trace needs to be longer you can zigzag back and forth to make the trace longer (see Chap. 6 concerning acute and 90° corners on high-frequency traces) or move the components accordingly. In this example the top trace was about 50 mils longer, so LD1 was moved down to make the lower trace longer, bringing the difference in lengths to within about 0.7 mils. The transmission lines running between the microprocessor (U1) and U2 are completed using the same procedure. Once the transmission lines have been routed, disable and lock the nets.

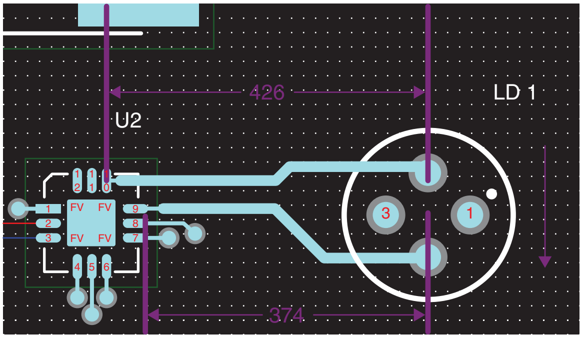


Figure 9-133 The completed transmission line.

Moated ground areas for clock circuits

The oscillator is routed next. In many applications a moated ground plane around the clock circuitry is recommended to prevent stray ground currents from affecting other circuits. Before adding the moated ground area around the oscillator, the traces should be routed so that the size of the required ground area is known. Begin by enabling all of the nets associated with the clock circuitry (if necessary use Capture and the Nets spreadsheet in Layout to identify the nets as described above). Route the traces manually or automatically using the route box (see design Example 1 on how to use the route box). Figure 9-134 shows the routed clock traces (along with the moat, which is described below).

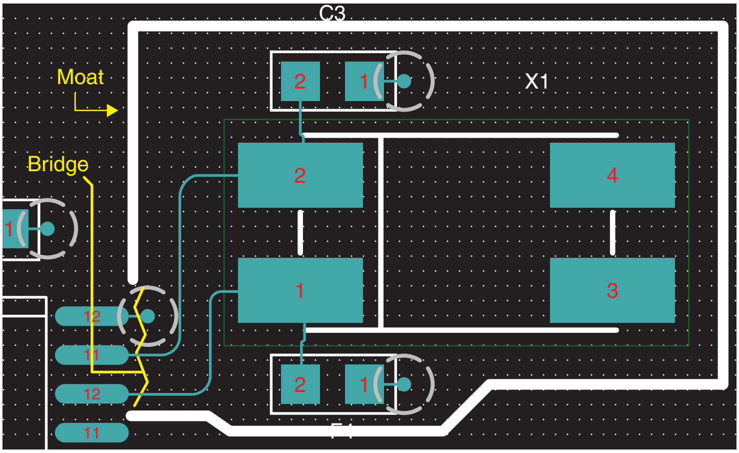


Figure 9-134 Clock circuitry routing and moated ground.

Routing curved traces

Notice that the traces between the crystal and U1 are curved. While they are not necessary, the curved corners are used here as a demonstration. **To route curved traces** choose one of the manual routing tools, right click, and select Curve Corners from the pop-up (see Fig. 9-135). Routing is conducted with curved corners as with other corner types (although it has a slightly different feel to it). **To revert back to regular corners** right click and select one of the other corner types.

The clock crystal, X1, has four pins on the package, but electrically it uses only two pins. The floating pins X1.3 and X1.4 can be left floating or can be routed to ground. **To connect the floating pins to the ground plane** the pins need to be modified. Choose the Pin tool, select the pin, right click, and select Properties... from the pop-up. Use the Modify Connections selection box (Fig. 9-136) and select the GND net. Click OK. This is performed for both pin X1.3 and pin X1.4.

Hit the Refresh button (!) to update the rat's nest (make sure the GND net is enabled). Later a ground will be poured on the top layer and X1.3 and X1.4 will automatically have fanouts to

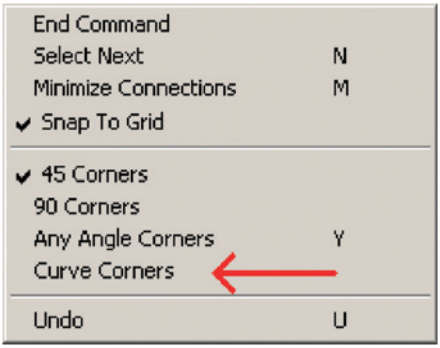
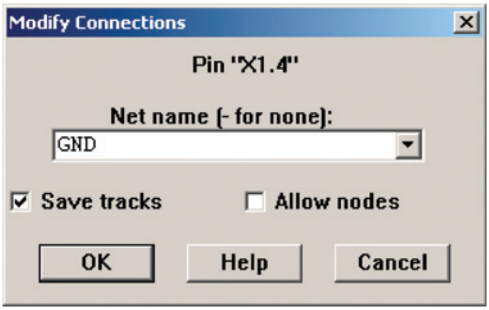


Figure 9-135 Changing to/from curved corners.



Pin "X1.4"

Net name (- for none): GND

☑ Save tracks ☐ Allow nodes

Figure 9-136 Connecting a floating pin to the ground plane.

the poured ground plane. Occasionally the DRC does not recognize the connection between the floating pins that are forced to ground and a poured ground. The solution is to fanout X1.3 and X1.4 with vias (the copper pour will be poured over the vias later).

Fanout X1.3 and X1.4 manually using one of the manual routing tools. Select the net leading from a pad route a trace away from the pad (about 100 mils), and click once to add a vertex. Right click and select Add Free Via. A regular via could also be used but when the ground plane is poured later a thermal relief is not desired on the via since the pad will have its own thermal reliefs (remember that VIA3 was set up earlier for Flood Planes/Pours).

The next step is to etch a moat into the GND plane around the clock circuitry (see Fig. 9-134). **To etch a moat into a plane layer** choose the Obstacle tool, right click and select New from the pop-up, right click again and select Properties... to display the Edit Obstacle dialog box. Select Free Track as the Obstacle Type, set the Width to 20 (or however wide you want the moat to be), select GND as the Obstacle Layer, and select "-" (none) for the Net Attachment. Click OK and draw the moat around the clock circuitry as shown in Fig. 9-134. Make sure to leave a "bridge" attached to the main ground plane. The bridge should be wide enough to include the ground pin and the area under the clock traces on U1. The local ground area under the clock circuitry is required to be attached electrically to the rest of the ground system but the moat is used to "corral" the ground currents back to the ground pin on the IC. Ground areas (and moats) will be placed on the top and bottom layers, and ground stitching will be used on all ground planes, but before that is performed, the rest of the board needs to be routed.

Disable and lock all routed traces. Enable the remaining unrouted nets and set the routing grid to 25 mils. Autoroute the board (Auto → Autoroute → Board). Figure 9-137 shows the result. A significant number of vias have been used and many of the traces have wandered around due to poor usage of the gates (as assigned on the schematic). By swapping gate A and gate C the routing distances and number of vias can be reduced.

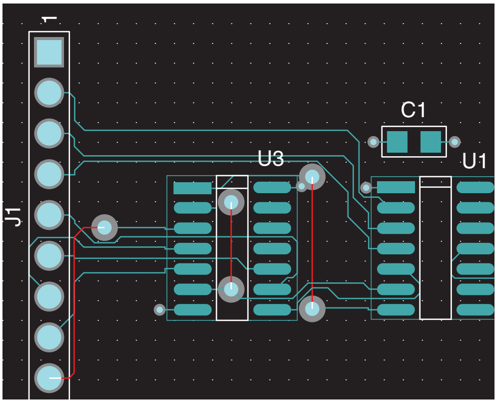


Figure 9-137 Bad routing caused by poor gate usage.

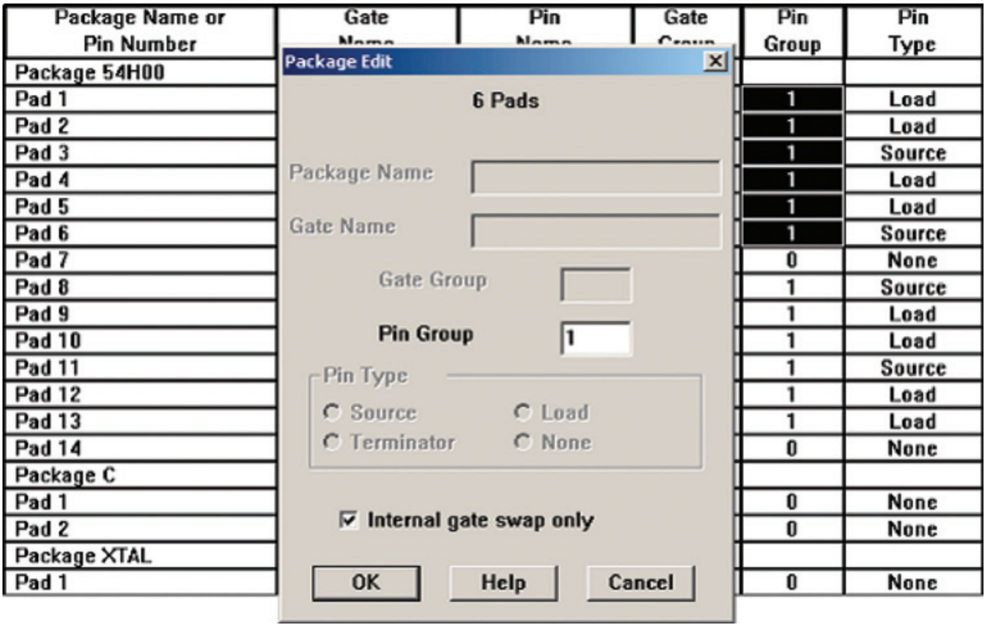
Gate and pin swapping

There are two methods that can be used to swap gates and pins. The first (and easiest) is to swap the gates (or pins on a gate) on the schematic page and run an ECO to Layout; this is also the safest way. The second method is to swap pins in Layout and back annotate to Capture to update the schematic. With the second method gates are swapped by swapping each of the pins associated with the gate(s). Gate-by-gate swapping is available in the Layout Plus version and SPECCTRA but is not discussed here.

The second method described above will be demonstrated here. Before doing the swap save the design (or save as a new .MAX file) so that the preswap design can be recovered if something goes wrong.

The first task is to unroute the gates. Make sure all gate nets are enabled and that all other nets are disabled and locked. As an added precaution the DRC/route box can be used to isolate the area to be unrouted. If using the DRC/route box, change the size of the box (select View → Zoom DRC Box and then drag a box with the "Z" cursor) to include only the gates (U3) and the applicable pins of U1. Unroute the traces by selecting Auto → Unroute → DRC/Route Box from the menu.

In order to swap pins the pins need to be swappable. **To verify that pins are swappable or to make pins swappable** choose the Component tool and, using Ctrl + left click, select U3. Open the Packages spreadsheet, select the desired pins from the Pin Group column, right click, and select Properties from the pop-up (see Fig. 9-138). Enter any integer number greater than 0 (zero) to enable pin swapping for those pins. You can restrict which gates and pins are swappable by selecting different integers for each swappable group. For example, if you enter a “1” for pins on gates A and C, and a “2” for B and D, you cannot swap pins or gates between A and D, but you can swap between A and C (or between B and D).



Package Name or Pin Number	Pin Group	Pin Type
Package 54H00		
Pad 1	1	Load
Pad 2	1	Load
Pad 3	1	Source
Pad 4	1	Load
Pad 5	1	Load
Pad 6	1	Source
Pad 7	0	None
Pad 8	1	Source
Pad 9	1	Load
Pad 10	1	Load
Pad 11	1	Source
Pad 12	1	Load
Pad 13	1	Load
Pad 14	0	None
Package C		
Pad 1	0	None
Pad 2	0	None
Package XTAL		
Pad 1	0	None

Package Edit

6 Pads

Package Name

Gate Name

Gate Group

Pin Group: 1

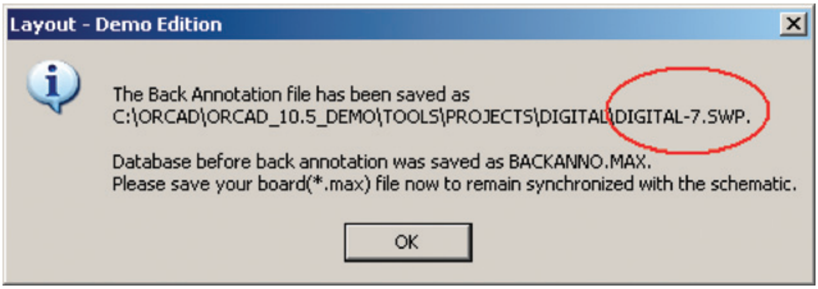
Pin Type
○ Source ○ Load
○ Terminator ○ None

☑ Internal gate swap only

Figure 9-138 Setting pin/gate swappability.

Once the pins are swappable the gates can be swapped pin by pin. To swap gate A for gate C swap pins as follows: 3 ↔ 8, 2 ↔ 10, and 1 ↔ 9. Select the Pin tool, . Ctrl + left click to select pin 3, right click, and select Swap from the pop-up. At the very bottom of the window Layout instructs you to “Select second gate/pin for swap;” click pin 8. You will get the warning: “Unable to validate pin swap (cannot be back-annotated) Continue?” Click Yes because this is true only under certain circumstances (see the Note below). Swap the remaining pins (2 ↔ 10 and 1 ↔ 9) using the same procedure.

The next step is to **back annotate the swap information to Capture**. Select Back Annotate from the Auto menu. At the back annotation information box (see Fig. 9-139) make certain to take note of the swap file name *before* you click OK as you will need to find the file again in Capture.



The Back Annotation file has been saved as
C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\DIGITAL\DIGITAL-7.SWP.

Database before back annotation was saved as BACKANNO.MAX.
Please save your board(*.max) file now to remain synchronized with the schematic.

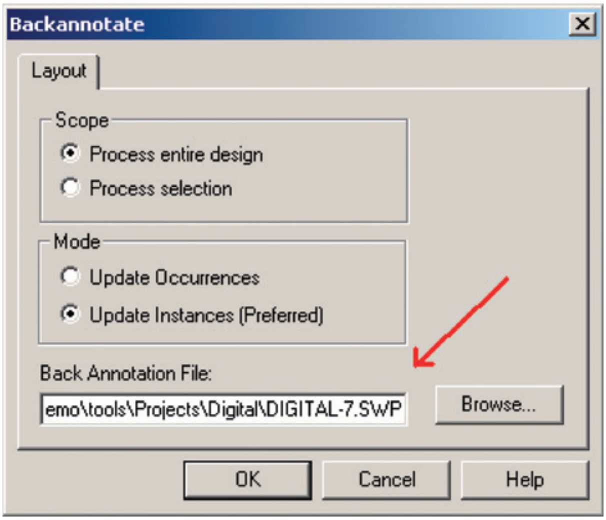
Figure 9-139 Take note of the swap file name and location.

To back annotate the swap to the schematic in Capture return to the Project Manager and select the **Design** icon. From the **Tools** menu select **Back Annotate**. In the **Back annotate** dialog box (Fig. 9-140), **Browse** for the correct .SWP file (Fig. 9-139) and click **OK**.

Figure 9-141 shows the schematic after the pin swapping and back annotation operations.

Note

- *You can only do one pin/gate swap evolution per back annotation without performing an AutoECO from Capture to Layout. If you need to do more swaps, perform an AutoECO first (even if nothing else has changed) to keep the schematic and the PCB synchronized. After that you can swap the next set of pins/gates and then do another back annotation.*



Scope
● Process entire design
○ Process selection

Mode
○ Update Occurrences
● Update Instances (Preferred)

Back Annotation File: emo\tools\Projects\Digital\DIGITAL-7.SWP

Figure 9-140 Select the .SWP file in Capture.

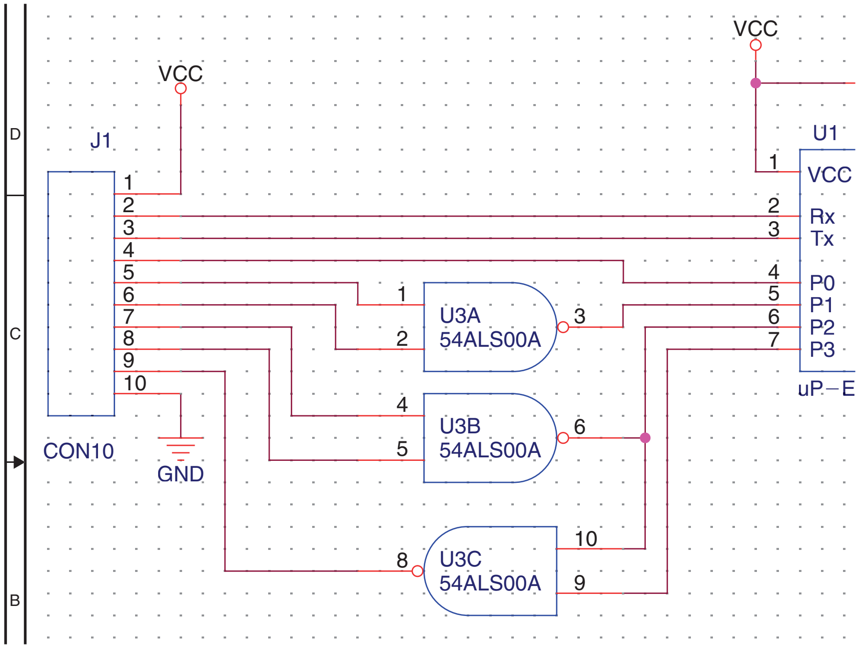


Figure 9-141 Schematic after the gate/pin swap is performed.

Now the board can be rerouted. To use the autorouter again, the “done” flag will need to cleared. Go to Options → Route Strategies → Route Passes..., double click the Enable column, and clear the “done” flag. After autorouting the board, use the Edit Segment Mode tool to clean up traces and then perform a DRC. Check the Statistics spreadsheet to make sure no nets have been missed. Disable and lock all traces and save the design.

Stitching a ground plane with the free via matrix

The next step is to apply a ground plane to the top of the board (using copper pour) and moat a local ground area around the clock circuitry using an anti-copper obstacle. The first step is to draw the anti-copper obstacle before pouring the copper ground, otherwise it will be difficult to see where the moat is on the GND layer. Set the detail grid (Options → Systems Settings...) to 1 or 2 mils so that the anti-copper obstacle (top layer) can be easily placed exactly over the free track (on negative GND plane).

The anti-copper obstacle is a closed polygon, and the copper is removed from inside the boundaries. To make the top anti-copper the same size as the (negative) free track on the ground plane, the anti-copper polygon will be an outline of the free track (see Fig. 9-142). To draw the anti-copper obstacle choose the Obstacle tool, right click and select New from the pop-up, right click again and select Properties. In the Edit Obstacle dialog box select Anti-Copper as the Obstacle Type, set the Width to 1, select TOP as the Obstacle Layer, and leave the Net Attachment as none. Outline the moat area as shown in Fig. 9-142. Once the last vertex is placed, right click and select Finish.

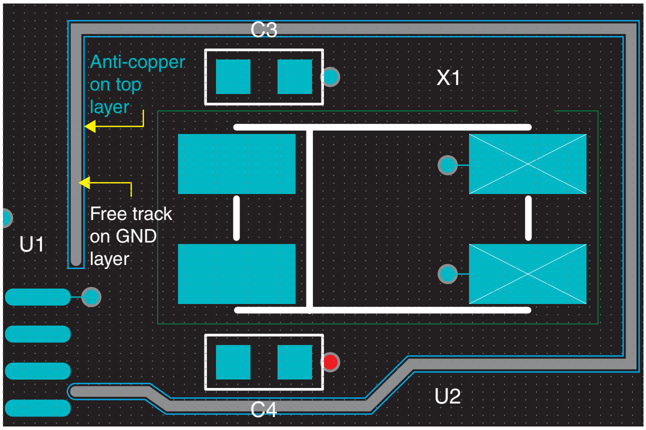

C3
Anti-copper on top layer
X1
Free track on GND layer
U1
U2
C4

Figure 9-142 Moat on TOP defined with anti-copper obstacle.

The copper pour can now be placed on the top layer. Choose the Obstacle tool, right click and select **New** from the pop-up, right click again and select **Properties.** In the **Edit Obstacle** dialog box select **Copper Pour** as the Obstacle Type, set the Width to 10, set the Clearance to 20 (or tighter if preferred), select **TOP** as the Obstacle Layer, and select **GND** as the Net Attachment. Follow the board outline to pour copper over the entire board. The finished copper pour is shown in Fig. 9-143. Note that the gray line (etched copper) on the GND plane

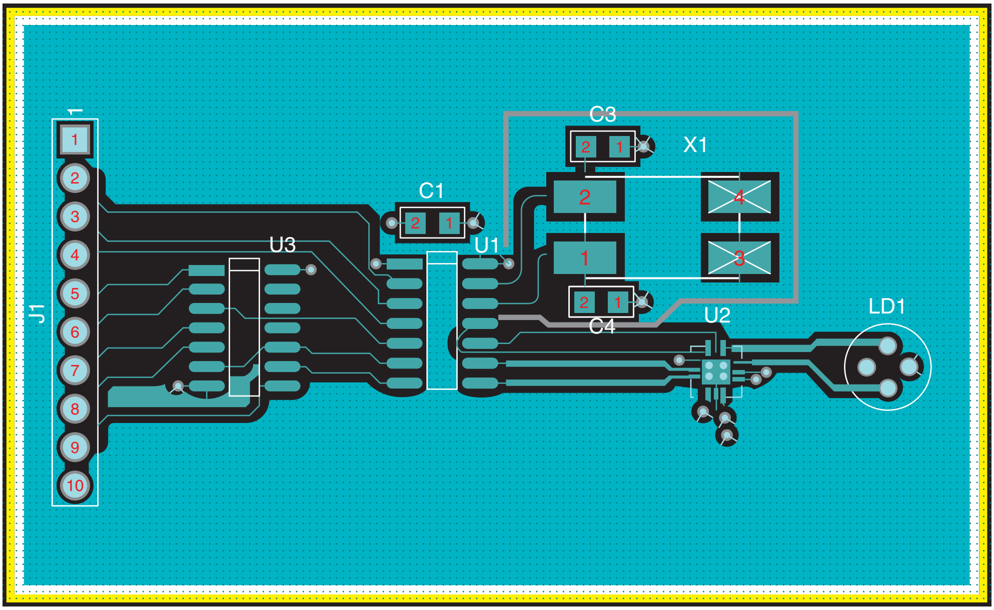

1
1
2
3
4
5
6
7
8
9
10
J1
U3
C1
2
1
U1
C3
2
1
X1
2
4
1
3
2
1
C4
U2
LD1

Figure 9-143 The finished copper pour on the TOP layer.

is visible through the moat etched into the top copper. You can repeat this process for the bottom layer as well except that the moat is not required in this case.

The last step that will be described is ground plane stitching. Using the procedure described above for placing a free via matrix under the heat spreader, set the via spacing to 100 or 200 mils. Draw a large box over the entire board and, after a moment, you should see a field of free vias tightly connecting the top, bottom, and inner ground planes as shown in Fig. 9-144. Perform a final DRC and delete any free vias that cause errors or that have violated the ground moat.

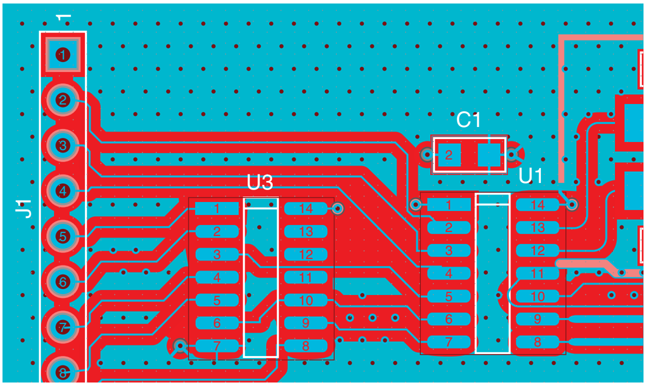


Figure 9-144 A densely stitched ground plane.

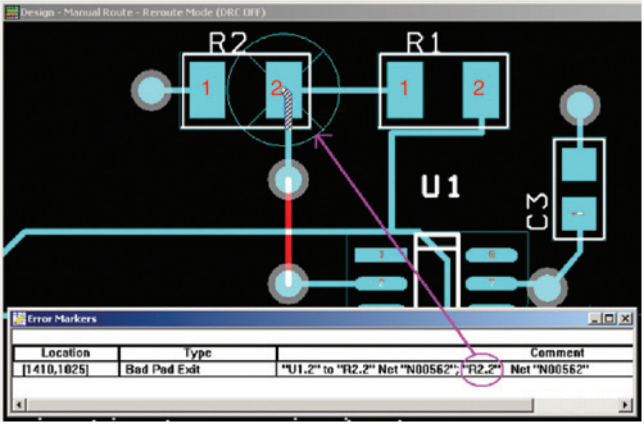
Miscellaneous Items

The following discusses items that were not specifically demonstrated in the design examples.

Fixing bad pad exits

A common error is the Bad Pad Exit. If you get this error it is most likely because a trace is leaving a pad off-center or the trace has a jog in it inside a pad. Figure 9-145 shows an example of a bad pad exit (colors enhanced) and the corresponding Error Markers spreadsheet. The problem is the jog inside in R2 pad 2.

To fix a bad pad exit error use the manual Add/Edit Route Mode tool, select the trace using Ctrl + left click, then right click, and select Unroute Segment to unroute the trace from the center of the pad up to the via (make sure to get all of the segments). Manually reroute the trace starting at R2.2. Click on the net near R2.2 to start routing. Run the trace straight down, leaving the pad at its center (and perpendicular). Click the mouse just past the R2's silk-screen outline to place a vertex. Right click and select Finish. This will force the jog to be placed outside of the pad as shown in Fig. 9-146.



Location	Type	Comment
[1410,1025]	Bad Pad Exit	"U1.2" to "R2.2" Net "N00562"; "R2.2" Net "N00562"

Figure 9-145 **Bad Pad Exit** error.

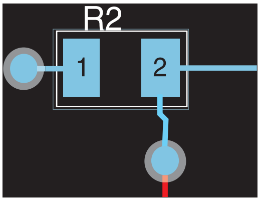


Figure 9-146 Corrected pad exit.

Design cache—cleanup, replace, update

Every project in Capture contains a design cache. At some point during the design process you will likely be confronted with having to modify the design cache (whether directly or indirectly) and will need to use one of the three cache commands. The differences between the commands are subtle and (usually) fairly benign. Under certain circumstances, however, using the wrong command can cause unintended results. The purpose of this section is to explain the differences between the commands and explain when and how to use them.

The design cache contains a list of all the parts that you have added to the design and the parts that are included with the template that was used (if any) when the project was originally set up. You can view the design cache in the Project Manager (shown in Fig. 9-147). Parts in the design cache are also listed in the **Place Part** dropdown list on the menu bar, which makes it easy to find and place additional parts.

When you place a part you are actually using a local copy of the part from the library, not the part itself. However, Capture maintains a link between the copy and the original part. If the part in the library is changed or if the local copy is changed the Capture "librarian" will know about it and break the link.

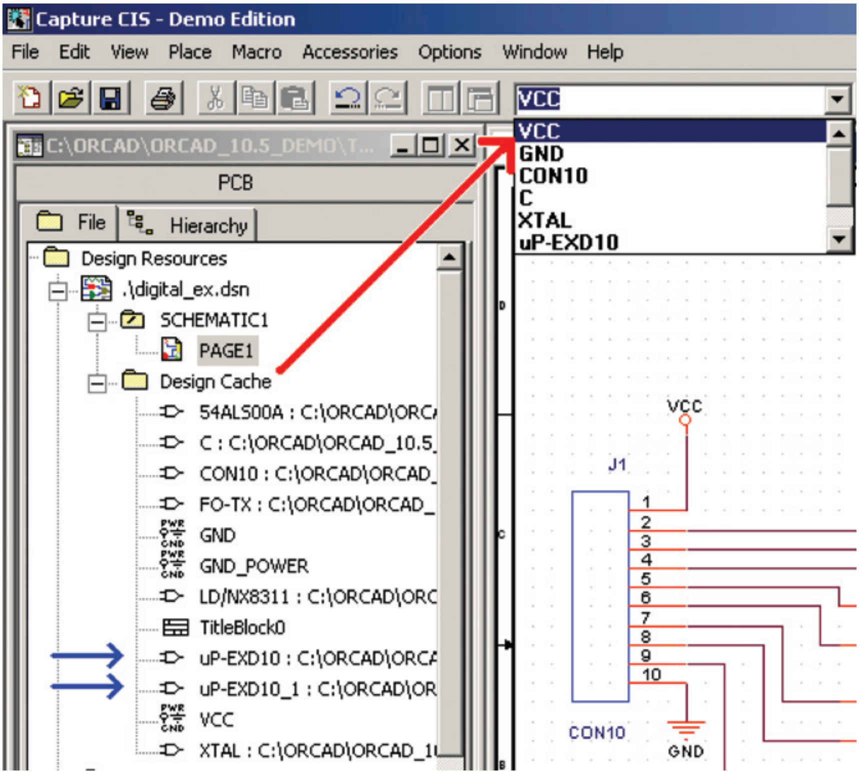

Capture CIS - Demo Edition
File
Edit
View
Place
Macro
Accessories
Options
Window
Help
VCC
VCC
GND
CON10
C
XTAL
uP-EXD10
C:\ORCAD\ORCAD_10.5_DEMO\T...
PCB
File
Hierarchy
Design Resources
.\digital_ex.dsn
SCHEMATIC1
PAGE1
Design Cache
54ALS00A : C:\ORCAD\ORC
C : C:\ORCAD\ORCAD_10.5
CON10 : C:\ORCAD\ORCAD
FO-TX : C:\ORCAD\ORCAD
GND
GND_POWER
LD/NX8311 : C:\ORCAD\ORC
TitleBlock0
uP-EXD10 : C:\ORCAD\ORC
uP-EXD10_1 : C:\ORCAD\OR
VCC
XTAL : C:\ORCAD\ORCAD_1
VCC
J1
1
2
3
4
5
6
7
8
9
10
CON10
GND

Figure 9-147 The design cache contains a list of placed parts.

If you change a part on the schematic page the modified part is given a new name (an extension such as "_1" is added to the name as indicated by the blue arrows in Fig. 9-147) and it is no longer linked to the original part library. If you change your mind and need to get the original part back you can have Capture replace the part in the design cache folder with the original library part. **To replace a part in the design cache**, select the part in the Project Manager's design cache folder and select Replace Cache from the Design menu. You can also use the Replace Cache function to exchange an existing part with one from the same or a different library (for example exchanging a 74LS00 NAND gate for a 74ACT00 NAND gate or exchanging an op-amp that was from the Linear Technologies library with one from the Analog Devices library—or vice versa).

If the original part in the library is changed and then you try to place another one of those parts in your design, the Capture librarian will catch the difference and recommend that you update your design cache with the new part (but you do not have to if you do not want to). **To update the project's design cache** select the part in the Project Manager's Design Cache folder, right click, and select Update Cache from the pop-up. The Capture librarian will not catch differences between a modified library part and a modified project part because the names will be different (by "_1" or similar) and the Capture librarian will ignore it.

If you have performed a back annotation from Layout the part in your design will likely contain properties that you will not want to lose. When you change a part with the Replace Cache command you can retain those properties with the Preserve Schematic Part Properties option in the Replace Cache dialog box.

If you have placed and deleted parts several times the design cache will fill up with unused parts. While this does not really cause a problem it can be cumbersome to continue looking through unused parts while looking for the one of interest. **To clean out unused parts from the design cache** select the Design Cache folder in the Project Manager window, right click, and select Cleanup Cache from the pop-up.

Adding test points

There are two approaches to adding test points to a board. The first approach is to add a test point "part" to the schematic, assign a single-pad footprint to it, and place it on the board in Layout as you would any other part. The second approach is to have Layout place a test point on a net. This type of test point can be back annotated to Capture (to the Net Properties spreadsheet), but it will not be displayed on the schematic. The latter approach is described here to place a surface-type test point that is inline with the trace, shown in Fig. 9-148.

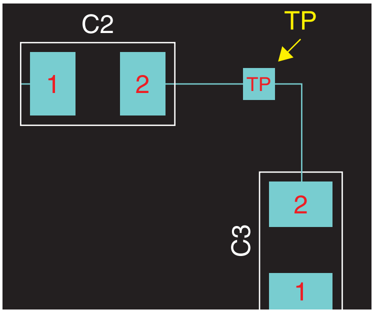
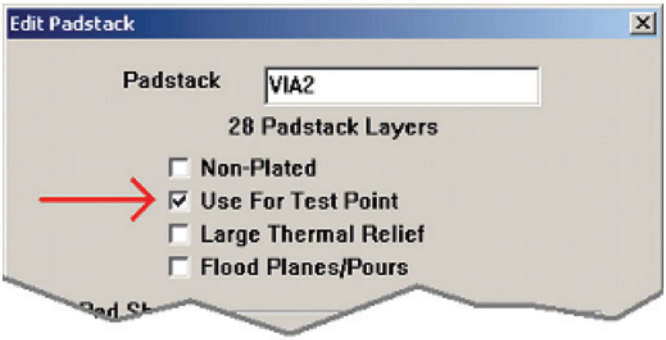


Figure 9-148 A test point placed on a net in Layout.

The first step is to define a padstack that will be used as the test point. Open the Padstacks spreadsheet. You can use one of the unused vias or construct a custom padstack from scratch and save it in your UserLib.LLB (Figs. 9-149 and 9-150).

You can place a test point during manual routing or you can have Layout place all test points at once. To place a test point manually choose one of the manual routing tools. The test point can be added while routing the net (in which case the trace must contain at least one vertex) or after it has been completely routed. Select the desired net, right click, and select Add Test Point from the pop-up.

To have Layout automatically place test points the traces must be routed first. Then select Place → Test points from the Auto menu. Test points will be placed on all nets that were

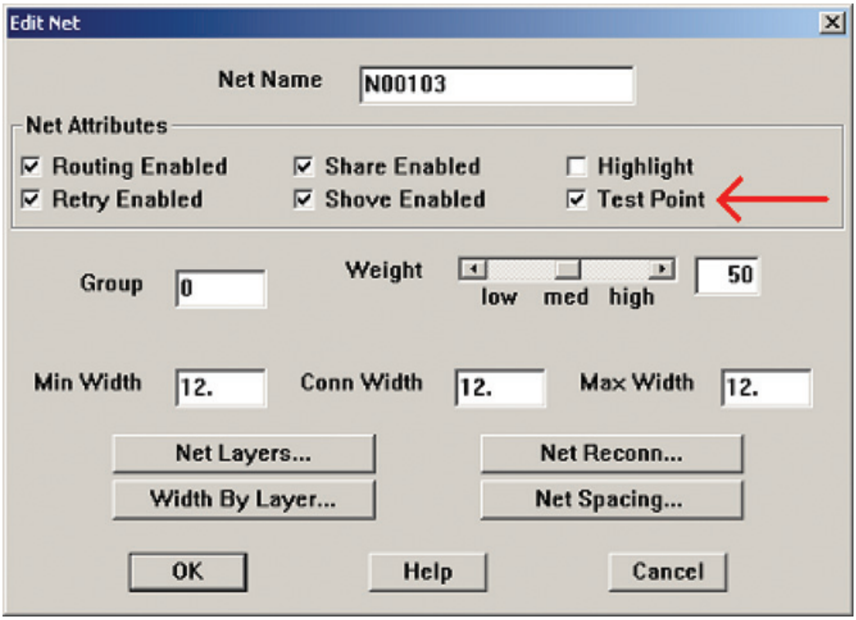


Padstack VIA2

28 Padstack Layers

☐ Non-Plated
☑ Use For Test Point
☐ Large Thermal Relief
☐ Flood Planes/Pours

Figure 9-149 Assigning a via as a test point.



Net Name N00103

Net Attributes

☑ Routing Enabled ☑ Share Enabled ☐ Highlight
☑ Retry Enabled ☑ Shove Enabled ☑ Test Point

Group 0

Weight (low, med, high) 50

Min Width 12. Conn Width 12. Max Width 12.

Figure 9-150 Assigning the test point property to a net.

assigned as test points and had test-point padstacks assigned to them. You can move or delete test points with the manual routing tools.

Types of AutoECOs

There are seven different types of ECOs that can be run. The correct ECO to run depends on what you want to update (components or nets); whether you want to add, delete, or update; and whether a back annotation has previously been performed from Layout to Capture (and how recently). Table 9-15 shows the general effects on components by the type of ECO, Table 9-16 shows the effects on nets (traces in Layout), and Table 9-17 explains the color scheme

MNL to MAX	AutoECO	Override attrs	Override coord	Override all	Add only	Add override
Components	Match schematic	Match schematic	Match schematic	Match schematic	Match schematic except deletes	Match schematic except deletes
Component properties except coordinates	No changes except additions	Match schematic	No changes except additions	Match schematic	No Changes except additions	Match schematic except deletes
Component coordinates	No changes except additions	No changes except additions	Match schematic	Match schematic	No Changes except additions	Match schematic except deletes
Placement	No changes except additions	No changes	Match schematic	Match schematic	No changes except additions	Match schematic except deletes

Table 9-15 Effects on components by ECO type

MNL to MAX	AutoECO	Override attrs	Override coord	Override all	Add only	Add override
Nets	Match schematic	Match schematic	Match schematic	Match schematic	Match schematic except deletes	Match schematic except deletes
Net properties	No changes except additions	Match schematic	No changes except additions	Match schematic	No changes except additions	Match schematic except deletes

Table 9-16 Effects on nets (Traces) by ECO type

Match schematic All existing data on the PCB in this category are made to match the schematic page, including additions and deletions.	**Match schematic except deletes** All existing data on the PCB in this category are made to match the schematic page, including additions, but not deletions.
No changes except new All existing data on the PCB in this category remain the same, except additions that are made from the schematic page.	**No changes** All data in this category of the PCB remains the same.

Table 9-17 ECO Effects legend

of the tables and explains the effects. The tables contain most of the information provided in the *Layout User's Guide* (Layug.pdf) but have been reorganized and abridged for readability. Effects on text and obstacles are omitted from the tables since they are never affected by ECOs, and the Net Attrs AutoECO was omitted because it is used to communicate information between printed circuit boards. For more information on AutoECOs see p. 35 of the Layug.pdf.

Making a custom Capture template

If you design a lot of projects that are similar to each other, setting up a project template in Capture can be a real time saver and can help eliminate errors by reusing known good project setups. Project templates can be used only when setting up a project through the Analog or Mixed A/D option from the New Project dialog box. However, since you can make a PCB design from either the Analog or Mixed A/D option or the PC Board Wizard option, you can still take advantage of creating your own Capture templates for PCB design projects.

To make a custom Capture project template start a new Analog or Mixed A/D project; set it up with power supply and ground symbols, connectors, or whatever you want; and then save it in the OrCAD/tools/Capture/templates/PSpice folder with the other templates. It will automatically be added to the templates list so that you can select it the next time you start a new project.

Making a custom Layout technology/template file

As with the Capture templates, if you design a lot of PCBs that are similar to each other, setting up a custom technology file (.TCH) in Layout can save a lot of time and can eliminate many manufacturing errors by reusing known good PCB setups.

To make a custom technology (.TCH), template (.TPL), or reusable PCB design (.MAX) file in Layout begin with a known good board design. Save the board design with the desired file extension (.TCH, .TPL, or .MAX) in the Layout Data folder or a folder of your choice. The new file will contain all the elements of the known good board including the layer stack-up, padstack definitions, board outlines, trace width and spacing, etc. You can save and reuse some, all, or none of the board elements (including the board outline and connectors). Delete unwanted elements by selecting them and deleting them. You will likely want to delete all nets except for maybe the ground and power nets. To delete nets open the Nets spreadsheet and select the nets to delete and hit the Delete key on the keyboard. You can leave the power and ground nets so that if you consistently reuse the Capture template with a specific Layout template you can preserve all ground and power net names and assignments to plane layers (which are also preserved with the layer stack-up). Save the modified file. Note: When you save nets with the template and then import ones with the same name from a new .MNL from Capture Layout will make two nets with duplicate names and will mark the imported one with a darker yellow color. Since they are really the same net you can delete the 'new' one with the darker yellow color if you have previously established a color scheme for the net.

The next time you start a new board, select your template file (whether a .TCH, a .TPL, or a .MAX) from the AutoECO dialog box instead of the usual default .TCH or 1bet_any.TCH.

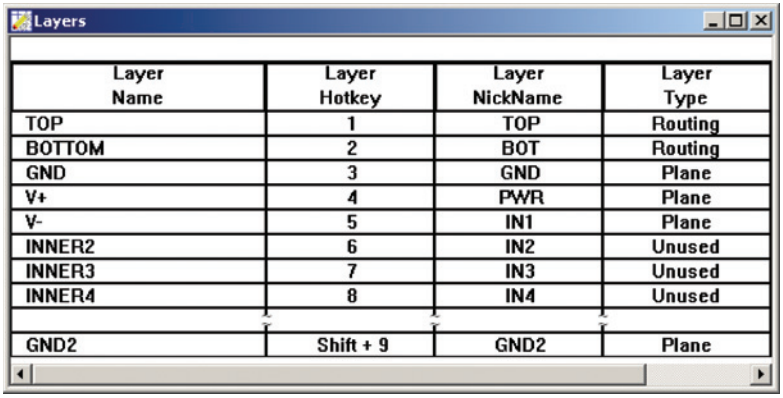
Using the Stackup Editor

The Stackup Editor is new to version 10.5. It can be invoked from the main Layout session frame to modify and rename existing technology and template files, or it can be invoked from an active board design to modify its layer properties. The Stackup Editor can be used to:

- add or delete routing and plane layers,
- change the order of the layer names,
- define the board technology type (cores or built up),
- specify core and prepreg properties (thickness and ε_r),
- specify copper layer properties (name, thickness, conductivity, etc.),
- specify solder paste sizes (relative to pad sizes),
- specify soldermask properties (wet/dry and ε_r),
- specify the overall board thickness,
- specify the board impedance (in ohms),
- specify via protection (none, tent, plug, cap), and
- specify a document layer in which to insert a stack-up drawing.

Using the Stackup Editor with an active board design

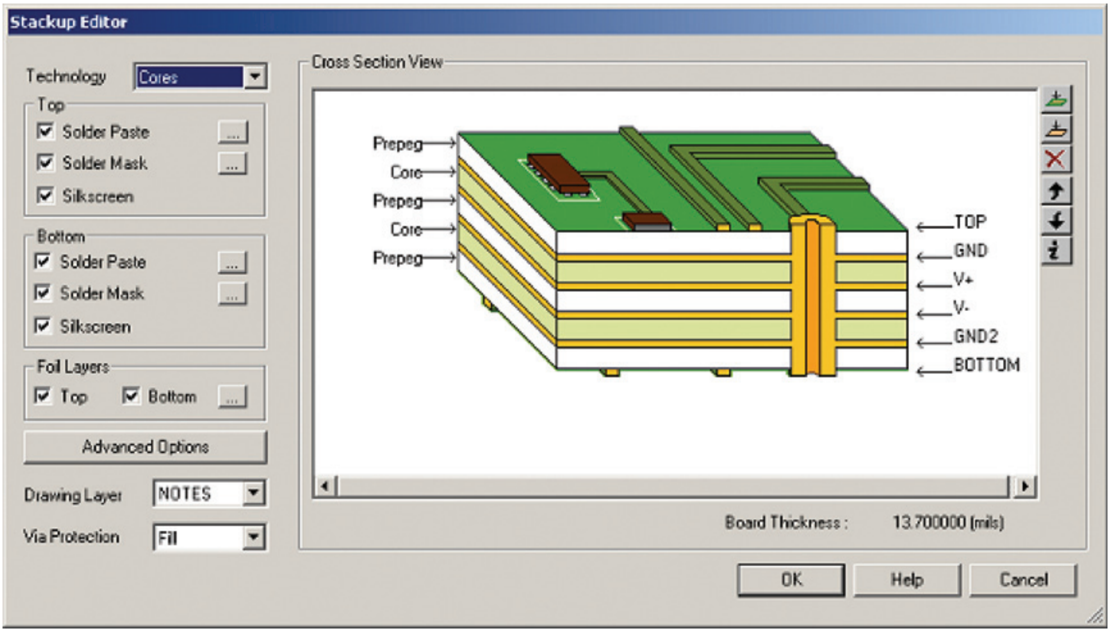
The Stackup Editor will be demonstrated by using it to modify the stack-up of the analog design example—Example 1. Recall from the analog design example that a second ground plane was added to the design by copying the existing GND plane and creating a new ground plane, GND2. As indicated in Fig. 9-151 the GND2 plane was placed at the very bottom of the **Layers** spreadsheet by default. The Stackup Editor will be used to move the GND2 layer (from the analog design example—Example 1) from the bottom of the **Layers** spreadsheet to its actual position in the stack-up.



Layer Name	Layer Hotkey	Layer NickName	Layer Type
TOP	1	TOP	Routing
BOTTOM	2	BOT	Routing
GND	3	GND	Plane
V+	4	PWR	Plane
V-	5	IN1	Plane
INNER2	6	IN2	Unused
INNER3	7	IN3	Unused
INNER4	8	IN4	Unused
GND2	Shift + 9	GND2	Plane

Figure 9-151 **Layers** spreadsheet before using the Stackup Editor.

To invoke the Stackup Editor from an active board design (.MAX file) select Stackup Settings from the Options menu. The Stackup Editor is shown in Fig. 9-152.


Stackup Editor

Technology: Cores

Top
☑ Solder Paste
☑ Solder Mask
☑ Silkscreen

Bottom
☑ Solder Paste
☑ Solder Mask
☑ Silkscreen

Foil Layers
☑ Top ☑ Bottom

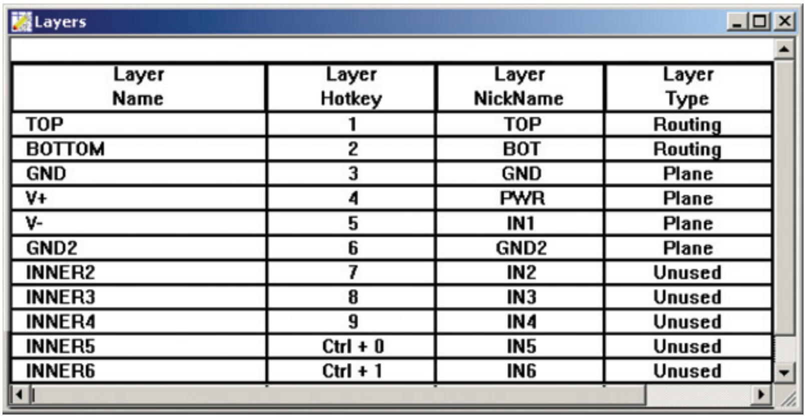
Drawing Layer: NOTES

Via Protection: Fill

Board Thickness : 13.700000 (mils)

Figure 9-152 Layer Stackup Editor.

To move layers up and down select the layer you want moved (left click once) and then use the move up/down arrow buttons, ↑ ↓ (see right-hand side of Fig. 9-152). Figure 9-153 shows the Layers spreadsheet in the active design after moving the GND2 layer around.


Layers

Layer Name	Layer Hotkey	Layer NickName	Layer Type
TOP	1	TOP	Routing
BOTTOM	2	BOT	Routing
GND	3	GND	Plane
V+	4	PWR	Plane
V-	5	IN1	Plane
GND2	6	GND2	Plane
INNER2	7	IN2	Unused
INNER3	8	IN3	Unused
INNER4	9	IN4	Unused
INNER5	Ctrl + 0	IN5	Unused
INNER6	Ctrl + 1	IN6	Unused

Figure 9-153 **Layers** spreadsheet after using the Stackup Editor.

Note

- *You cannot move the TOP or BOT layers around. When you click the **OK** button in the Stackup Editor the **Layers** spreadsheet will be updated with the new configuration (compare Fig. 9-151 to Fig. 9-153).*

You can also use the Stackup Editor to delete and add layers. **To delete a layer** select the layer you want deleted and press the Delete button, on the Stackup Editor toolbar. Deleting a layer with the Stackup Editor does not delete it from the Layers spreadsheet but only changes the layer type to Unused.

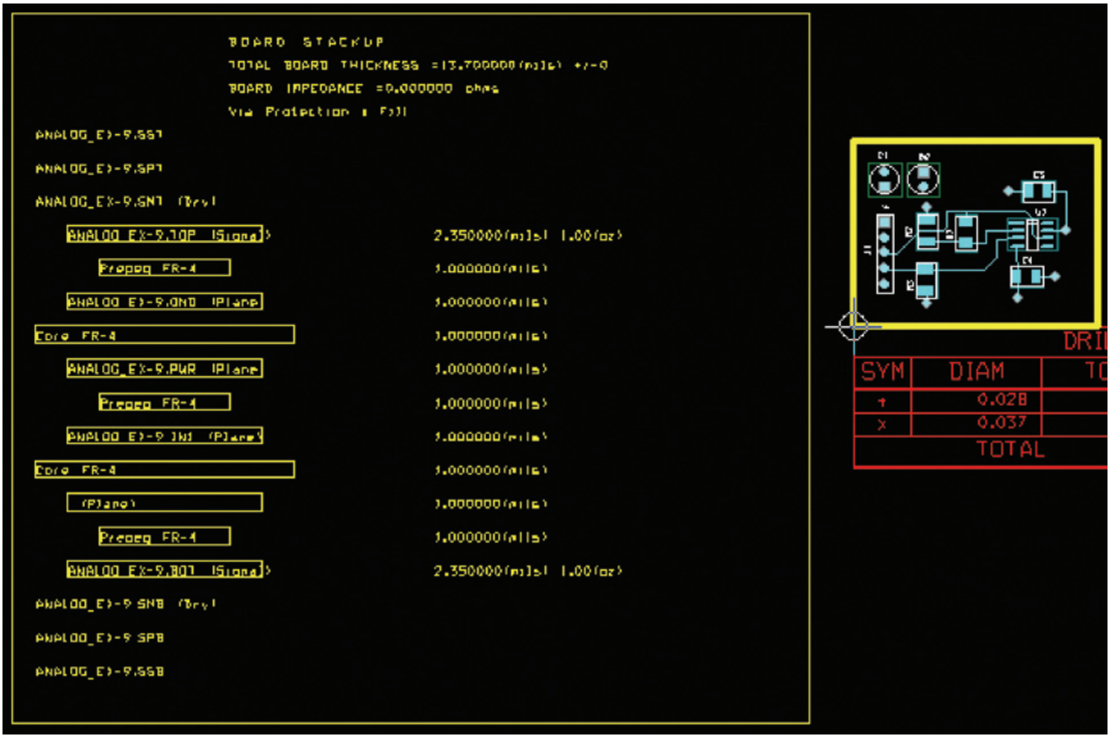
To add a routing layer press the Insert Layer button, . **To add a plane layer** press the Insert Plane button, . After you have added a layer you can change its properties.

To change the properties of a conductor or laminate layer select the conductor or laminate layer and press the Properties button, and use the dialog box to specify the layer's new properties.

You can add a stack-up drawing to the PCB design for engineering documentation and to aid the board manufacturer in fabricating the board. A stack-up drawing is shown next to a board design in Fig. 9-154. The stack-up information is saved with the file that is associated with the layer on which the stack-up drawing is placed. The stack-up drawing is automatically generated by the Stackup Editor, is inserted into the PCB design as a nonelectrical *component*, and is included with the postprocessed Gerber files as specified by the postprocess settings (see Submitting stack-up drawings with Gerber files). The stack-up drawing cannot be back annotated to Capture.

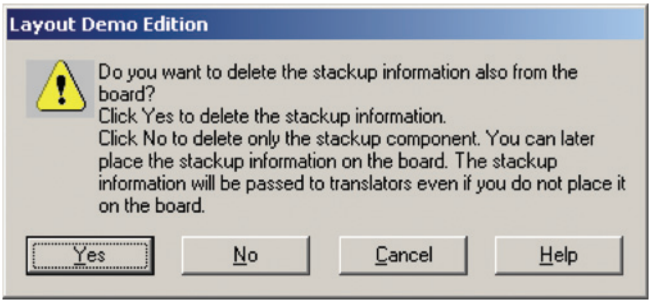
To add a stack-up drawing to a board design choose one of the document layers from the Drawing Layer dropdown list (see lower left corner of Fig. 9-152). When you click OK the stack-up drawing will be added to the board design. Note that you may have to zoom out to see it, and you have to have the document layer you selected visible. You can change the color of the stack-up drawing by changing the color of the layer to which it is assigned (click the Color Settings button on the toolbar).

To move the stack-up drawing select the Component tool and then left click and drag a selection box across the stack-up drawing to select it. Move the drawing to its new location and left click to place it. If you do not want the stack-up drawing to be visible you can either turn off the document layer on which it resides or delete the stack-up drawing. If you choose to delete the drawing you can delete it and the stack-up information or just delete the drawing. **To delete the stack-up drawing** select the Component tool and drag a box across the stack-up drawing to select it. Hit the Delete key on your keyboard. You will be asked if you want to delete just the drawing or both the drawing and the stack-up information from the board (see Fig. 9-155).



```
BOARD STACKUP
TOTAL BOARD THICKNESS =13.700000(mils) +/-0
BOARD IMPEDANCE =0.000000 ohms
Via Protection : Fill
ANALOG_EX-9.SST
ANALOG_EX-9.SPT
ANALOG_EX-9.SMT (Dry)
ANALOG_EX-9.TOP (Signal)        2.350000(mils) 1.00(oz)
Prepeg FR-4                     1.000000(mils)
ANALOG_EX-9.GND (Plane)         1.000000(mils)
Core FR-4                       1.000000(mils)
ANALOG_EX-9.PWR (Plane)         1.000000(mils)
Prepeg FR-4                     1.000000(mils)
ANALOG_EX-9.IN1 (Plane)         1.000000(mils)
Core FR-4                       1.000000(mils)
(Plane)                         1.000000(mils)
Prepeg FR-4                     1.000000(mils)
ANALOG_EX-9.BOT (Signal)        2.350000(mils) 1.00(oz)
ANALOG_EX-9.SMB (Dry)
ANALOG_EX-9.SPB
ANALOG_EX-9.SSB
```

Figure 9-154 The layer stack-up drawing object.



Layout Demo Edition

Do you want to delete the stackup information also from the board?
Click Yes to delete the stackup information.
Click No to delete only the stackup component. You can later place the stackup information on the board. The stackup information will be passed to translators even if you do not place it on the board.

Figure 9-155 Deleting the stack-up drawing and information (optional).

Using the Stackup Editor to set up a custom technology or template file

You can use the Stackup Editor to modify an existing technology or template file, or you can set up a new custom technology or template file by using an existing file as a starting block. **To make a new technology/template file with the Stackup Editor** invoke the Stackup Editor from the main Layout session window (not a design window) by selecting Define Stackup from the Tools menu. At the Create/Edit Stackup dialog box select a baseline stack-up by clicking the browse button, ... and selecting a .TCH or .TPL file. The Predefined Stackup text box will be automatically filled in when you select a file from the Open File dialog box and click OK. Click OK in the Create/Edit Stackup dialog box to display the Stackup Editor. Use the tools described above to modify the stack-up properties inherited from the baseline technology file. When the modifications are complete click the Save As... button to save the new technology file with a new name.

Note

- *If you click the **Save** button instead, the baseline technology file will be changed to the new settings, so make sure you press the right button if you do not want to modify the original file.*

Submitting stack-up drawings with Gerber files

To submit the layer stack-up information to a board manufacturer you can include it with the Gerber files. As described above the stack-up drawing is typically placed on a documentation layer. To include it with the Gerber files you must use one of the documentation layers that are included in the postprocess list. These include the assembly layers (*.AST and *.ASB) and the fabrication layer (*.FAB). Note that you can also use one of the other documentation layers (silk screen, etc.), but the assembly and fabrication layers are probably more appropriate. The target document layer is selected with the Drawing Layer dropdown list on the Stackup Editor (see lower left corner of Fig. 9-152). When you perform the postprocessing make sure that the layer containing the stack-up drawing is enabled. To enable that layer select Post Process Settings... from the Options menu and set Batch Enabled = Yes.

When you perform a DRC the stack-up drawing will produce an error because it is a component that is outside the board outline. You can ignore the error; open the Error Markers spreadsheet, select Place Spacing Error, right click, and select Mark as Good DRC from the pop-up menu.

Adding solder thieves

Adding solder thieves for SMDs that will be wave soldered is straightforward. Solder thieves are constructed from the copper areas on the TOP layer of the board behind the last set of leads on the IC with a soldermask opening over the pad to expose it to the solder. To allow adequate placement resolution you will need to set the detail grid to 1 mil. Select System Settings... from the Options menu and the Detail Grid [X,Y]: to 1 mil.

To place the solder pad select the Obstacle tool. Right click in the work space and select New, right click again, and select Properties. In the Edit Obstacle dialog box select Copper Area from the Obstacle Type list, set the Width to 1 mil, select TOP from the Obstacle Layer list, leave the Net Attachment as none, “-”. Draw a box of the correct size (same size as or slightly larger than the solder pads you are thieving from) in the correct location (see Fig. 5-3). Right click and select Finish from the pop-up when the box is completed.

To expose the copper area select the Obstacle tool, right click and select New, right click again and select Properties. In the Edit Obstacle dialog box select Copper Area from the Obstacle Type list, set the Width to 1 mil, select SMTOP from the Obstacle Layer list, leave the Net Attachment as none, "-". Draw a box over the pad that was drawn in the previous step. Right click and select Finish from the pop-up when the box is completed.

Printing a footprint catalog from a PCB design

You can print out a catalog of the footprints used in a PCB design. This gives you the opportunity to review the packages used in the design. The footprints are printed to scale so you can perform a "dry run" to make sure that all of the parts fit the footprints before you have the board fabricated. This is especially helpful if you (or someone else) had to make custom footprints and wanted to verify that they were made correctly. The directions for creating and printing a catalog are provided in Chap. 15 of the *Layout User's Guide* (search for Catalog Tool). The directions are very straightforward, so they will not be duplicated here.

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CHAPTER 10

Postprocessing and Board Fabrication

Postprocessing was briefly introduced in Chap. 2. In Chap. 10 we look at postprocessing in greater detail and show how to submit the Gerber files to an actual board house (Advanced Circuits).

The Circuit Design with OrCAD

Schematic design in Capture

As with the previous examples, we will use a simple circuit to minimize details and allow us to focus on the board layout. The circuit (shown in Fig. 10-1) consists of a six-pin PCB

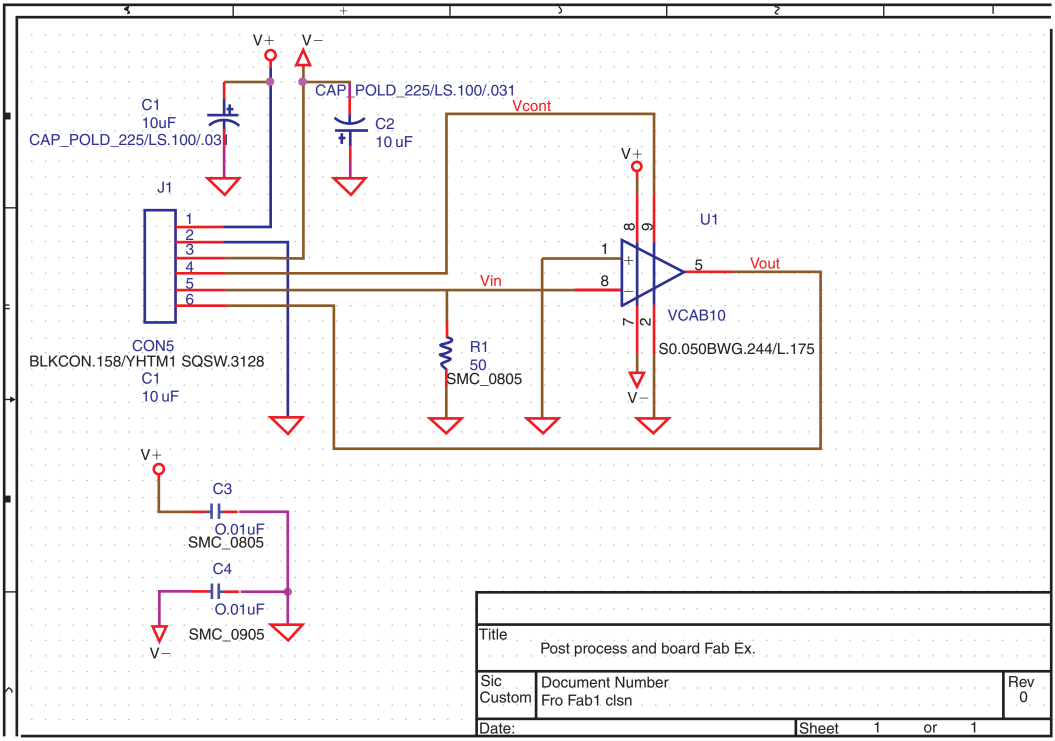
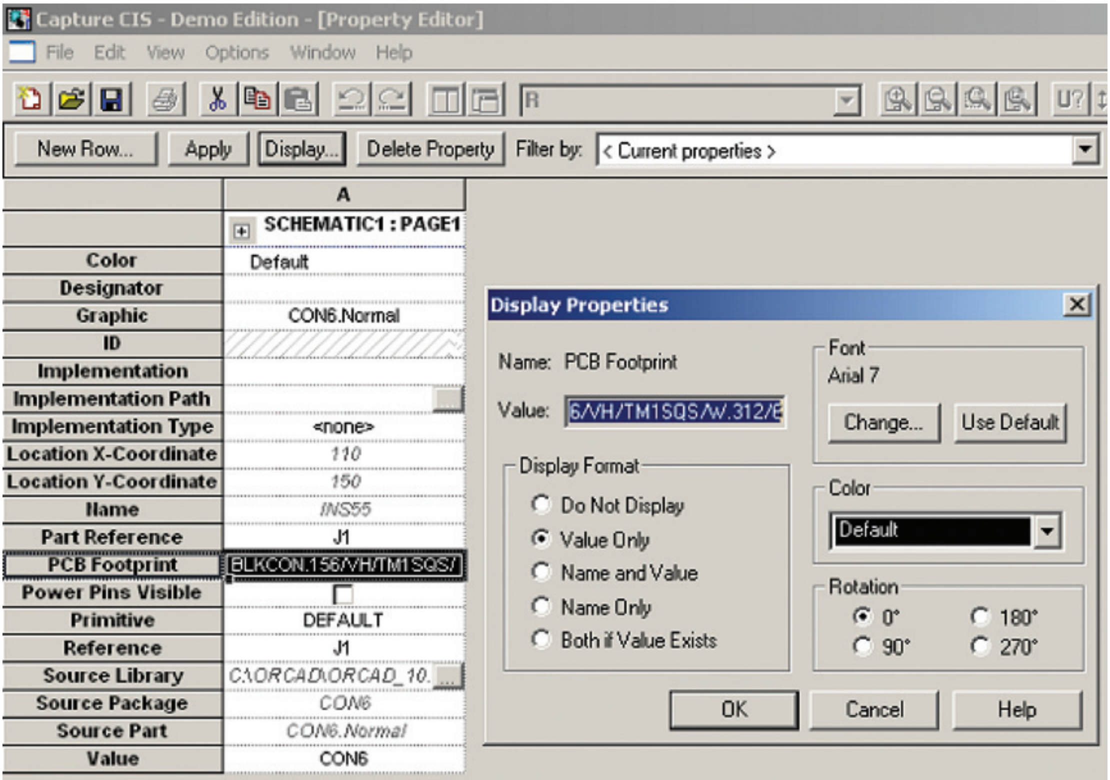

V+
V−
CAP_POLD_225/LS.100/.031
C1
10uF
CAP_POLD_225/LS.100/.031
C2
10 uF
Vcont
V+
J1
1
2
3
4
5
6
U1
8
6
1
+
5
Vout
Vin
8
−
7
2
VCAB10
CON5
BLKCON.158/YHTM1 SQSW.3128
C1
10 uF
R1
50
SMC_0805
S0.050BWG.244/L.175
V−
V+
C3
0.01uF
SMC_0805
C4
0.01uF
V−
SMC_0905
Title
Post process and board Fab Ex.
Sic
Custom
Document Number
Fro Fab1 clsn
Rev
0
Date:
Sheet
1
or
1

Figure 10-1 The circuit design for fabrication.

connector (J1), bulk decoupling capacitors (C1 and C2), a variable gain amplifier (U1), bypass capacitors (C3 and C4), and a terminating resistor (R1). Once we move the design to Layout we will add different types of mounting holes so that when we postprocess the design you will be able to see the different types of drill files that are generated. The circuit contains only 7 parts so that if you are using the Demo version the total part count is only 10 (including the mounting holes), so that the design can be saved and postprocessed.

The footprints for each of the components are shown on the schematic. **To display component information on the schematic** double click the part to display the Property Editor spreadsheet (see Fig. 10-2). Select the cell (row or column) that contains the information you want displayed. Click the Display... button at the top of the spreadsheet to show the Display Properties dialog box. Select one of the display formats and click OK. Click the Apply button at the top of the spreadsheet and close the spreadsheet.

Once the schematic is completed, generate a Layout netlist (.MNL file) as described in Chap. 9.



Filter by: < Current properties >

	A
	SCHEMATIC1 : PAGE1
Color	Default
Designator	
Graphic	CON6.Normal
ID	
Implementation	
Implementation Path	
Implementation Type	<none>
Location X-Coordinate	110
Location Y-Coordinate	150
Name	INS55
Part Reference	J1
PCB Footprint	BLKCON.156/VH/TM1SQS/
Power Pins Visible	☐
Primitive	DEFAULT
Reference	J1
Source Library	C:\ORCAD\ORCAD_10.
Source Package	CON6
Source Part	CON6.Normal
Value	CON6

Name: PCB Footprint

Value: 6/VH/TM1SQS/W.312/E

Font: Arial 7

Display Format
○ Do Not Display
● Value Only
○ Name and Value
○ Name Only
○ Both if Value Exists

Color: Default

Rotation
● 0°
○ 180°
○ 90°
○ 270°

Figure 10-2 Use the **Property Editor** to display part information on the schematic.

The board design with Layout

Figure 10-3 shows the routed board. The board properties are as follows:

- Layers: TOP, BOTTOM, GND, POWER.
- Strategy file: STD.SF.
- Technology file: 1bet_any.TCH.
- Vias: default VIA1 for all routing and fanouts.

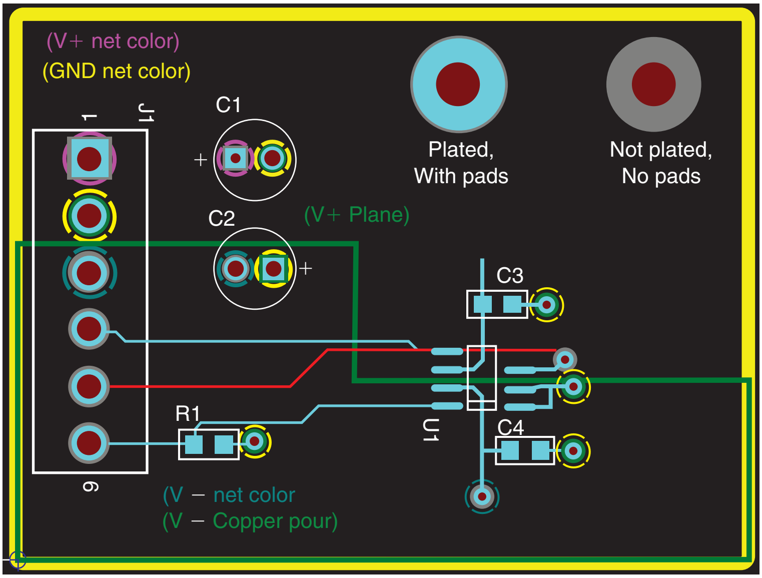


Figure 10-3 The routed board.

Both V+ and V− power are on the POWER plane. V+ is the primary net (magenta colored); V− is the secondary net (dark blue colored) and is placed on the power plane with a copper pour, which covers the bottom half of the board.

An actual board would be laid out more compactly and could be laid out on a single- or double-sided board. The extra layers were used here so that several layer (Gerber) files can be processed and submitted to the board house. The excessive space was used for ease of visibility. To look at the layout in greater detail see the design file (BRDFAB1B-2.MAX), which is on the CD included with this book.

There are two types of mounting holes on this board. The first has copper pads on the top and bottom layers and a plated through-hole. This type of mounting hole is included in the thruhole.TAP file since it is fabricated the same way and at the same time as all the other plated through-holes. The second has no pads and is not plated. It is made separately from the other holes and requires an extra manufacturing step. The postprocessor generates a separate drill file for it called thruhole.NPT.

In most cases there is no need for nonplated holes and since they require an extra processing step many board houses charge extra for them. The nonplated hole is included here as an example only.

Postprocessing the design with Layout

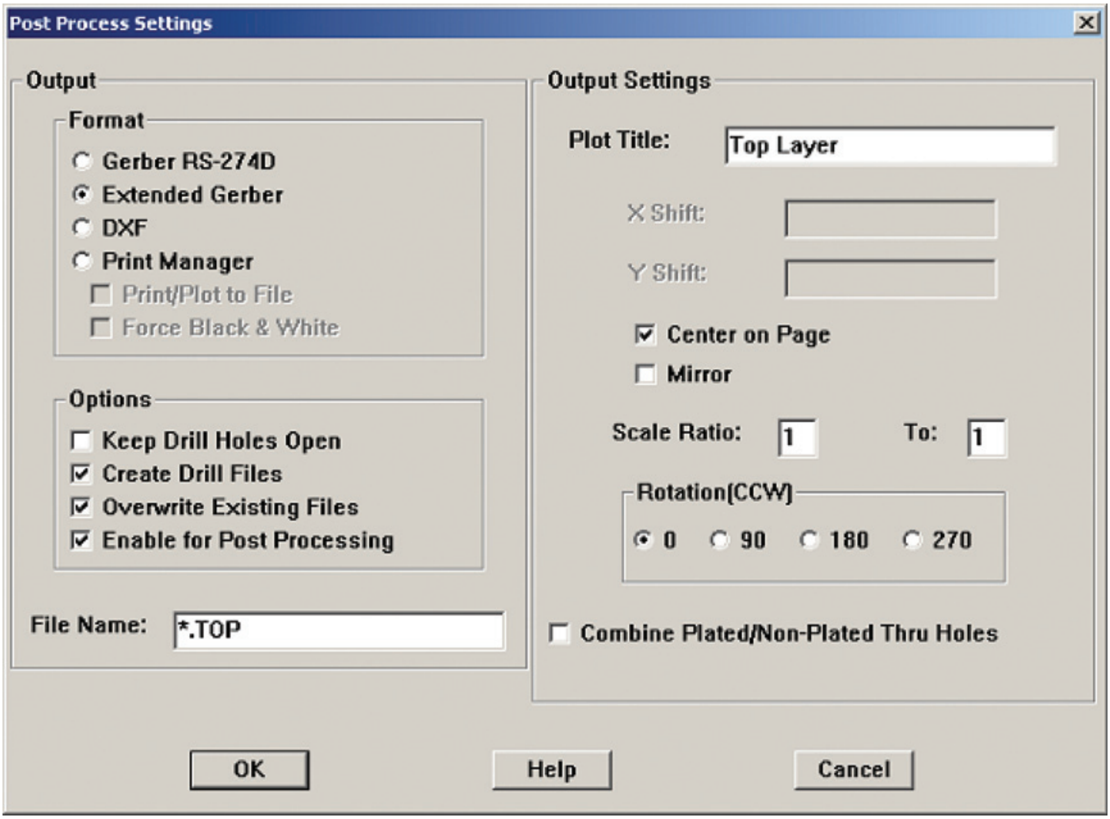
Before you set up and run the postprocessor it is suggested that you save a copy of the board design (.MAX) in a dedicated subfolder. The reason is that the postprocessor creates many files (Gerber files) and places them in the same folder as the .MAX file. If your .MAX file is in the same folder as the schematic and any PSpice files, it can become difficult to find the Gerber files. It is also a good idea to run a DRC one last time before running the postprocessor to catch any last-minute problems.

The first step to fabricating the board is to set up the postprocessor. **To set up the postprocessor** choose Post Process Settings... from the Options menu to display the Post Process Settings spreadsheet. The layers enabled for this example are shown in Fig. 10-4, and disabled layers are not included in the figure.

Plot output File Name	Batch Enabled	Device	Shift	Plot Title
*.TOP	Yes	EXTENDED GERBER	No shift	Top Layer
*.BOT	Yes	EXTENDED GERBER	No shift	Top Layer
*.GND	Yes	EXTENDED GERBER	No shift	Top Layer
*.PWR	Yes	EXTENDED GERBER	No shift	Top Layer
*.SMT	Yes	EXTENDED GERBER	No shift	Top Layer
*.SMB	Yes	EXTENDED GERBER	No shift	Top Layer
*.SST	Yes	EXTENDED GERBER	No shift	Top Layer
*.DRD	Yes	EXTENDED GERBER	No shift	Top Layer

Figure 10-4 ***Post Process Settings*** *spreadsheet.*

To enable or disable a layer for processing double click the layer to display the Post Process Settings dialog box (see Fig. 10-5). Check-mark the Enable for Post Processing box in the Options section of the dialog box. The dialog box also allows you to select the type of Gerber format. The Extended format is another name for RS-274X, which has superseded RS-274D. When you select a board manufacturer, find out which format they prefer. We will use the Extended format for this example.



Output

Format
○ Gerber RS-274D
● Extended Gerber
○ DXF
○ Print Manager
☐ Print/Plot to File
☐ Force Black & White

Options
☐ Keep Drill Holes Open
☑ Create Drill Files
☑ Overwrite Existing Files
☑ Enable for Post Processing

File Name: *.TOP

Output Settings

Plot Title: Top Layer
X Shift:
Y Shift:
☑ Center on Page
☐ Mirror
Scale Ratio: 1 To: 1

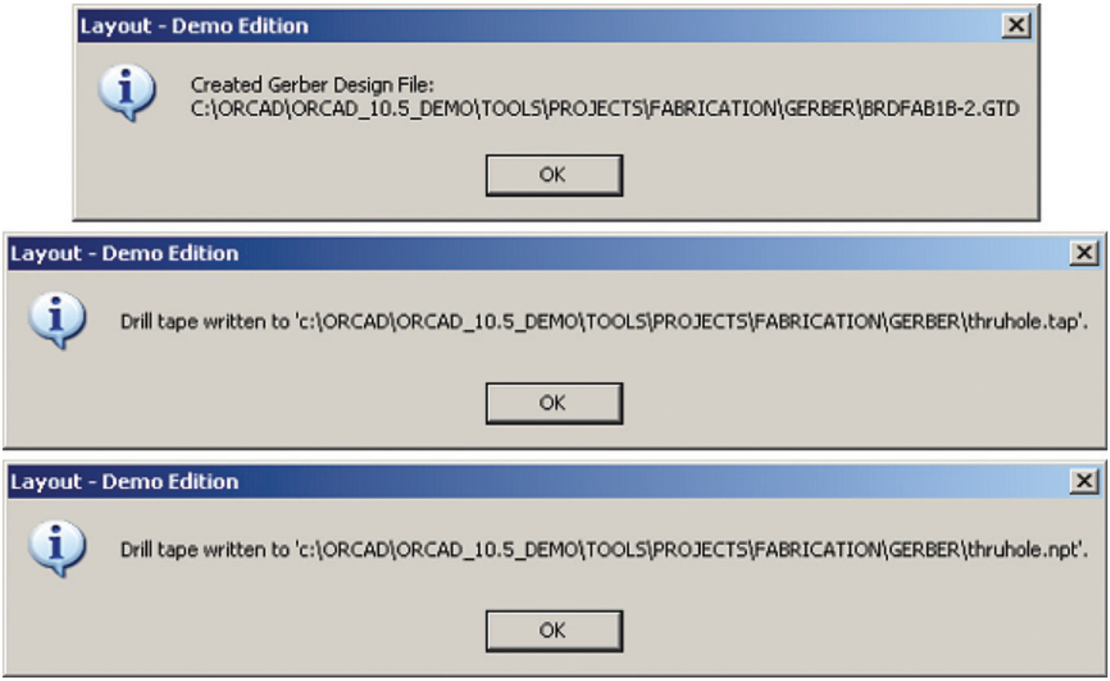
Rotation(CCW)
● 0 ○ 90 ○ 180 ○ 270

☐ Combine Plated/Non-Plated Thru Holes

*Figure 10-5 Use the **Post Process Settings** dialog box to enable/disable layers for processing.*

Once the postprocessor has been set up, the next step is to run the postprocessor. **To run the postprocessor** choose Run Post Processor from the Auto menu. The postprocessor will display several information boxes as shown in Fig, 10-6 and the postprocessor report as shown in Fig. 10-7.

Next use Windows Explorer to locate the Gerber files. An example of the generated Gerber files is shown in Fig. 10-8.

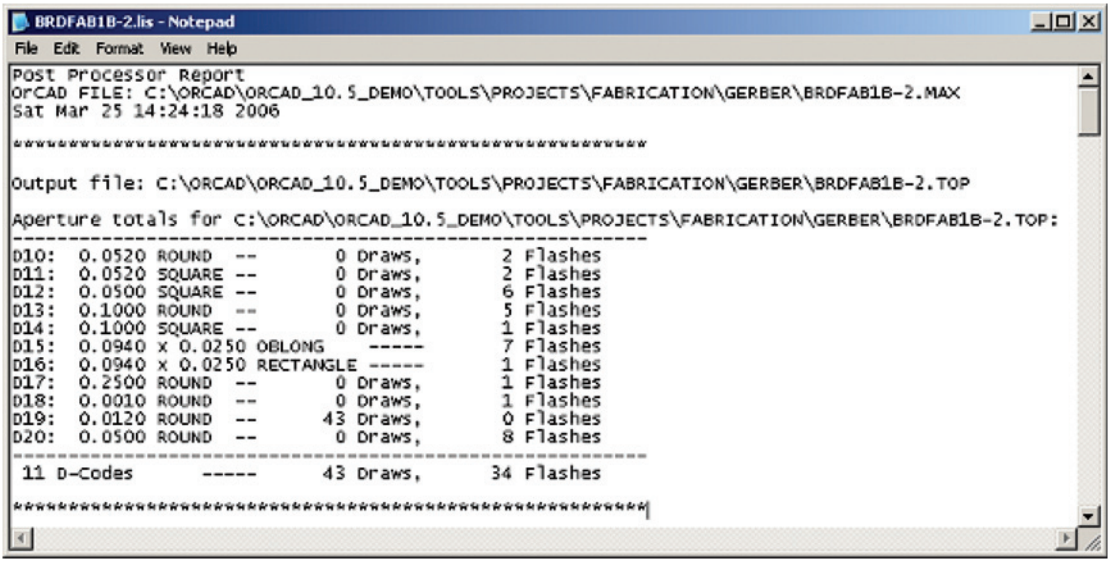


Created Gerber Design File:
C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\FABRICATION\GERBER\BRDFAB1B-2.GTD

Drill tape written to 'c:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\FABRICATION\GERBER\thruhole.tap'.

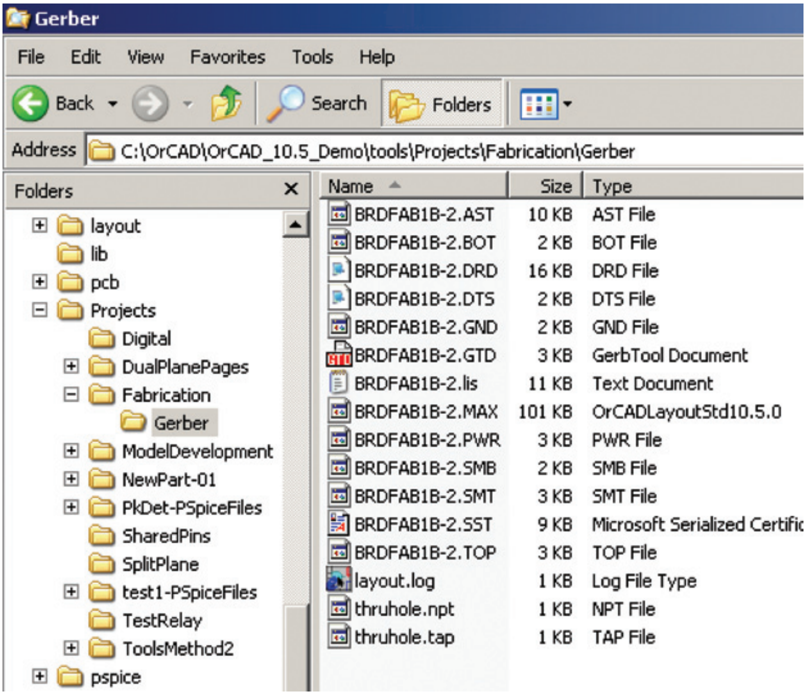
Drill tape written to 'c:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\FABRICATION\GERBER\thruhole.npt'.

Figure 10-6 Gerber file reports.



```
Post Processor Report
OrCAD FILE: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\FABRICATION\GERBER\BRDFAB1B-2.MAX
Sat Mar 25 14:24:18 2006

*********************************************************

Output file: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\FABRICATION\GERBER\BRDFAB1B-2.TOP

Aperture totals for C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\FABRICATION\GERBER\BRDFAB1B-2.TOP:
---------------------------------------------------------
D10:  0.0520 ROUND  --        0 Draws,       2 Flashes
D11:  0.0520 SQUARE --        0 Draws,       2 Flashes
D12:  0.0500 SQUARE --        0 Draws,       6 Flashes
D13:  0.1000 ROUND  --        0 Draws,       5 Flashes
D14:  0.1000 SQUARE --        0 Draws,       1 Flashes
D15:  0.0940 x 0.0250 OBLONG    -----        7 Flashes
D16:  0.0940 x 0.0250 RECTANGLE -----        1 Flashes
D17:  0.2500 ROUND  --        0 Draws,       1 Flashes
D18:  0.0010 ROUND  --        0 Draws,       1 Flashes
D19:  0.0120 ROUND  --       43 Draws,       0 Flashes
D20:  0.0500 ROUND  --        0 Draws,       8 Flashes
---------------------------------------------------------
 11 D-Codes      -----       43 Draws,      34 Flashes

*********************************************************
```

Figure 10-7 Postprocessor report.


Gerber
File
Edit
View
Favorites
Tools
Help
Back
Search
Folders
Address
Folders
layout
lib
pcb
Projects
Digital
DualPlanePages
Fabrication
Gerber
ModelDevelopment
NewPart-01
PkDet-PSpiceFiles
SharedPins
SplitPlane
test1-PSpiceFiles
TestRelay
ToolsMethod2
pspice

C:\OrCAD\OrCAD_10.5_Demo\tools\Projects\Fabrication\Gerber

Name	Size	Type
BRDFAB1B-2.AST	10 KB	AST File
BRDFAB1B-2.BOT	2 KB	BOT File
BRDFAB1B-2.DRD	16 KB	DRD File
BRDFAB1B-2.DTS	2 KB	DTS File
BRDFAB1B-2.GND	2 KB	GND File
BRDFAB1B-2.GTD	3 KB	GerbTool Document
BRDFAB1B-2.lis	11 KB	Text Document
BRDFAB1B-2.MAX	101 KB	OrCADLayoutStd10.5.0
BRDFAB1B-2.PWR	3 KB	PWR File
BRDFAB1B-2.SMB	2 KB	SMB File
BRDFAB1B-2.SMT	3 KB	SMT File
BRDFAB1B-2.SST	9 KB	Microsoft Serialized Certific
BRDFAB1B-2.TOP	3 KB	TOP File
layout.log	1 KB	Log File Type
thruhole.npt	1 KB	NPT File
thruhole.tap	1 KB	TAP File

Figure 10-8 Locating and zipping the Gerber files.

Fabricating the Board

Most board houses like to have the files compressed into a Zip file. The thruhole.NPT is not included in this example since it is not part the standard fabrication process.

Choosing a board house

Not all board houses are the same. While most follow certain fabrication standards, not all will have the same fabrication capabilities (e.g., number of layers, copper thickness, and drill sizes). There are also differences in design submission policies and minimum order and billing practices. Many board houses use a quote method similar to the one described here, but not all do. Some have you send the Gerber files by e-mail, and after someone looks at them with CAM software (such as GerbTool) they send a quote back to you via e-mail. Advanced Circuits uses a Web-based file submission process that is very user friendly, and they have granted permission to print screen shots of their Web site and submit a practice board design.

Setting up a user account

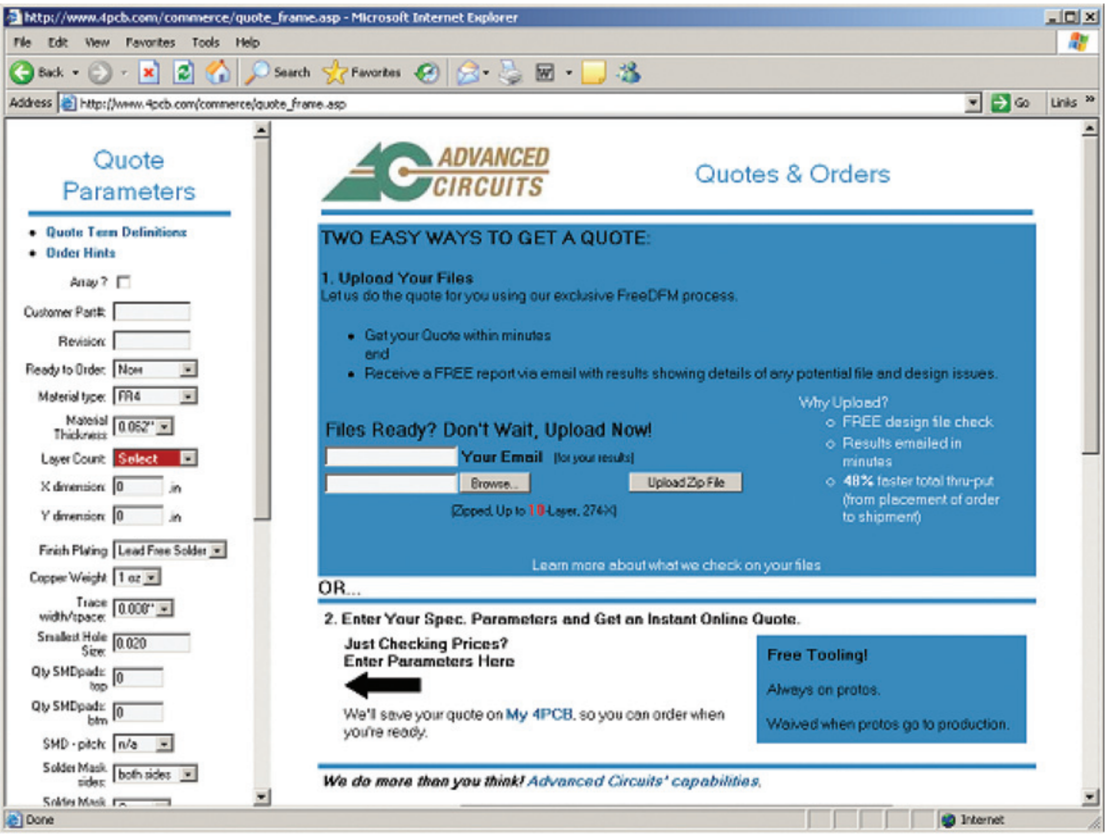
As with anything nowadays you will need to set up a user profile to submit your design files, but the registration is free. To set up a profile go to www.4pcb.com. Follow the Click Here to Register link. Follow the online instructions (two steps) to complete your registration.

In a few minutes you will receive an e-mail confirming your registration and a link to set up your password and activate your free account. After you choose your password you will be directed to an options page where you can check your Open PCB Orders, Existing PCB Quotes, and PCB Order History.

Submitting Gerber files and requesting a quote

To demonstrate the file submission process we will submit a design for a quote (not the same thing as placing an order). **To submit a design for a quote** click on the Get a Quote Now! link.

The Advanced Circuits quote page is shown in Fig. 10-9. There are two ways to submit a quote. The first is to use the selection lists on the left side of the page to describe the characteristics of your board. This method works well if you are intimately familiar with the parameters of your board. The second method is to upload your Gerber files and—through an automated process—have your board analyzed and a quote produced. This is the method that


http://www.4pcb.com/commerce/quote_frame.asp - Microsoft Internet Explorer
File
Edit
View
Favorites
Tools
Help
Back
Search
Favorites
Address
http://www.4pcb.com/commerce/quote_frame.asp
Go
Links
ADVANCED CIRCUITS
Browse...
Upload Zip File
Done
Internet

Quote Parameters

- Quote Term Definitions
- Order Hints

Array ? ☐
Customer Part#:
Revision:
Ready to Order: Now
Material type: FR4
Material Thickness: 0.062"
Layer Count: Select
X dimension: 0 in
Y dimension: 0 in
Finish Plating: Lead Free Solder
Copper Weight: 1 oz
Trace width/space: 0.008"
Smallest Hole Size: 0.020
Qty SMDpads top: 0
Qty SMDpads btm: 0
SMD - pitch: n/a
Solder Mask sides: both sides
Solder Mask

Quotes & Orders

TWO EASY WAYS TO GET A QUOTE:

1. Upload Your Files
Let us do the quote for you using our exclusive FreeDFM process.

- Get your Quote within minutes
  and
- Receive a FREE report via email with results showing details of any potential file and design issues.

Files Ready? Don't Wait, Upload Now!

Your Email (for your results)

(Zipped, Up to 10-Layer, 274-X)

Why Upload?
- FREE design file check
- Results emailed in minutes
- **48%** faster total thru-put (from placement of order to shipment)

Learn more about what we check on your files

OR...

2. Enter Your Spec. Parameters and Get an Instant Online Quote.

**Just Checking Prices?
Enter Parameters Here**

We'll save your quote on **My 4PCB**, so you can order when you're ready.

Free Tooling!

Always on protos.

Waived when protos go to production.

We do more than you think! Advanced Circuits' capabilities.

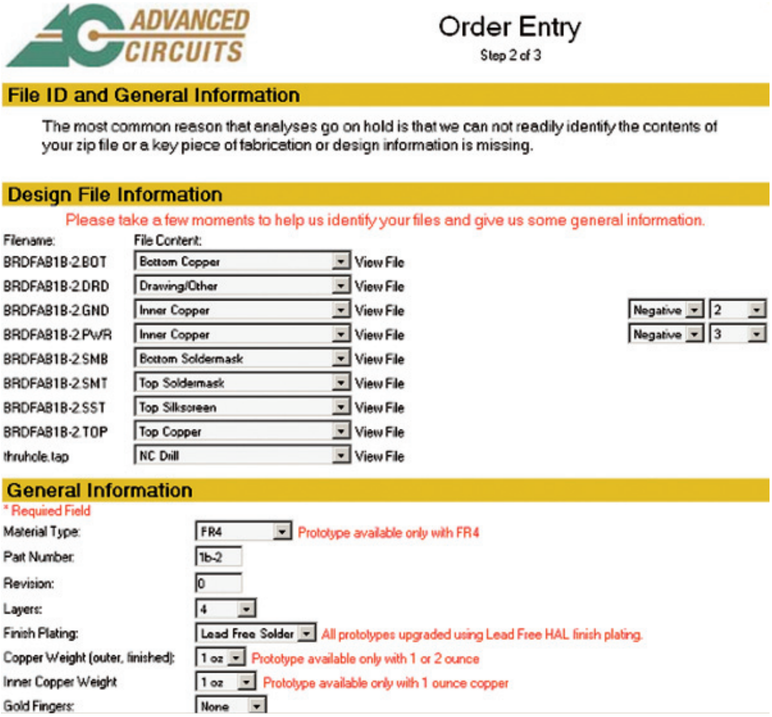
Figure 10-9 Submitting the Gerber files for an online quote.

will be used here. Note that the look of the Web page may have changed since this book was printed, but the process will likely be similar.

To upload Gerber design files enter your e-mail address, use the Browse... button to locate the Zip file that contains the Gerber files, and click the Upload Zip File button.

Annotating the layer types and stack-up

Moments after you upload your zipped Gerber files you will be taken to the Web page shown in Fig. 10-10. Most of the files will be correctly annotated (i.e., xxx.TOP is correctly assigned to Top Copper), but check them over carefully to make sure. Usually you will have to assign a File Content (using the selection lists shown in Fig, 10-10) to the file you uploaded that describes the board outline, etc. (DRD, FAB, AST, etc.). That file is assigned Drawing/Other.



Order Entry

Step 2 of 3

File ID and General Information

The most common reason that analyses go on hold is that we can not readily identify the contents of your zip file or a key piece of fabrication or design information is missing.

Design File Information

Please take a few moments to help us identify your files and give us some general information.

Filename:	File Content:			
BRDFAB1B-2.BOT	Bottom Copper	View File		
BRDFAB1B-2.DRD	Drawing/Other	View File		
BRDFAB1B-2.GND	Inner Copper	View File	Negative	2
BRDFAB1B-2.PWR	Inner Copper	View File	Negative	3
BRDFAB1B-2.SMB	Bottom Soldermask	View File		
BRDFAB1B-2.SMT	Top Soldermask	View File		
BRDFAB1B-2.SST	Top Silkscreen	View File		
BRDFAB1B-2.TOP	Top Copper	View File		
thruhole.tap	NC Drill	View File		

General Information

* Required Field

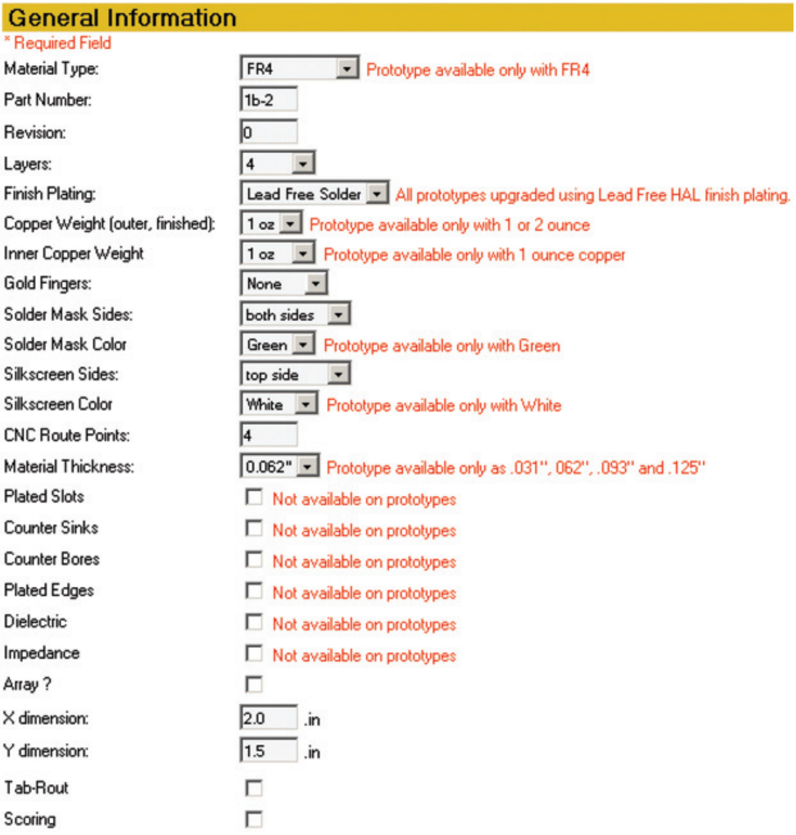
Material Type:	FR4	Prototype available only with FR4
Part Number:	1b-2	
Revision:	0	
Layers:	4	
Finish Plating:	Lead Free Solder	All prototypes upgraded using Lead Free HAL finish plating.
Copper Weight (outer, finished):	1 oz	Prototype available only with 1 or 2 ounce
Inner Copper Weight	1 oz	Prototype available only with 1 ounce copper
Gold Fingers:	None	

Figure 10-10 Specifying the layer type and stack-up.

This is the point at which you declare the layer stack-up. It is obvious where the TOP and BOTTOM layers go (layers 1 and 4 for this example), but the inner layers need to be specified and are so done using the dropdown lists at the right of the page. For this example the ground plane is placed next to the top layer, so it is No. 2, and the power plane is assigned layer No. 3.

Included in Gerber files is a code that indicates the image polarity of the layer (not the voltage polarity). Since plane layers in Layout are negative layers, make sure that the polarities are properly assigned. This step allows you to verify that the inner layers (power and ground planes) are indeed negative layers.

The Gerber files are analyzed by a CAM processor and checked for errors. To assist in making an accurate quote, a few more entries are made on the quote form as shown in Fig. 10-11. Items such as the color of the soldermask and silk screen and the thickness of the copper are not included in the Gerber files. See the section in Chap. 9 about using Layout's Stackup Editor to generate a stack-up drawing, which can be included with the Gerber files.



General Information

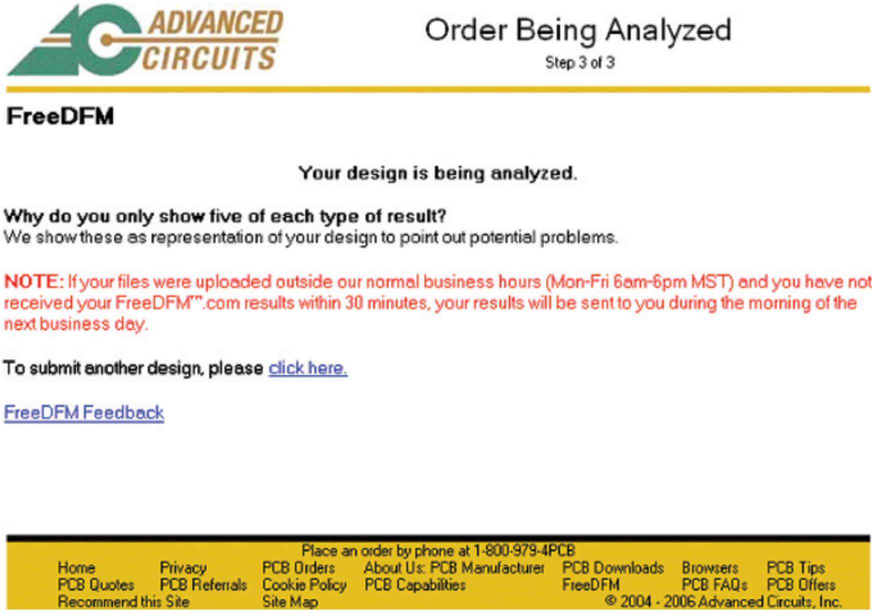
* Required Field

Material Type:	FR4	Prototype available only with FR4
Part Number:	1b-2	
Revision:	0	
Layers:	4	
Finish Plating:	Lead Free Solder	All prototypes upgraded using Lead Free HAL finish plating.
Copper Weight (outer, finished):	1 oz	Prototype available only with 1 or 2 ounce
Inner Copper Weight	1 oz	Prototype available only with 1 ounce copper
Gold Fingers:	None	
Solder Mask Sides:	both sides	
Solder Mask Color	Green	Prototype available only with Green
Silkscreen Sides:	top side	
Silkscreen Color	White	Prototype available only with White
CNC Route Points:	4	
Material Thickness:	0.062"	Prototype available only as .031", 062", .093" and .125"
Plated Slots	☐	Not available on prototypes
Counter Sinks	☐	Not available on prototypes
Counter Bores	☐	Not available on prototypes
Plated Edges	☐	Not available on prototypes
Dielectric	☐	Not available on prototypes
Impedance	☐	Not available on prototypes
Array ?	☐	
X dimension:	2.0 .in	
Y dimension:	1.5 .in	
Tab-Rout	☐	
Scoring	☐	

Figure 10-11 Additional PCB design parameters.

Once you have finished entering the design parameters hit the **Submit** button. If there are problems with any of the entries you will be notified immediately. If everything was entered correctly you will be taken to a page (Fig. 10-12) that tells you that the design is being analyzed.

Depending on the complexity of the board, and the number of other boards submitted by other customers at the same time, you should have a quote back within a few minutes to an



Order Being Analyzed

Step 3 of 3

FreeDFM

Your design is being analyzed.

Why do you only show five of each type of result?
We show these as representation of your design to point out potential problems.

NOTE: If your files were uploaded outside our normal business hours (Mon-Fri 6am-6pm MST) and you have not received your FreeDFM™.com results within 30 minutes, your results will be sent to you during the morning of the next business day.

To submit another design, please click here.

FreeDFM Feedback

Place an order by phone at 1-800-979-4PCB

Home	Privacy	PCB Orders	About Us: PCB Manufacturer	PCB Downloads	Browsers	PCB Tips
PCB Quotes	PCB Referrals	Cookie Policy	PCB Capabilities	FreeDFM	PCB FAQs	PCB Offers
Recommend this Site		Site Map				

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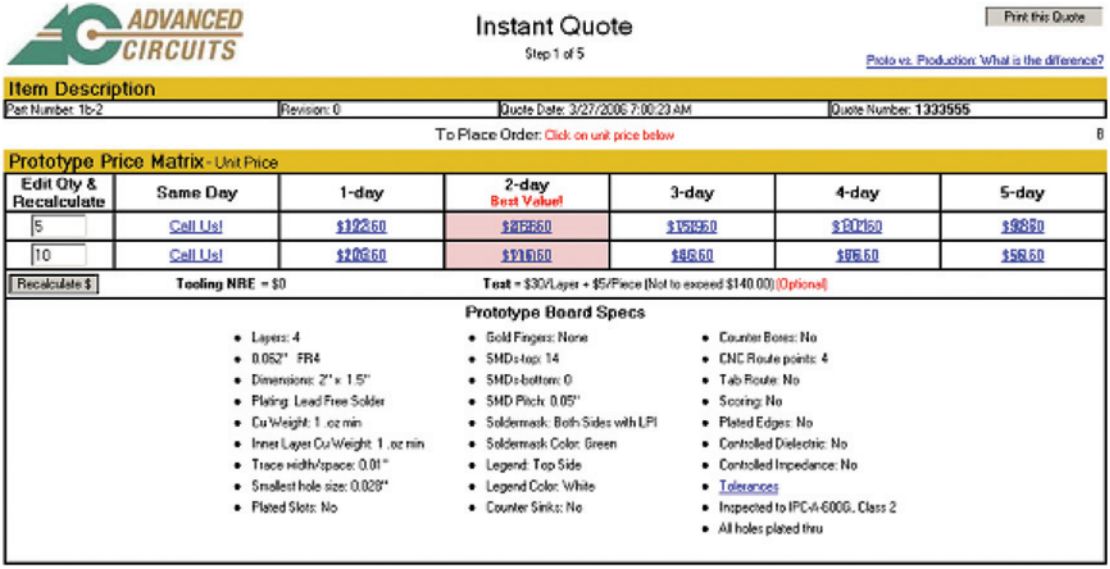
Figure 10-12 Design submission complete.

hour. An example of a quote for a prototype board is shown in Fig. 10-13. Note that the prices indicated in the quote are fictitious and shown for illustration purposes only. Also, only the prototype quote is shown in the figure due to space constraints (production quotes are on the



Instant Quote

Step 1 of 5

Proto vs. Production: What is the difference?

Item Description

Part Number: 1b-2	Revision: 0	Quote Date: 3/27/2006 7:00:23 AM	Quote Number: **1333555**

To Place Order: Click on unit price below

Prototype Price Matrix - Unit Price

Edit Qty & Recalculate	Same Day	1-day	2-day Best Value!	3-day	4-day	5-day
5	Call Us!	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
10	Call Us!	[illegible]	[illegible]	[illegible]	[illegible]	$56.60

Tooling NRE = $0

Test = $30/Layer + $5/Piece (Not to exceed $140.00) (Optional)

Prototype Board Specs

- Layers: 4
- 0.062" FR4
- Dimensions: 2" x 1.5"
- Plating: Lead Free Solder
- Cu Weight: 1 .oz min
- Inner Layer Cu Weight: 1 .oz min
- Trace width/space: 0.01"
- Smallest hole size: 0.028"
- Plated Slots: No
- Gold Fingers: None
- SMDs-top: 14
- SMDs-bottom: 0
- SMD Pitch: 0.05"
- Soldermask: Both Sides with LPI
- Soldermask Color: Green
- Legend: Top Side
- Legend Color: White
- Counter Sinks: No
- Counter Bores: No
- CNC Route points: 4
- Tab Route: No
- Scoring: No
- Plated Edges: No
- Controlled Dielectric: No
- Controlled Impedance: No
- Tolerances
- Inspected to IPC-A-600G, Class 2
- All holes plated thru

Figure 10-13 The quote.

same page but were not included in the figure). You can change the quantity and recalculate the price breakdown. Once you have decided the number of boards and lead time, click the link in the cell to order the board.

Receipt inspection and testing

Regardless of who fabricates your boards, you should perform an inspection of the boards, especially if it is a first run. You may also want to do some initial electrical tests (continuity and isolation), especially on the power and ground, before you place any components on the board. IPC-2515 and IPC-6011 outline many types of inspection and acceptance tests.

Nonstandard Gerber files

Some board houses have their own naming convention for the Gerber files, but the content of the files is often the same. In those cases you can change the extensions of the Gerber files without harming the files themselves. However, it is recommended that you only change the names of *copies* of the files. Keep the original files intact and in a safe place for your records.

Some CNC machines use proprietary software that does not accept all Gerber files either. We will look at how to modify the Gerber files using GerbTool for use with CNC machines in Chap. 11.

CHAPTER 11

Additional Tools

This chapter introduces tools that work with Capture and Layout in the design and manufacturing of PCBs. Some of the tools are included with the OrCAD design suite, while others are completely independent of OrCAD. The tools that are part of OrCAD are PSpice and SPECCTRA; the independent tools discussed here are GerbTool, Microsoft Excel, and CAD drawing tools.

Using PSpice to Simulate Transmission Lines

PSpice was used in Chap. 7 to develop PSpice subcircuit models for creating new Capture parts with simulation capabilities. In this chapter PSpice is used to simulate transmission lines. When used in conjunction with the design equations from Chap. 6 (and the design example in Chap. 9) PSpice can be of help in designing PCB-based transmission lines and in understanding transmission lines in general.

The circuit shown in Fig. 11-1 is used here to simulate a high-speed digital circuit (it was also used to generate the plots used to explain ringing in Chap. 6). The circuit consists of a driver

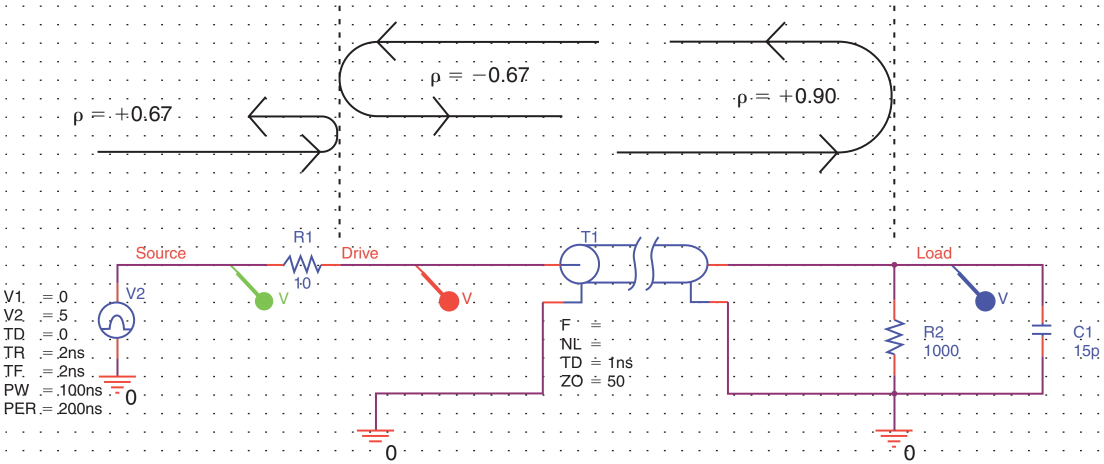


Figure 11-1 A basic transmission line simulation circuit.

gate with an output impedance of 10 Ω, a 50-Ω transmission line, and a receiving gate with an input resistance of 1 kΩ and input capacitance of 15 pF. The PSpice parts used in the circuit are the following:

- V_2 is VPULSE (from the Source library), the driver.
- R1 is R (from the Analog library), the source resistance (output impedance) of the driver.
- T1 is T (from the Analog library), the transmission line.
- R2 is R (from the Analog library), the load resistance.
- C1 is C (from the Analog library), the load capacitance.

Figure 11-1 also shows the various reflection coefficients at the impedance mismatches at which the reflection coefficient looking into T1 from R1 is

$$\rho = \frac{Z_0 - \mathrm{R1}}{Z_0 + \mathrm{R1}} = \frac{50 - 10}{50 + 10} = +0.667,$$

the reflection coefficient looking into R1 from T1 is

$$\rho = \frac{\mathrm{R1} - Z_0}{\mathrm{R1} + Z_0} = \frac{10 - 50}{10 + 50} = -0.667,$$

and the reflection coefficient looking into R2 from T1 is

$$\rho = \frac{\mathrm{R2} - Z_0}{\mathrm{R2} + Z_0} = \frac{1000 - 50}{1000 + 50} = +0.90.$$

To simulate a transmission line (T1) the characteristic impedance, Z_0, must be specified and either the transmission delay (TD) must be specified or the frequency (f) and number of wavelengths (NL) must be specified. Use TD for digital signals and use f and NL for analog signals.

Simulating digital transmission lines

The value TD is the same as PT (propagation time) from the discussion in Chap. 6 and is calculated by

$$\mathrm{TD} = t_{\mathrm{PD}} \cdot \mathrm{Length}_{\mathrm{trace}},$$

where t_{PD} is found from the tables in Chap. 6. For the surface microstrip, t_{PD} is

$$t_{\mathrm{PD}} = 85\sqrt{0.475\varepsilon_r + 0.67}$$

In laying out a digital circuit (for instance, the digital design example in Chap. 9) it is important to know the critical trace length so that traces can be kept short enough and parts can be placed accordingly. The critical trace length is calculated by

$$\text{Length}_{\text{trace}} < \frac{\text{RT}}{k \cdot t_{\text{PD}}},$$

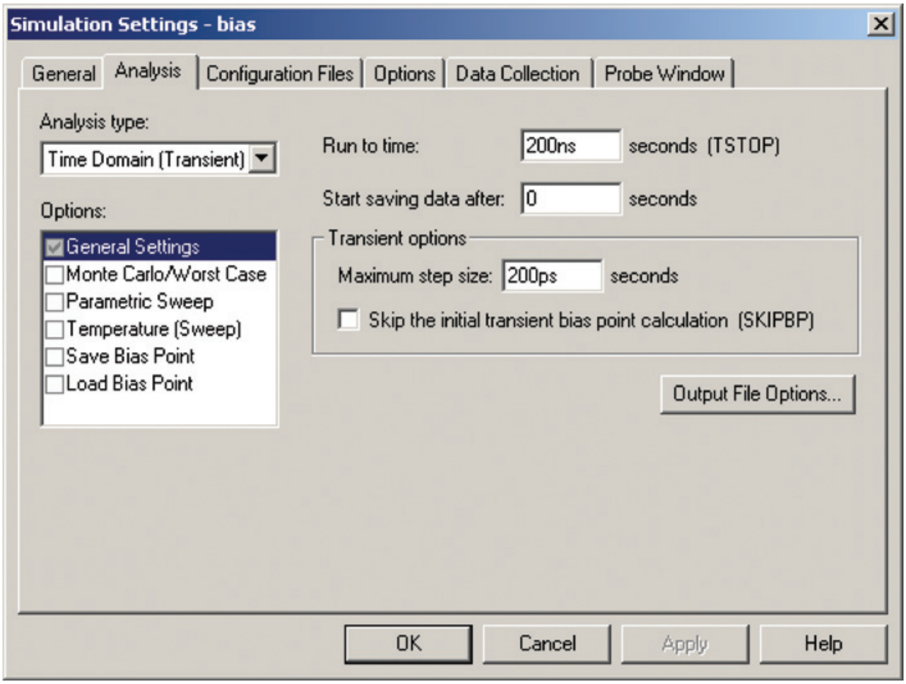
where k is a safety factor and is essentially the ratio PT/RT. The maximum trace length recommended is with $k = 2$; larger values of k (shorter traces) are better.

For ALS family logic RT is approximately 2 ns. Using $\varepsilon_r = 4.2$, the critical trace length is then 7.3 in. Table 11-1 shows the effective k value and TD for various transmission line lengths.

	Long	**Critical**	**Safe**
$\text{Length}_{\text{trace}}$ (in.)	30	7.3	3.5
k (approximate)	1/2	2	4
TD (ns)	4.1	1	0.24

Table 11-1 TD calculations considering various trace lengths

Knowing RT (2 ns) and TD (from Table 11-1), we can use PSpice to simulate the various transmission line lengths. Set up the PSpice simulation as shown in Fig. 11-2. To display the



Analysis type: Time Domain (Transient)

Options:
- ☑ General Settings
- ☐ Monte Carlo/Worst Case
- ☐ Parametric Sweep
- ☐ Temperature (Sweep)
- ☐ Save Bias Point
- ☐ Load Bias Point

Run to time: 200ns seconds (TSTOP)

Start saving data after: 0 seconds

Transient options

Maximum step size: 200ps seconds

☐ Skip the initial transient bias point calculation (SKIPBP)

Figure 11-2 PSpice simulations settings.

Simulation Settings dialog box select **Edit Simulation Profile** from the **PSpice** menu. Note that if the step time is too large the simulation may become unstable and you will not get good results. A maximum step size of 1/1000 of the total run time usually produces satisfactory results. Click **OK.**

To start the simulation press the blue triangle on the menu bar, or press **F11** on the keyboard, or select **Run** from the **PSpice** menu. The results are shown in Figs. 11-3, 11-4, and 11-5.

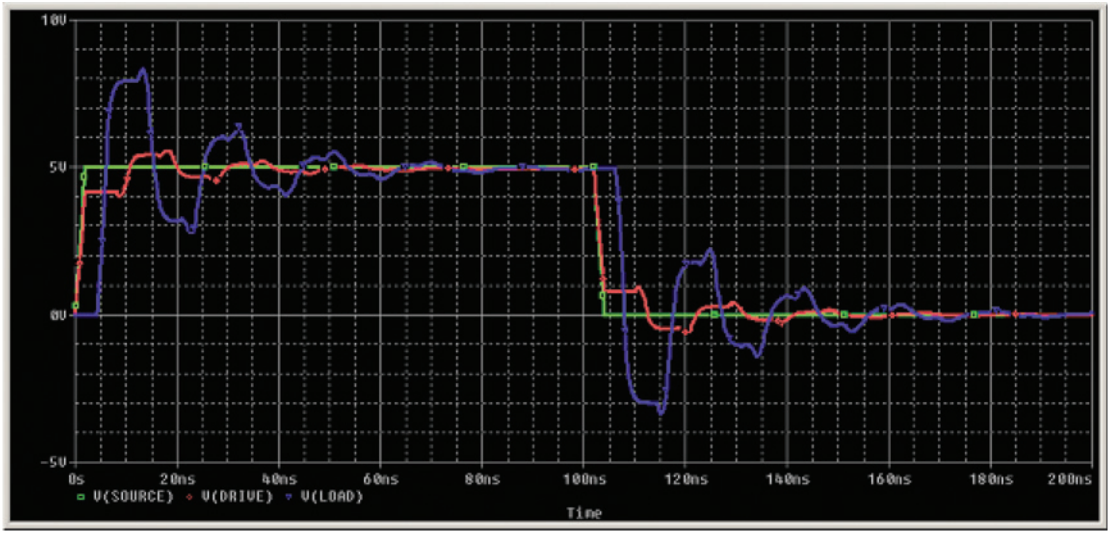


Figure 11-3 Simulation results for a long line ($k = 1/2$).

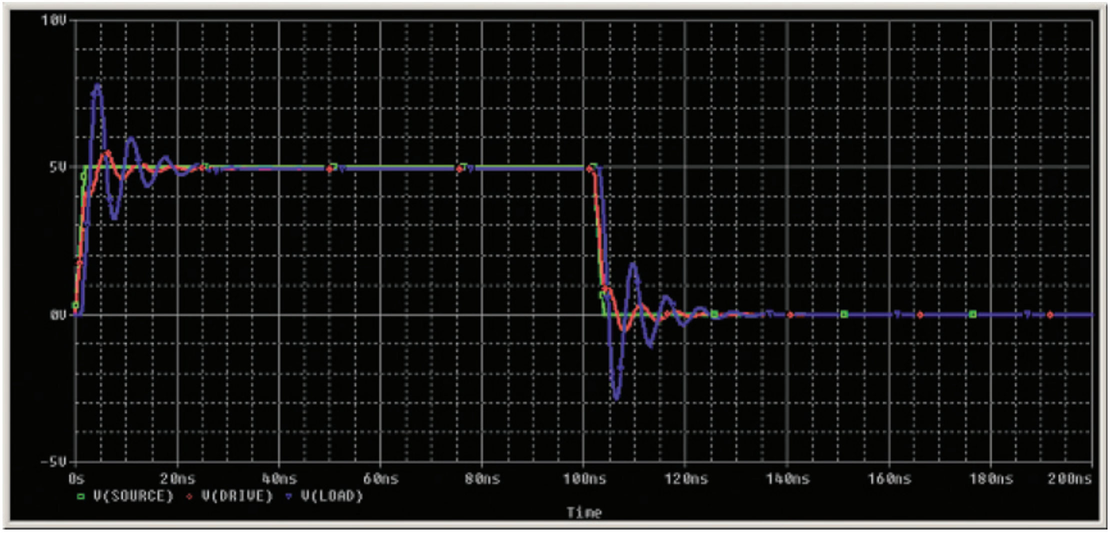


Figure 11-4 Simulation results for a critical-length line ($k = 2$).

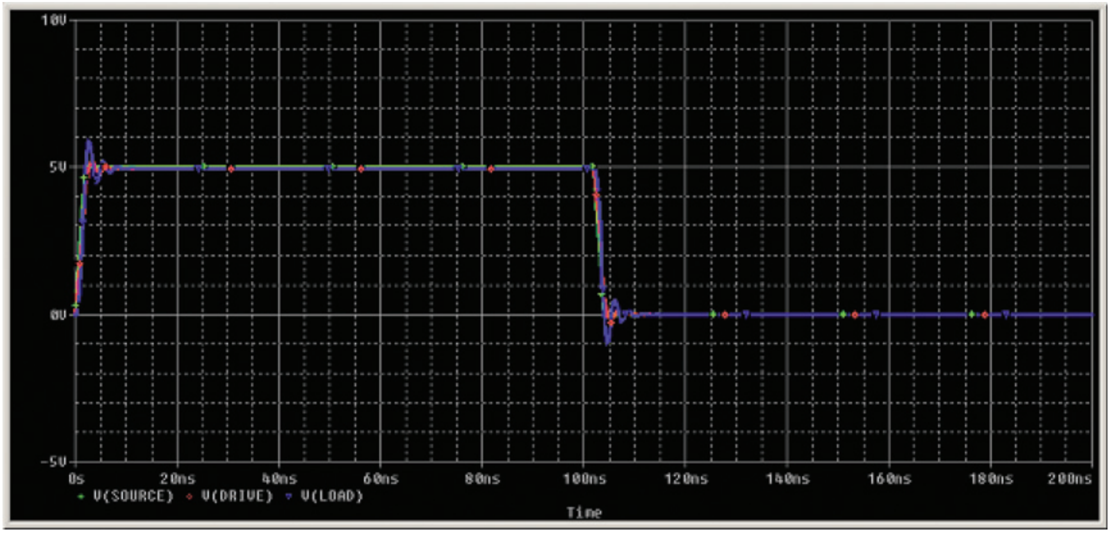


Figure 11-5 Simulation results for a short line (k = 4).

Simulating analog signals

For analog signals f is the frequency on the trace and NL is the length of the trace in relative wavelengths (e.g., NL would be 0.25 for a quarter-wavelength trace at frequency f). To determine NL you need to know the wavelength, λ. You can calculate the wavelength using Eq. (1),

$$\lambda = \frac{v_{\mathrm{PD}}}{f} = \frac{1}{f \cdot t_{\mathrm{PD}}}, \tag{1}$$

where v_{PD} is the propagation velocity (distance/time) of a wave through a dielectric, f is the frequency of the wave, and t_{PD} is the propagation time (time/distance) as described above.

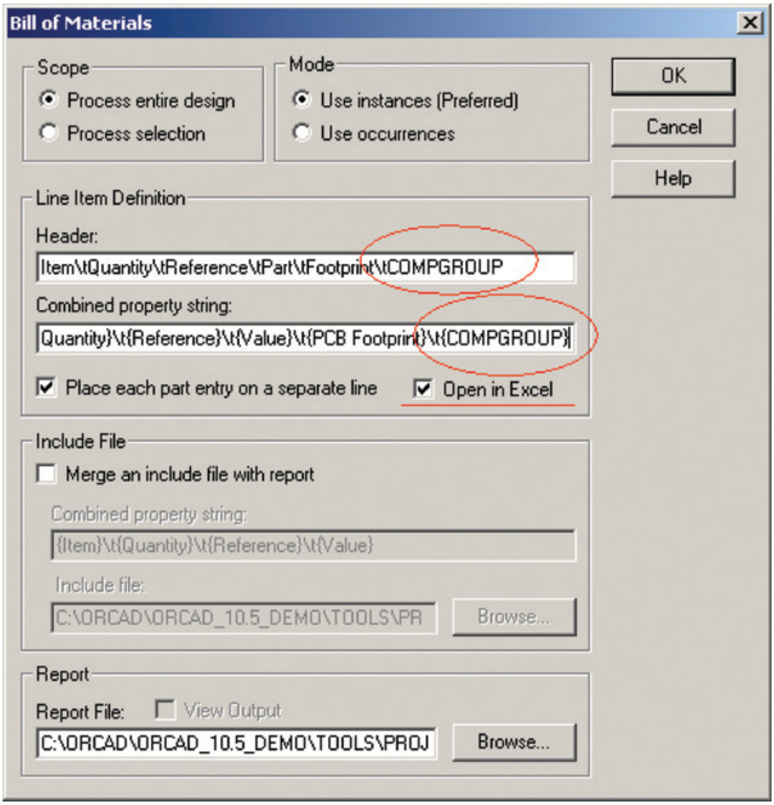
So for a 66-MHz signal traveling through the same surface microstrip from the above example ($\varepsilon_r = 4.2$), $\lambda = 110.8$ in. The critical length for traces carrying analog signals varies depending on which reference you read, but is often cited as being $\lambda/6$, $\lambda/15$, or $\lambda/20$ (or somewhere in between). As with the digital signals, the shorter the trace the better.

Using Microsoft Excel with a Bill of Materials Generated by Capture

In the design examples it was mentioned that Excel can be used with the bill of materials (BOM). The nice thing about using the Excel spreadsheet is that you can easily modify the BOM to suite your needs. You can export any of the Capture part properties (from the **Edit Properties** spreadsheet) into Excel and have the data sorted in ascending or descending order by any of the headers listed in the BOM. For example you could sort the list by COMPGROUP number and then print the spreadsheet as an aid when placing parts in Layout. You could also sort by footprint, part reference, etc.

As an example, let's say you wanted a chronological listing of the component groups while placing parts on the PCB. The first step is to add the COMPGROUP property to the Bill of Materials listing and export it into an Excel spreadsheet. Then you can have Excel sort the data, add outlines and other information, and then print the listing. To add the COMPGROUP property to the BOM go to the Capture Project Manager, select the Design icon, and then select Bill of Materials… from the Tools menu.

The Bill of Materials dialog box will be displayed as shown in Fig. 11-6. Add the text, "\tCOMPGROUP" to the Header: list and "\t{COMPGROUP}" to the Combined property string: list. Check the Open in Excel box and select a path and file name in the Report File: text box. Click OK. An example BOM in an Excel spreadsheet is shown in Fig. 11-7.



● Process entire design
○ Process selection

● Use instances (Preferred)
○ Use occurrences

Header: Item\tQuantity\tReference\tPart\tFootprint\tCOMPGROUP

Combined property string: Quantity}\t{Reference}\t{Value}\t{PCB Footprint}\t{COMPGROUP}

☑ Place each part entry on a separate line
☑ Open in Excel

☐ Merge an include file with report

Combined property string: {Item}\t{Quantity}\t{Reference}\t{Value}

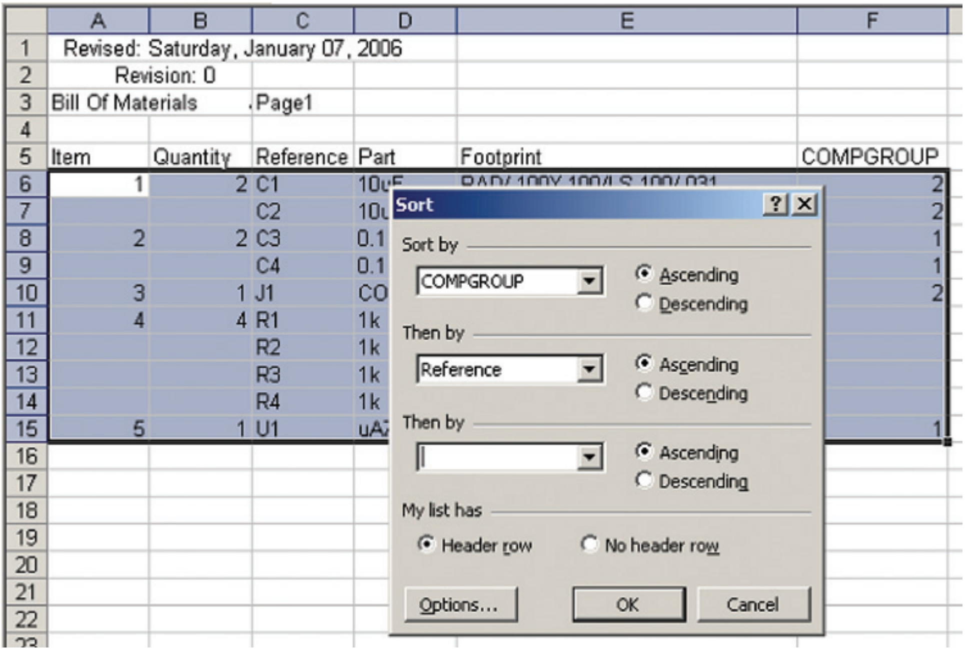
Include file: C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PR

Report File: ☐ View Output

C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJ

Figure 11-6 Modifying the Bill of Materials list to include COMPGROUP.

To sort a BOM in Excel, select the list including the headers. From the Data menu select Sort to bring up the Sort dialog box (shown in Fig. 11-7). Using the Sort by lists you can



	A	B	C	D	E	F
1	Revised: Saturday, January 07, 2006					
2	Revision: 0					
3	Bill Of Materials		Page1			
4						
5	Item	Quantity	Reference	Part	Footprint	COMPGROUP
6	1	2	C1	10uF		2
7			C2	10u		2
8	2	2	C3	0.1		1
9			C4	0.1		1
10	3	1	J1	CO		2
11	4	4	R1	1k		
12			R2	1k		
13			R3	1k		
14			R4	1k		
15	5	1	U1	uA7		1

Sort

Sort by: COMPGROUP ● Ascending ○ Descending

Then by: Reference ● Ascending ○ Descending

Then by: ● Ascending ○ Descending

My list has: ● Header row ○ No header row

Figure 11-7 Using Excel to sort and display a BOM.

specify how Excel should list the items of interest. You can sort the data repeatedly using different headers in the BOM. This provides a powerful and convenient tool for making sure you have the correct footprints assigned, etc., before making the .MNL netlist and beginning work in Layout.

Using the SPECCTRA Autorouter with Layout

SPECCTRA (now called Allegro PCB Router) is a shape-based autorouter that is included with and works with Layout. SPECCTRA uses different algorithms during the routing process and can usually route high-density boards faster and with fewer cleanup actions than Layout. You can use SPECCTRA by itself or launch it from Layout and have the two applications tag-team on the PCB. Figure 11-8(a) shows what SPECCTRA looks like if used in the stand-alone mode and Fig. 11-8(b) shows what SPECCTRA looks like if used with Layout.

To launch SPECCTRA without Layout navigate to Start → All Programs → OrCAD 10.5 Demo → SPECCTRA Demo. Figure 11-9 shows the start-up window and a SPECCTRA design file. Use the Browse… button to select a design file (xxx.dsn), which is different from a Capture design file with the same extension. There are several design examples you can open. One design example (design.dsn) is located in the OrCAD/tools/specctra/common folder and lesson(n).dsn, and there are several more example designs located in the /OrCAD/share/specctra/tutorial folder. Once you have selected a design, click Start Allegro PCB Router (you can ignore Do file entries, etc.). If you are using the Demo version it will take a few minutes as SPECCTRA searches for a license. When it does not find one, click OK at the License Error box, click OK at the License Not Found box, click OK at the No Rules Found box. You will end up with a session as shown in Fig. 11-8(a). Although

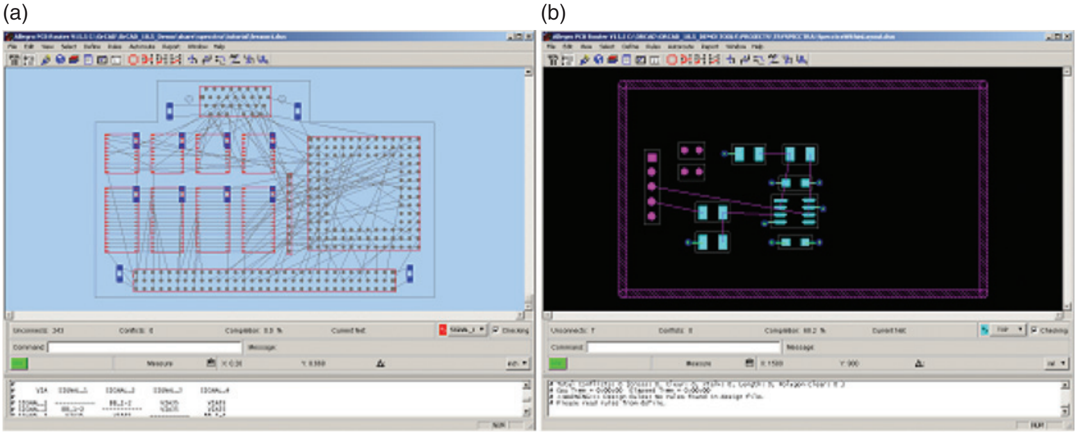
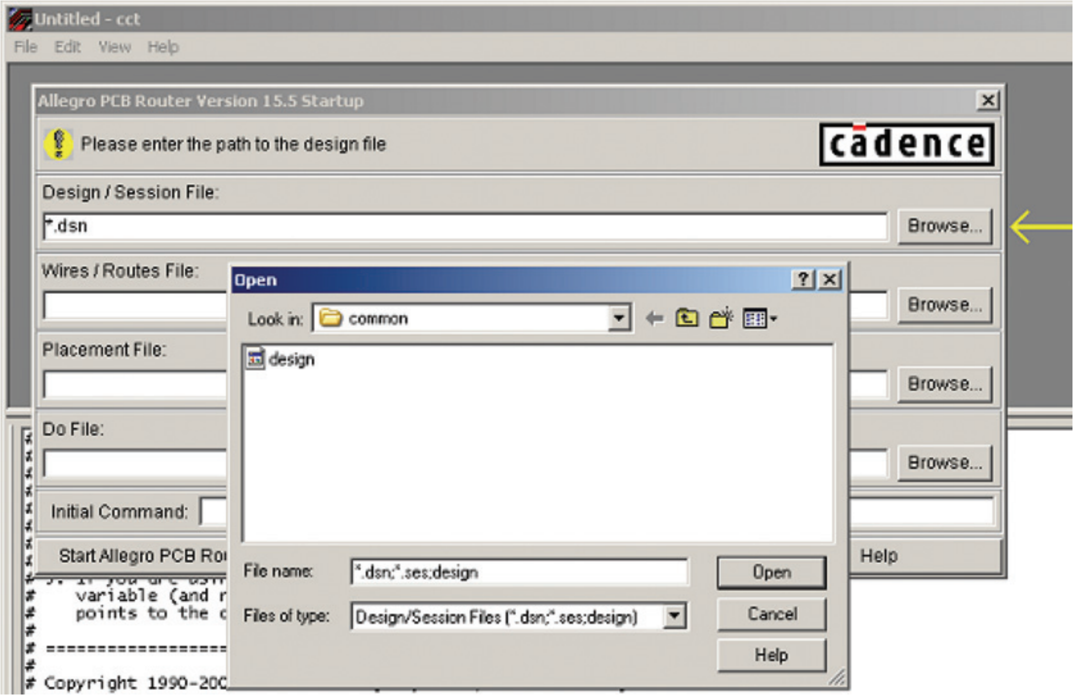


Figure 11-8 The two appearances of SPECCTRA. (a) Stand-alone SPECCTRA. (b) SPECCTRA from Layout.


Untitled - cct
File
Edit
View
Help
Allegro PCB Router Version 15.5 Startup
cadence
Wires / Routes File:
Placement File:
Do File:
Initial Command:
Start Allegro PCB Ro
Browse...
Browse...
Browse...
Browse...
Help
Open
Open
Cancel
Help
# variable (and r
# points to the c
# ==================
# Copyright 1990-200

Please enter the path to the design file

Design / Session File: *.dsn

Look in: common

design

File name: *.dsn;*.ses;design

Files of type: Design/Session Files (*.dsn;*.ses;design)

Figure 11-9 Starting the SPECCTRA autorouter.

the appearance of SPECCTRA is dependent on how it was launched, the tools are the same. Since we are interested in using SPECCTRA with Layout, the tools will be discussed from that perspective.

To launch SPECCTRA from Layout you will need to have a board design open in Layout. You can do all portions of the PCB design with SPECCTRA, but in this basic demonstration Layout is used to set up the basic board design (as described in the examples in Chap. 9) and SPECCTRA will be used to autoroute the board. Basic board setup tasks performed in Layout include:

1. placing components,
2. setting up layers (power and ground planes) and net/layer assignments,
3. completing fanouts (although you can do this with SPECCTRA as well),
4. locking power and ground nets (if not automatically locked), and
5. enabling all nonpower/ground-type nets.

To launch and autoroute the board with SPECCTRA, select the Auto menu from the menu bar in Layout and then (as shown in Fig. 11-10) select Autoroute SPECCTRA → Launch

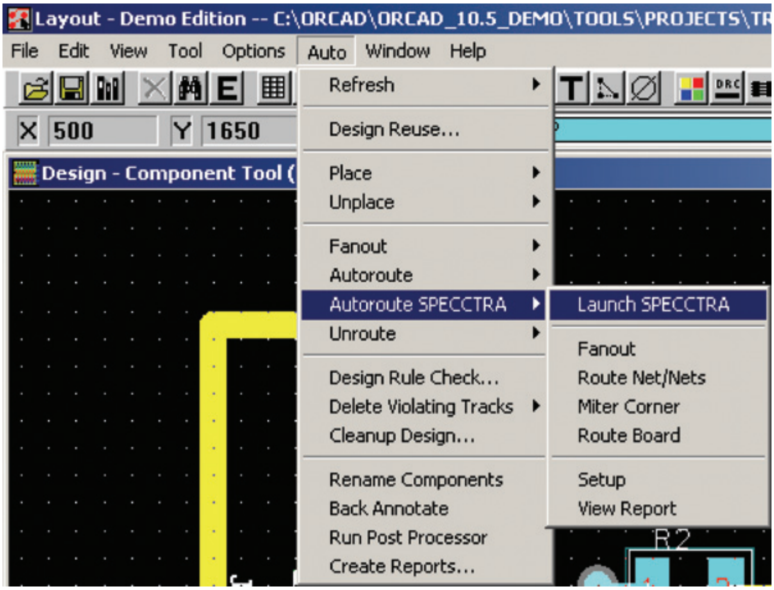

Layout - Demo Edition -- C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TR
File
Edit
View
Tool
Options
Auto
Window
Help
X 500
Y 1650
Design - Component Tool (
Refresh
Design Reuse...
Place
Unplace
Fanout
Autoroute
Autoroute SPECCTRA
Unroute
Design Rule Check...
Delete Violating Tracks
Cleanup Design...
Rename Components
Back Annotate
Run Post Processor
Create Reports...
Launch SPECCTRA
Fanout
Route Net/Nets
Miter Corner
Route Board
Setup
View Report
R2

Figure 11-10 Launching SPECCTRA from Layout.

SPECCTRA. Again SPECCTRA will look for a license, so click OK at the License Error box, click OK at the License Not Found box, and click OK at the No Rules Found box.

Once SPECCTRA is up and running you should see your PCB design from Layout in the SPECCTRA window. An example circuit is shown in Fig. 11-11.

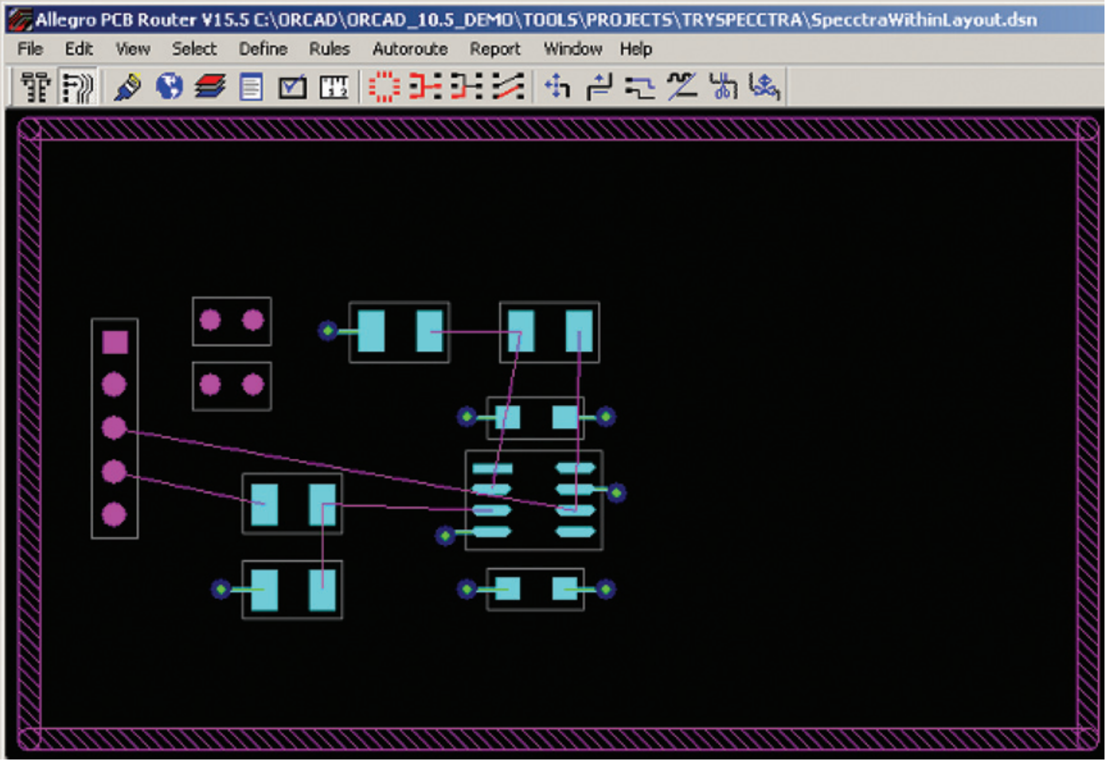

Allegro PCB Router V15.5 C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TRYSPECCTRA\SpecctraWithinLayout.dsn
File
Edit
View
Select
Define
Rules
Autoroute
Report
Window
Help

Figure 11-11 The PCB design in SPECCTRA.

To start the autorouting process select Route… from the Autoroute menu (see Fig. 11-12).

The AutoRoute dialog box (Fig. 11-13) will be displayed. To keep things simple select Basic and enter 25 in the Passes: box and then click OK. SPECCTRA will route the board using the rules imported from Layout. The routing results are shown in Fig. 11-14.

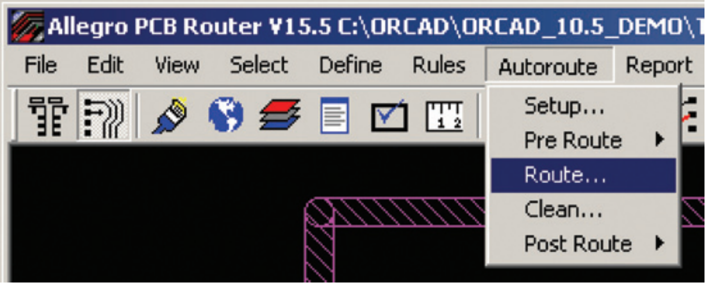
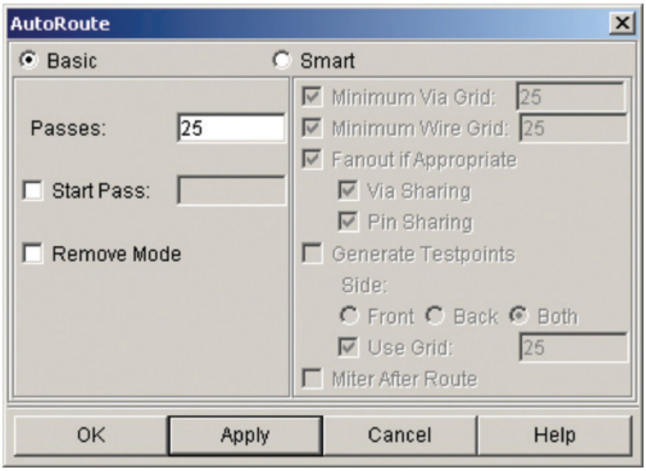

Allegro PCB Router V15.5 C:\ORCAD\ORCAD_10.5_DEMO\
File
Edit
View
Select
Define
Rules
Autoroute
Report
Setup…
Pre Route
Route…
Clean…
Post Route

Figure 11-12 Launching the autorouter.



AutoRoute

● Basic ○ Smart

Passes: 25

☐ Start Pass:

☐ Remove Mode

☑ Minimum Via Grid: 25

☑ Minimum Wire Grid: 25

☑ Fanout if Appropriate

☑ Via Sharing

☑ Pin Sharing

☐ Generate Testpoints

Side:

○ Front ○ Back ● Both

☑ Use Grid: 25

☐ Miter After Route

Figure 11-13 The SPECCTRA **AutoRoute** *dialog box.*

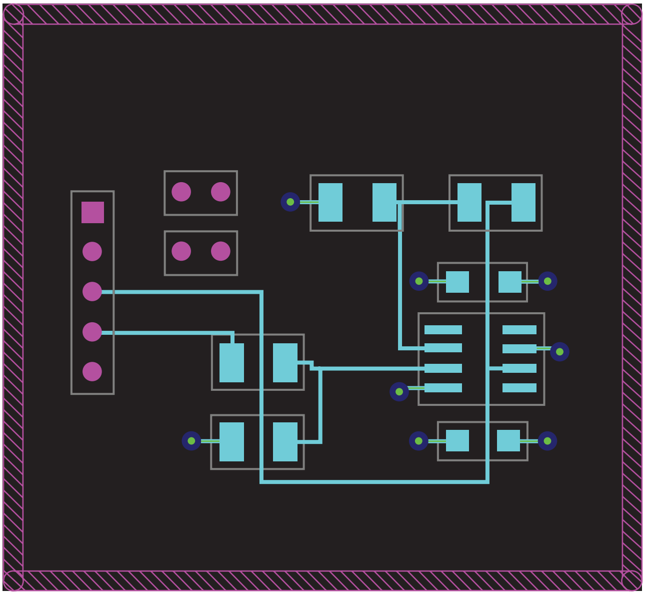
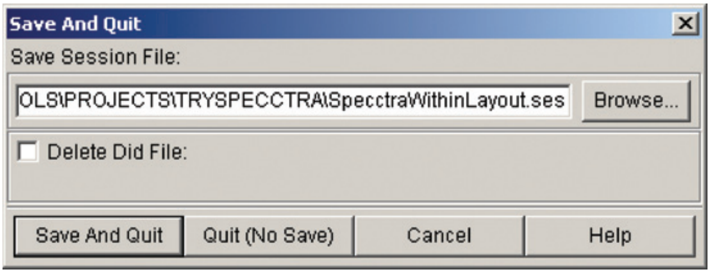


Figure 11-14 The circuit autorouted by SPECCTRA.

To transfer the routed board design from SPECCTRA back to Layout simply close SPECCTRA by selecting **Quit…** from the **File** menu, or click the **X** in the upper right-hand corner of the window.

In order for the transfer to be completed the **SpecctraWithinLayout.ses** file must be saved when SPECCTRA displays the **Save And Quit** box shown in Fig. 11-15. If you are using



Save And Quit

Save Session File: OLS\PROJECTS\TRYSPECCTRA\SpecctraWithinLayout.ses

☐ Delete Did File:

Figure 11-15 Save the SES file to transfer the file back to Layout.

the Demo version you will not be able to save the .SES file and the transfer will not be completed.

If the .SES file were saved then the board routed by SPECCTRA would be automatically transferred into Layout (the example from Fig. 11-14 is shown in Fig. 11-16). You can then save the design with the existing file name and .MAX extension.

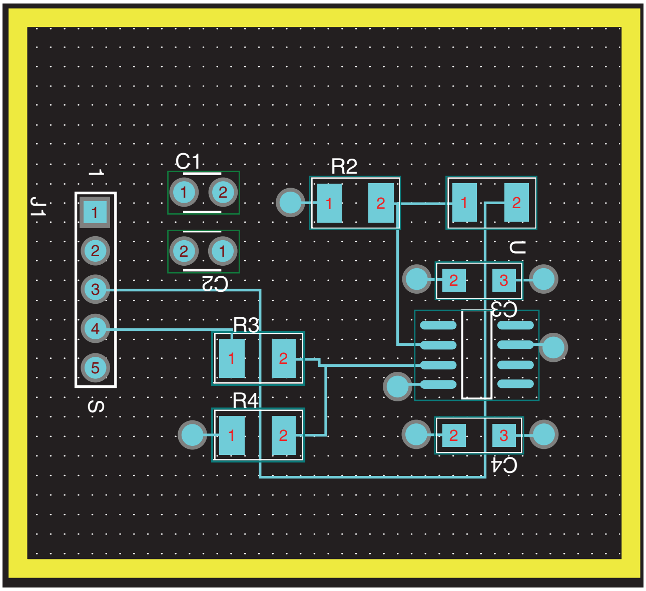


Figure 11-16 The SPECCTRA-routed board in Layout.

Additional information on how to use SPECCTRA is included in the *Allegro PCB Router User's Guide* (spug.pdf) located in the OrCAD doc folder. As such only a few manual routing tips are presented here. Placing parts and routing traces are performed from two different window views. To place parts select the Place Mode view by clicking the Place Mode button, , located on the left side of the toolbar (see Fig. 11-17). To route nets select the route mode view by clicking the Route Mode button, , also located on the left side of the toolbar (see Fig. 11-18).

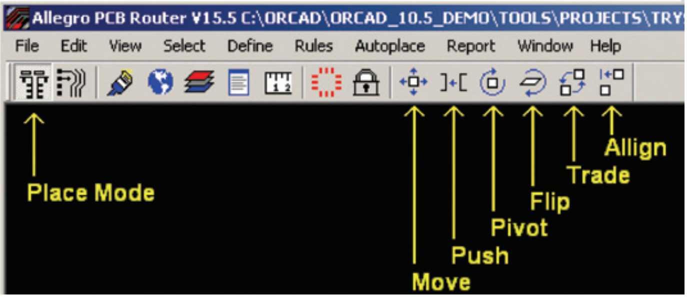

Allegro PCB Router V15.5 C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TRY
File
Edit
View
Select
Define
Rules
Autoplace
Report
Window
Help
Place Mode
Allign
Trade
Flip
Pivot
Push
Move

Figure 11-17 SPECCTRA Place Mode view.

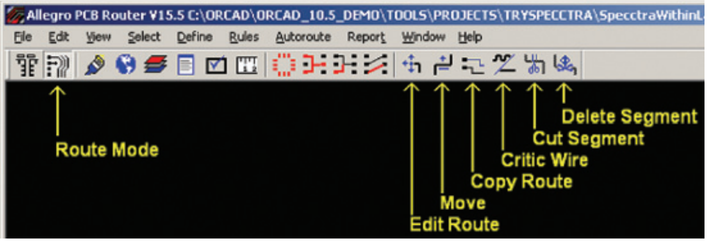

Allegro PCB Router V15.5 C:\ORCAD\ORCAD_10.5_DEMO\TOOLS\PROJECTS\TRYSPECCTRA\SpecctraWithinL
File
Edit
View
Select
Define
Rules
Autoroute
Report
Window
Help
Route Mode
Delete Segment
Cut Segment
Critic Wire
Copy Route
Move
Edit Route

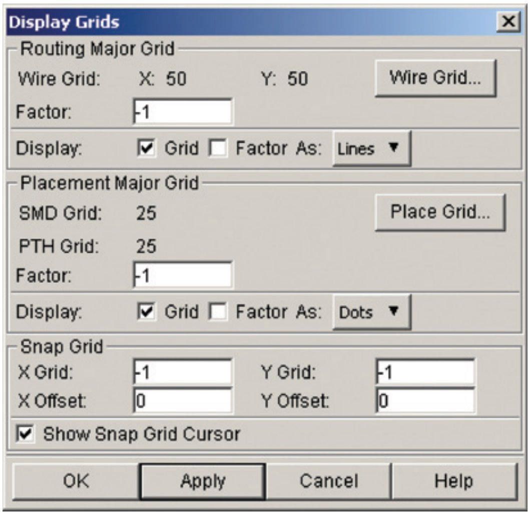
Figure 11-18 SPECCTRA Route Mode view.

To move a part in Place Mode click the Select Component button, , and then click the Move Component button, . Left click a component to select it, and then left click again to place it. The other Place Component tools are shown in Fig. 11-17.

To route a net in Route Mode click the Edit Route button, . Move the cursor (a + symbol) to a pad or vertex. The cursor will become a pencil and allow you to select a wire to route. Left click a wire to begin routing. Left click to place vertices and continue routing. To quit routing left click on a pad or another routed trace, or right click and select Done from the pop-up. The other manual routing tools are shown in Fig. 11-18.

As with Layout there are many layers associated with the PCB. Unlike Layout, which uses spreadsheets to access many of the layers, you access layers in SPECCTRA with the Layer control panel. To display the layer control panel click the Layers button, .

There are separate grids for placement, routing, and vias. You can control the grids using the Display Grids dialog box by selecting Display Grids from the View menu (Fig. 11-19).



Display Grids

Routing Major Grid

Wire Grid: X: 50 Y: 50

Factor: -1

Display: ☑ Grid ☐ Factor As: Lines

Placement Major Grid

SMD Grid: 25

PTH Grid: 25

Factor: -1

Display: ☑ Grid ☐ Factor As: Dots

Snap Grid

X Grid: -1 Y Grid: -1

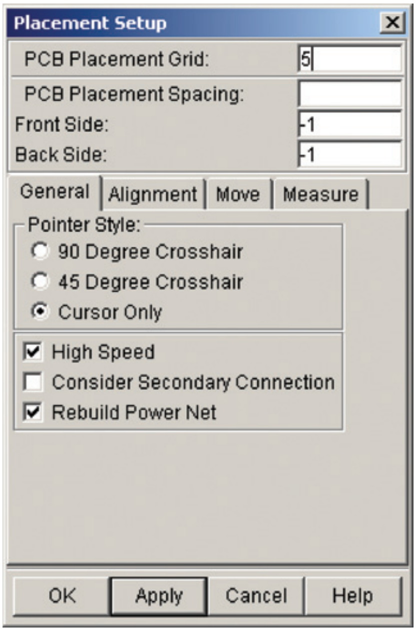
X Offset: 0 Y Offset: 0

☑ Show Snap Grid Cursor

Wire Grid...
Place Grid...
OK
Apply
Cancel
Help

*Figure 11-19 The **Display Grids** dialog box.*

The place grid set with the **Display Grids** dialog box is visual only. To set the actual placement grid select the **Place Mode** button and then select **Setup…** from the **Autoplace** menu. Select the desired place grid setting in the **Placement Setup** dialog box (see Fig. 11-20) and click **Apply.**



Placement Setup

PCB Placement Grid: 5

PCB Placement Spacing:

Front Side: -1

Back Side: -1

Pointer Style:

○ 90 Degree Crosshair

○ 45 Degree Crosshair

● Cursor Only

☑ High Speed

☐ Consider Secondary Connection

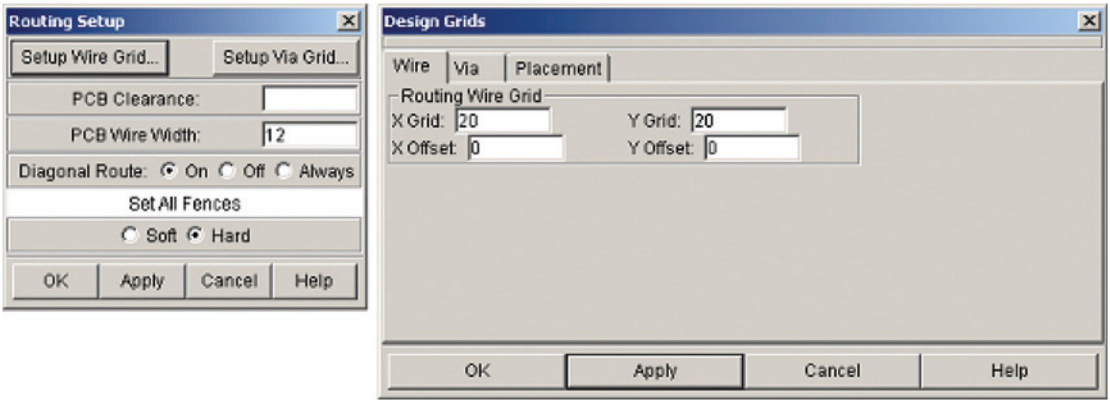
☑ Rebuild Power Net

General
Alignment
Move
Measure
OK
Apply
Cancel
Help

*Figure 11-20 **Placement Setup** dialog box.*

To set an actual route grid, select the Route Mode and select Setup… from the Autoroute menu. Use the dialog boxes shown in Fig. 11-21 to set the wire and via grids.

Those are the basics of SPECCTRA and are all that will be discussed here. For more information on SPECCTRA see the *Allegro PCB Router User's Guide* (SPECCTRA user's guide, spug.pdf) and the Allegro PCB Router Tutorial (SPECCTRA tutorial, sptut.pdf) in the documents folder.



PCB Clearance:

PCB Wire Width: 12

Diagonal Route: ● On ○ Off ○ Always

Set All Fences

○ Soft ● Hard

X Grid: 20 Y Grid: 20

X Offset: 0 Y Offset: 0

Figure 11-21 Route grid dialog boxes.

Introduction to GerbTool

GerbTool is a computer-aided manufacturing tool. It is not used for routing but is used as a postprocessing tool. When you postprocess your board design with Layout a .GTD file is created along with the other Gerber files discussed in Chap. 10. GerbTool can open and operate on the .GTD file. GerbTool can be used to work with a PCB design with regard to apertures, composites, embedded passives, and penalization, to name a few. In this section GerbTool will be used to demonstrate how to set up a drill file for a CNC machine and how to panelize a PCB design generated from Layout.

A demo version of GerbTool is included with the full version of Layout but not with the Demo version of Layout. You can download the latest demo version of GerbTool from WISE Software's Web site. The *GerbTool User Manual* (laygtug.pdf) is included with both the demo and the full version of OrCAD in the OrCAD documents folder.

Opening a Layout-generated Gerber file with GerbTool

After you have completed your PCB design and postprocessed it with Layout, you can start GerbTool from within Layout by going to the main Layout session frame (not the Design window) and selecting GerbTool → Open from the Tools menu. If you are using the Demo version of Layout, start GerbTool from Windows as you normally start other programs.

Once GerbTool is up and running, open a Gerber design (.GTD) file by selecting Open from the File menu. Several example files are included with GerbTool; the design file TryGerber-2.gtd on the CD included with this book is used here and is shown in Fig. 11-22.

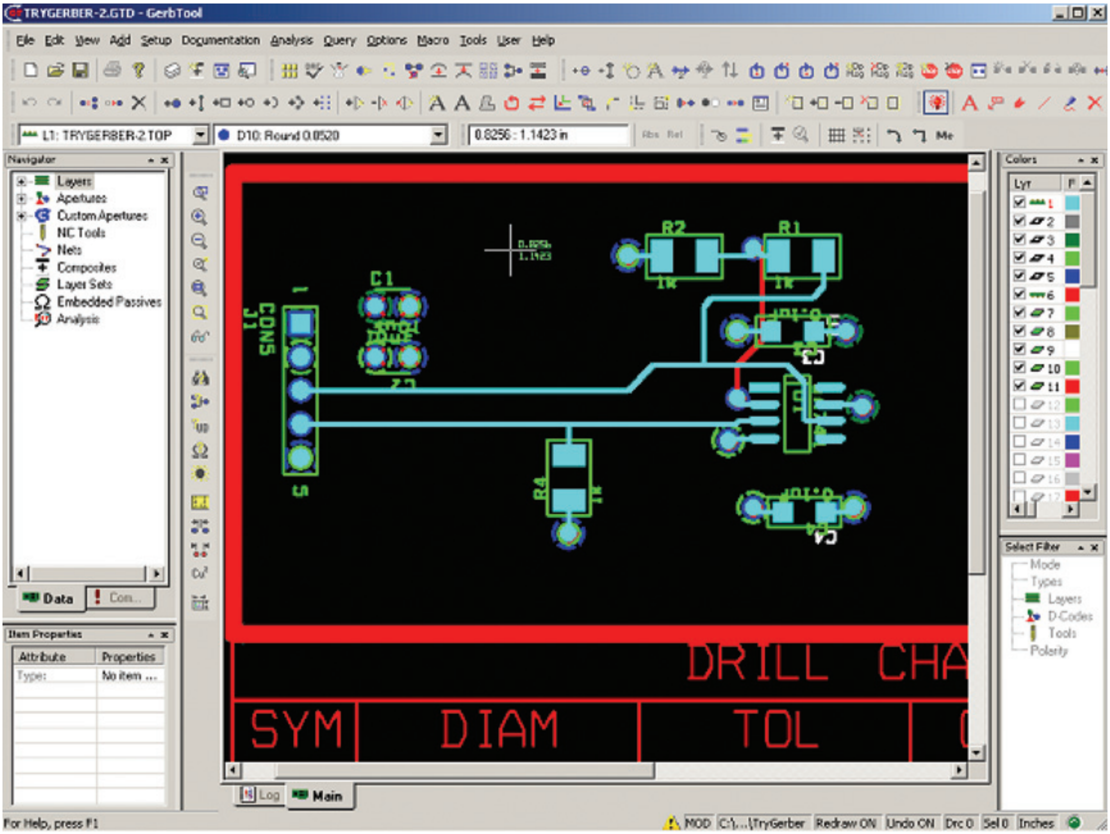

TRYGERBER-2.GTD - GerbTool
File Edit View Add Setup Documentation Analysis Query Options Macro Tools User Help
L1: TRYGERBER-2.TOP
D10: Round 0.0520
0.8256 : 1.1423 in
Navigator
Layers
Apertures
Custom Apertures
NC Tools
Nets
Composites
Layer Sets
Embedded Passives
Analysis
Data
Con...
Item Properties
Attribute
Properties
Type:
No item ...
Colors
Lyr
Select Filter
Mode
Types
Layers
D-Codes
Tools
Polarity
R2
R1
C1
J1
CONS
R4
DRILL CHA
SYM
DIAM
TOL
Log
Main
For Help, press F1
MOD
C:\...\TryGerber
Redraw ON
Undo ON
Drc 0
Sel 0
Inches

Figure 11-22 A .GTD file opened with GerbTool.

Making a .DRL file for a CNC machine

Drill information is included with the .DRD file generated by the postprocessing step in Layout, but some CNC files require a specific file (a .DRL file) that contains drill information and format that are in the thruhole.tap file for their programming. A .DRL can be generated by Layout, but only in the older Gerber format. In this example GerbTool will be used to convert the thruhole.tap file from the Excelon format into a .DRL file.

Look at the active layers in the Layer dropdown list as shown in Fig. 11-23. These are the Gerber files that Layout generated during postprocessing. Note, however, that the thruhole.tap layer is not listed. Notice that the .DRL layer is not listed either. The basic process is to add a drill layer, make it the active layer, and then import the thruhole.tap data into the drill layer.

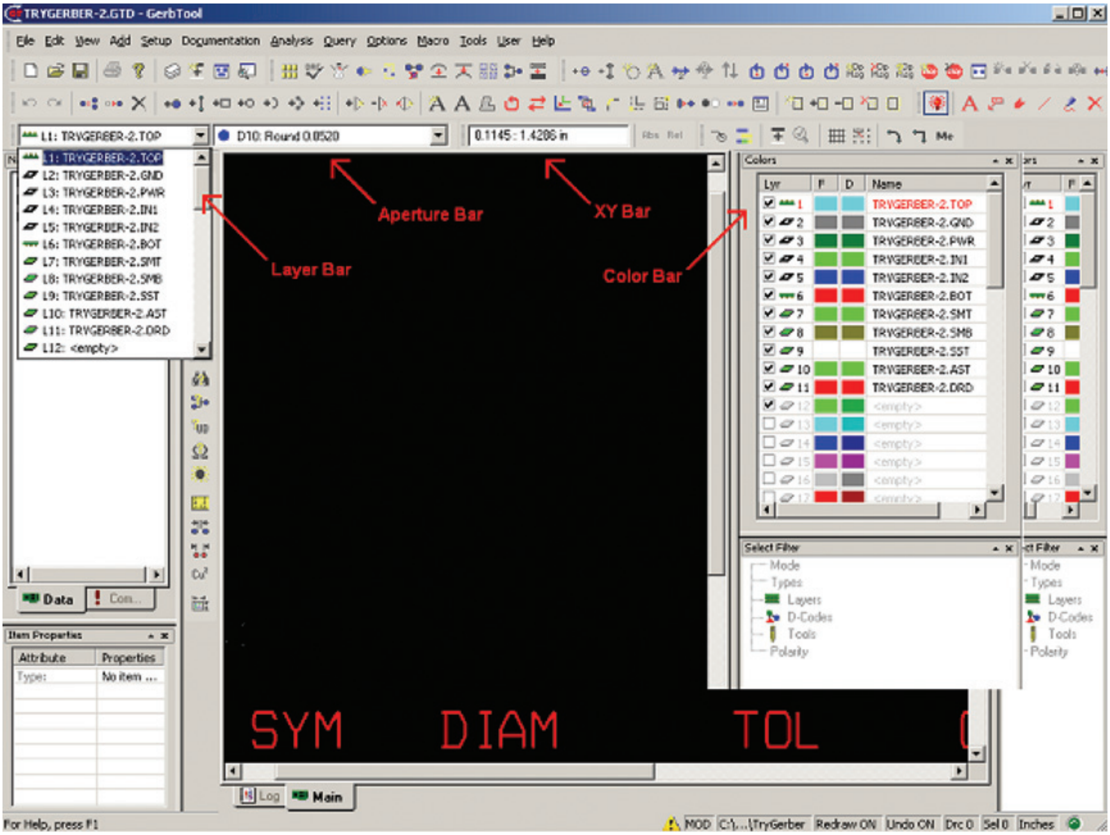

TRYGERBER-2.GTD - GerbTool
File Edit View Add Setup Documentation Analysis Query Options Macro Tools User Help
L1: TRYGERBER-2.TOP
D10: Round 0.0520
0.1145 : 1.4286 in
Aperture Bar
XY Bar
Layer Bar
Color Bar
L1: TRYGERBER-2.TOP
L2: TRYGERBER-2.GND
L3: TRYGERBER-2.PWR
L4: TRYGERBER-2.IN1
L5: TRYGERBER-2.IN2
L6: TRYGERBER-2.BOT
L7: TRYGERBER-2.SMT
L8: TRYGERBER-2.SMB
L9: TRYGERBER-2.SST
L10: TRYGERBER-2.AST
L11: TRYGERBER-2.DRD
L12: <empty>
Colors
Lyr
F
D
Name
Select Filter
Mode
Types
Layers
D-Codes
Tools
Polarity
Item Properties
Attribute
Properties
Type:
No item ...
Data
Com...
SYM
DIAM
TOL
Log
Main
For Help, press F1
MOD
C:\...\TryGerber
Redraw ON
Undo ON
Drc 0
Sel 0
Inches

Figure 11-23 GerbTool toolbars.

To make a drill layer make the first available <empty> layer active by selecting it from the Layer toolbar. Go to Setup → Layers on the dropdown menu or press the Setup Layers button on the toolbar as shown in Fig. 11-24. The Layer Setup control box is shown in Fig. 11-25.

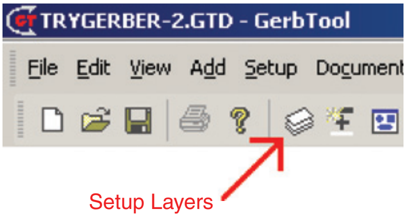
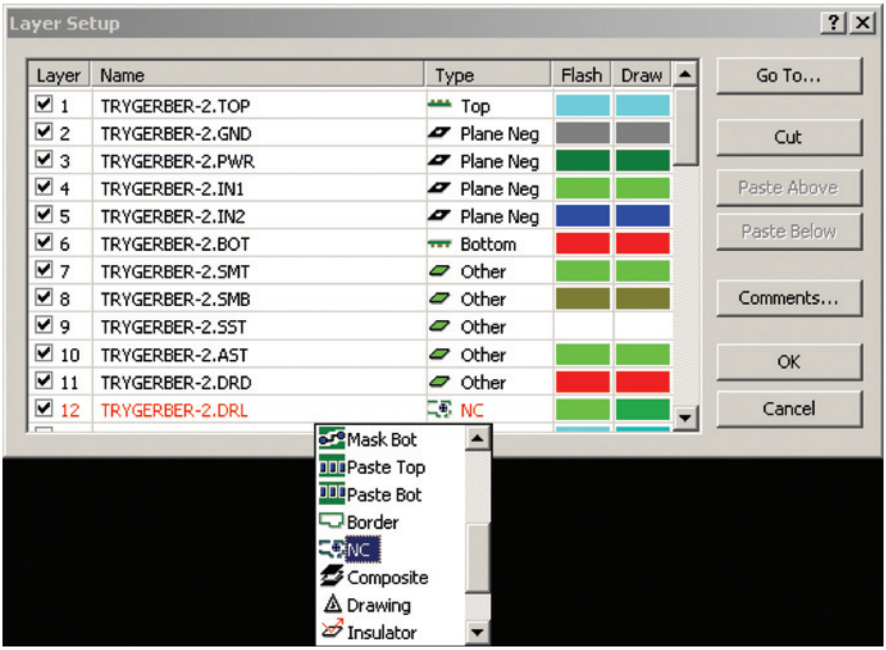

TRYGERBER-2.GTD - GerbTool
File Edit View Add Setup Document
Setup Layers

Figure 11-24 **Setup Layers** toolbar button.


Layer Setup
? ×
Go To…
Cut
Paste Above
Paste Below
Comments…
OK
Cancel
Mask Bot
Paste Top
Paste Bot
Border
NC
Composite
Drawing
Insulator

Layer	Name	Type	Flash	Draw
☑ 1	TRYGERBER-2.TOP	Top	🟦	🟦
☑ 2	TRYGERBER-2.GND	Plane Neg	⬛	⬛
☑ 3	TRYGERBER-2.PWR	Plane Neg	🟩	🟩
☑ 4	TRYGERBER-2.IN1	Plane Neg	🟩	🟩
☑ 5	TRYGERBER-2.IN2	Plane Neg	🟦	🟦
☑ 6	TRYGERBER-2.BOT	Bottom	🟥	🟥
☑ 7	TRYGERBER-2.SMT	Other	🟩	🟩
☑ 8	TRYGERBER-2.SMB	Other	🟫	🟫
☑ 9	TRYGERBER-2.SST	Other	⬜	⬜
☑ 10	TRYGERBER-2.AST	Other	🟩	🟩
☑ 11	TRYGERBER-2.DRD	Other	🟥	🟥
☑ 12	TRYGERBER-2.DRL	NC	🟩	🟩

Figure 11-25 Drill layer creation and setup.

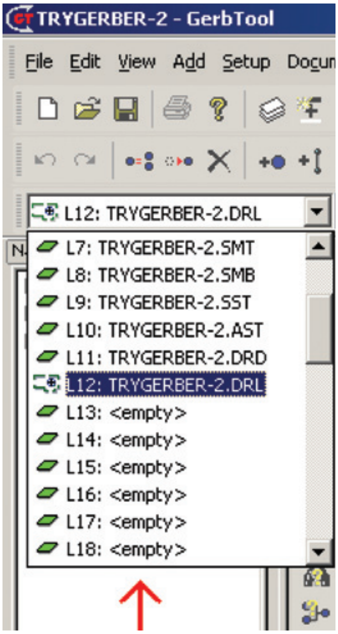

TRYGERBER-2 - GerbTool
File
Edit
View
Add
Setup
Docu
L12: TRYGERBER-2.DRL
L7: TRYGERBER-2.SMT
L8: TRYGERBER-2.SMB
L9: TRYGERBER-2.SST
L10: TRYGERBER-2.AST
L11: TRYGERBER-2.DRD
L12: TRYGERBER-2.DRL
L13: <empty>
L14: <empty>
L15: <empty>
L16: <empty>
L17: <empty>
L18: <empty>

Figure 11-26 Making a layer the active layer.

In the Layer Setup control box (Fig. 11-25) the drill layer will not initially be present. Left click inside the empty Name box after the empty cell and type the name of your file followed by ".DRL" to name the drill layer (see line 12 in Fig. 11-25). Hit the Enter key on your keyboard to display the Layer Type selection list. Next, select NC (for NC drill), and make sure to set Visibility to ON (with the check mark). You can also change the colors if you want. Click OK.

Next, make the DRL layer active by selecting the Layer selection list and select the .DRL layer to make it active (see Fig. 11-26).

Once you have the DRL layer set up and active, import the thruhole.tap data into it by navigating to File → Import → Drill from the menu bar as shown in Fig. 11-27. In the open file dialog box (see Fig. 11-28) make sure you have the All Files(*.*) option selected in the Files of Type: box and navigate to the folder where your thruhole.tap file is located. Select it and click Open.

Next, you will need to set the drill format in the NC Import Data Format dialog box that pops up as shown in Fig. 11-29. To find out which m.n setting to use open the Gerber Preferences dialog box in Layout (Options → Gerber Settings…). The m.n setting

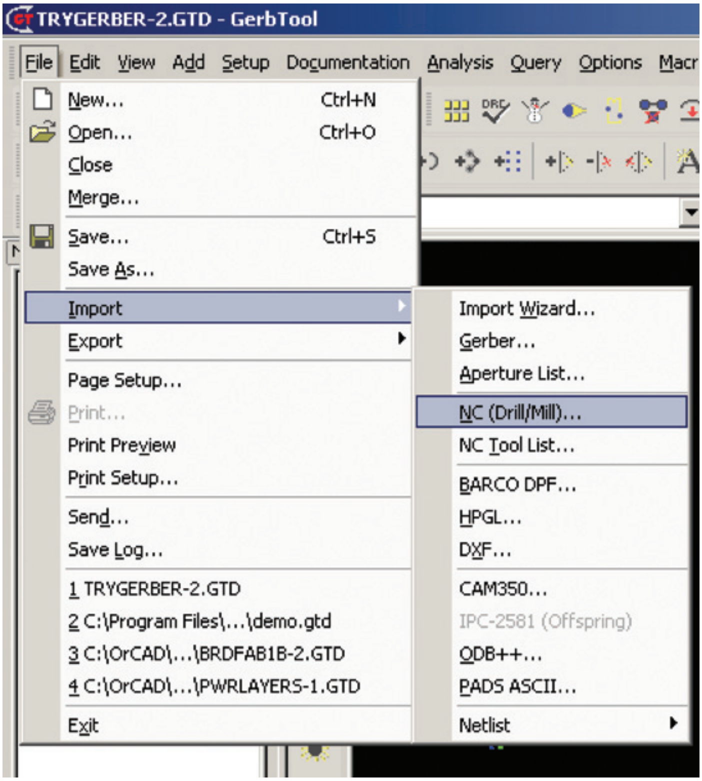
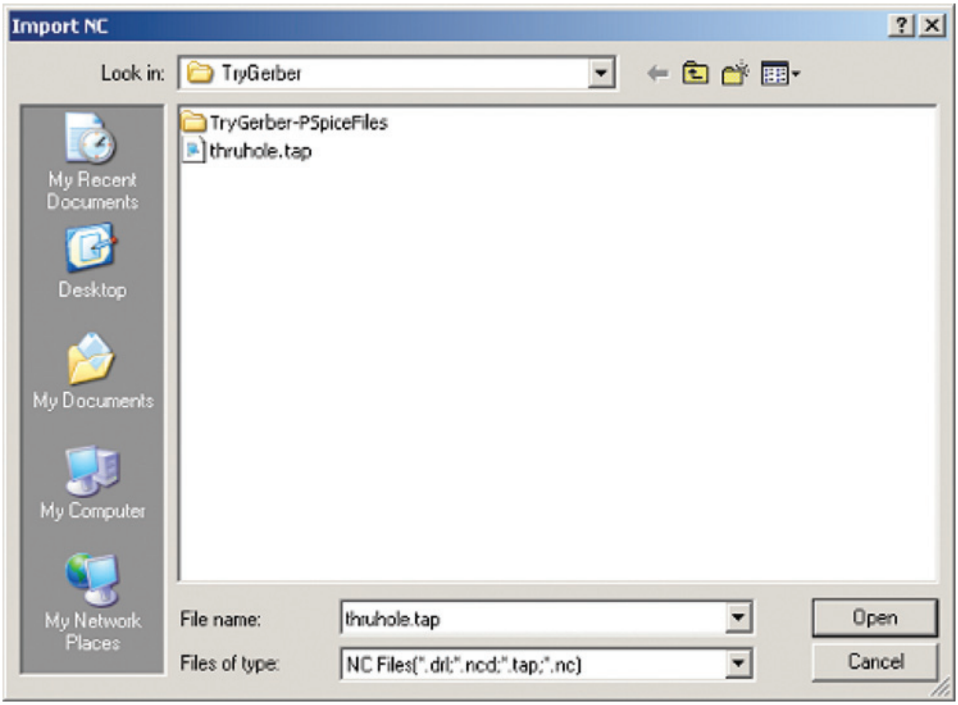

TRYGERBER-2.GTD - GerbTool
File
Edit
View
Add
Setup
Documentation
Analysis
Query
Options
Macr
New… Ctrl+N
Open… Ctrl+O
Close
Merge…
Save… Ctrl+S
Save As…
Import
Export
Page Setup…
Print…
Print Preview
Print Setup…
Send…
Save Log…
1 TRYGERBER-2.GTD
2 C:\Program Files\…\demo.gtd
3 C:\OrCAD\…\BRDFAB1B-2.GTD
4 C:\OrCAD\…\PWRLAYERS-1.GTD
Exit
Import Wizard…
Gerber…
Aperture List…
NC (Drill/Mill)…
NC Tool List…
BARCO DPF…
HPGL…
DXF…
CAM350…
IPC-2581 (Offspring)
ODB++…
PADS ASCII…
Netlist

Figure 11-27 Import drill data.



Look in: TryGerber

TryGerber-PSpiceFiles

thruhole.tap

File name: thruhole.tap

Files of type: NC Files(*.drl;*.ncd;*.tap;*.nc)

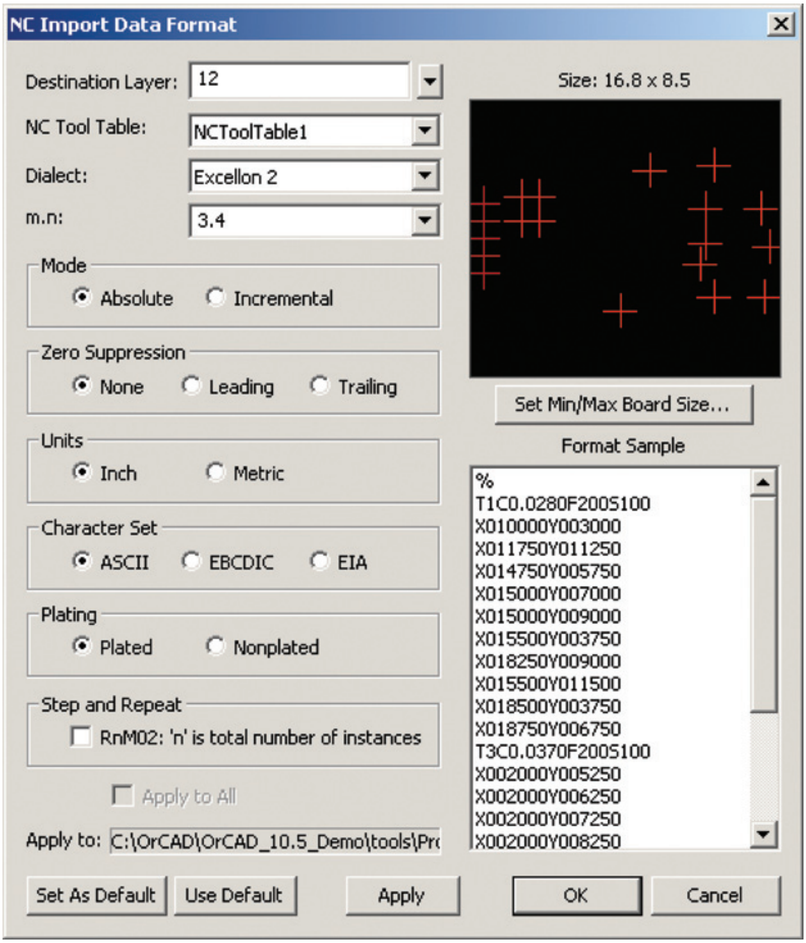
Figure 11-28 Look for thruhole.tap drill file.

in GerbTool should match the Output Resolution setting as indicated by the arrow in Fig. 11-30. Click OK.

Back at the design view in GerbTool (Fig. 11-31), verify that the drill data were imported correctly by noticing that the drill symbols (filled circles with crosses through them) are located in the correct places. If they are not correct it will be very obvious as the drill holes will be scaled up or down by several factors.

If you need to undo the import, select Undo from the Edit menu to display the Undo selection box shown in Fig. 11-32. Select the item you want undone and click OK. You can then repeat the process to redo the import steps above.

At this point there is a drill layer in the *.GTD file, but there is not a Gerber file for it yet. To make a Gerber drill file, you need to export the drill layer you just set up. To generate a Gerber drill file select File → Export → Drill from the toolbar. The Export dialog box will pop up as shown in Fig. 11-33. Although the file name will be correct in the Output and Report File boxes, you need to click the Browse button to make sure that the files go to the folder you want. The default path is whatever it was the last time an export was performed. Also make sure that the *.DRL layer is selected. The proper Export NC data format is determined by the CNC machine used. The format shown in the figure is an example of one type of machine’s requirements. The new .DRL can now be used with the CNC machine.



NC Import Data Format

Destination Layer: 12
NC Tool Table: NCToolTable1
Dialect: Excellon 2
m.n: 3.4

Mode: ● Absolute ○ Incremental
Zero Suppression: ● None ○ Leading ○ Trailing
Units: ● Inch ○ Metric
Character Set: ● ASCII ○ EBCDIC ○ EIA
Plating: ● Plated ○ Nonplated
Step and Repeat: ☐ RnM02: 'n' is total number of instances
☐ Apply to All
Apply to: C:\OrCAD\OrCAD_10.5_Demo\tools\Pr

Size: 16.8 x 8.5

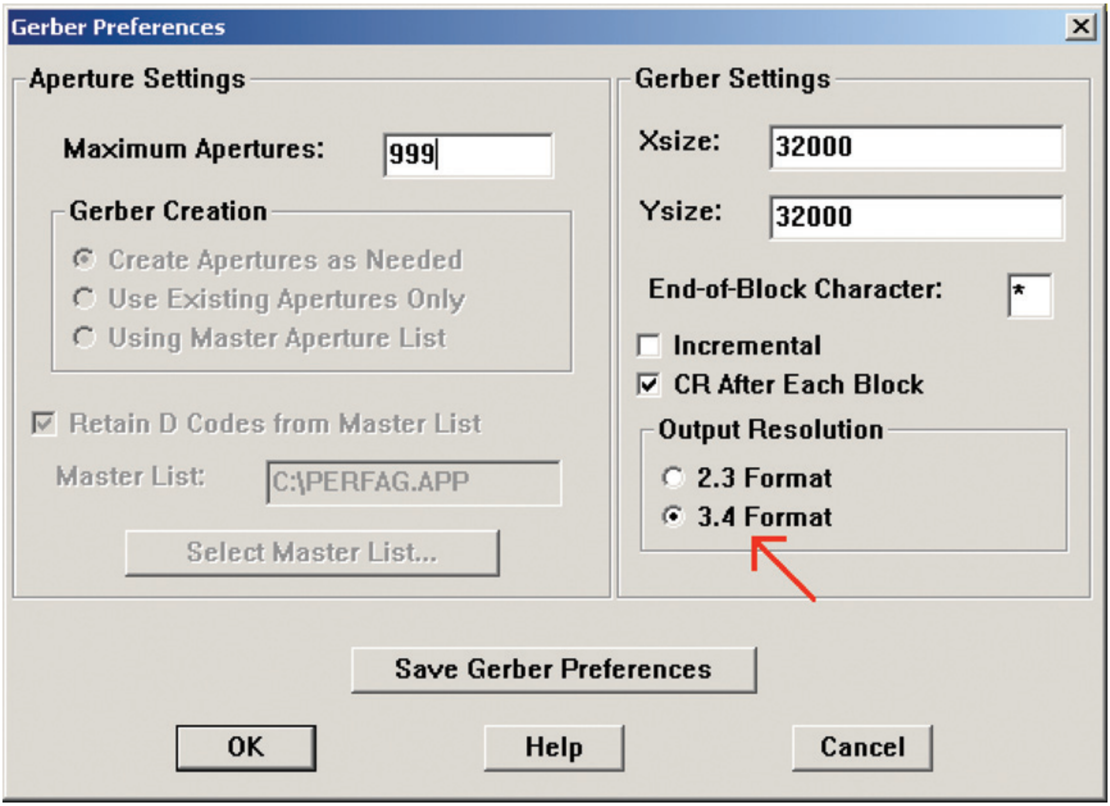
Format Sample

```
%
T1C0.0280F200S100
X010000Y003000
X011750Y011250
X014750Y005750
X015000Y007000
X015000Y009000
X015500Y003750
X018250Y009000
X015500Y011500
X018500Y003750
X018750Y006750
T3C0.0370F200S100
X002000Y005250
X002000Y006250
X002000Y007250
X002000Y008250
```

Figure 11-29 **Import Data Format** dialog box.

Panelization

When PCBs are too small they are not able to be assembled and soldered with standard processes such as pick-and-place machinery and wave soldering stations. The only way to be able to handle them in that case is to leave the small, individual PCBs attached to each other in large panels; this is called panelization. The arrayed PCBs can be handled as larger units, allowing them to be easily mass fabricated, populated, and soldered using standard processes. The panels are either tab-routed as in Fig. 11-34(a) or V-scored as in Fig. 11-34(b) so that when the assembly processes are complete the individual pieces can be snapped apart. With tab-routing small slivers of the panel are removed with a router bit and the individual PCBs are held together with the remaining tabs. With V-scoring a V-shaped groove is cut partway


Gerber Preferences

Aperture Settings

Maximum Apertures: 999

Gerber Creation

● Create Apertures as Needed
○ Use Existing Apertures Only
○ Using Master Aperture List

☑ Retain D Codes from Master List

Master List: C:\PERFAG.APP

Gerber Settings

Xsize: 32000

Ysize: 32000

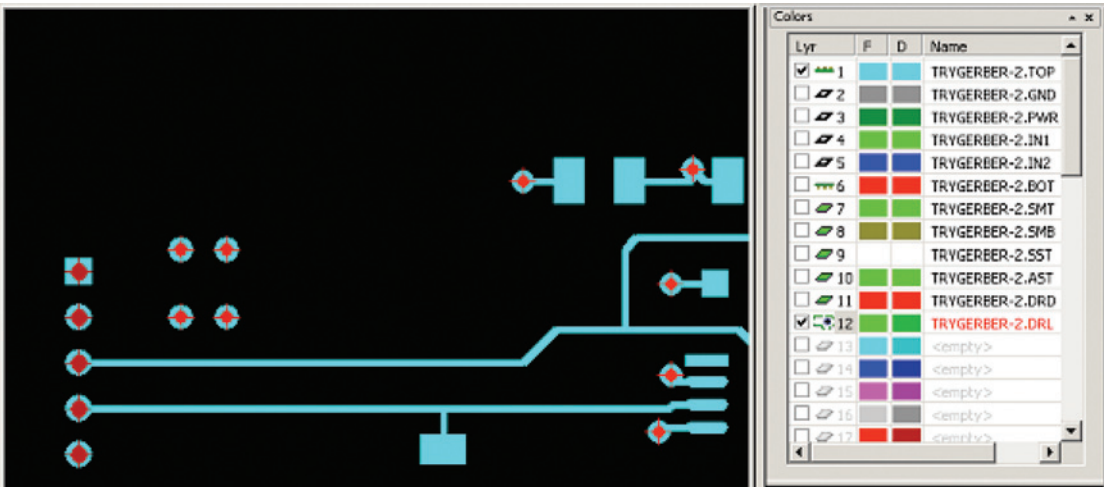
End-of-Block Character: *

☐ Incremental
☑ CR After Each Block

Output Resolution

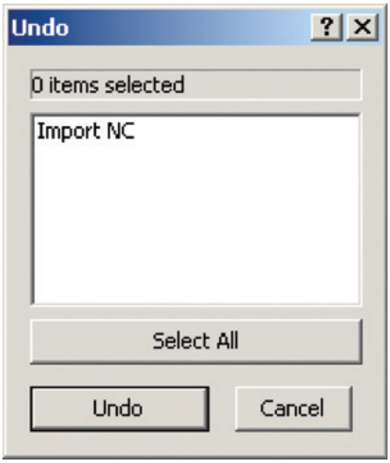
○ 2.3 Format
● 3.4 Format

Figure 11-30 Gerber settings in Layout.



Lyr	F	D	Name
☑ 1	🟦	🟦	TRYGERBER-2.TOP
☐ 2	⬛	⬛	TRYGERBER-2.GND
☐ 3	🟩	🟩	TRYGERBER-2.PWR
☐ 4	🟩	🟩	TRYGERBER-2.IN1
☐ 5	🟦	🟦	TRYGERBER-2.IN2
☐ 6	🟥	🟥	TRYGERBER-2.BOT
☐ 7	🟩	🟩	TRYGERBER-2.SMT
☐ 8	🟫	🟫	TRYGERBER-2.SMB
☐ 9	⬜	⬜	TRYGERBER-2.SST
☐ 10	🟩	🟩	TRYGERBER-2.AST
☐ 11	🟥	🟥	TRYGERBER-2.DRD
☑ 12	🟩	🟩	TRYGERBER-2.DRL
☐ 13	🟦	🟦	<empty>
☐ 14	🟦	🟦	<empty>
☐ 15	🟪	🟪	<empty>
☐ 16	⬜	⬛	<empty>
☐ 17	🟥	🟥	<empty>

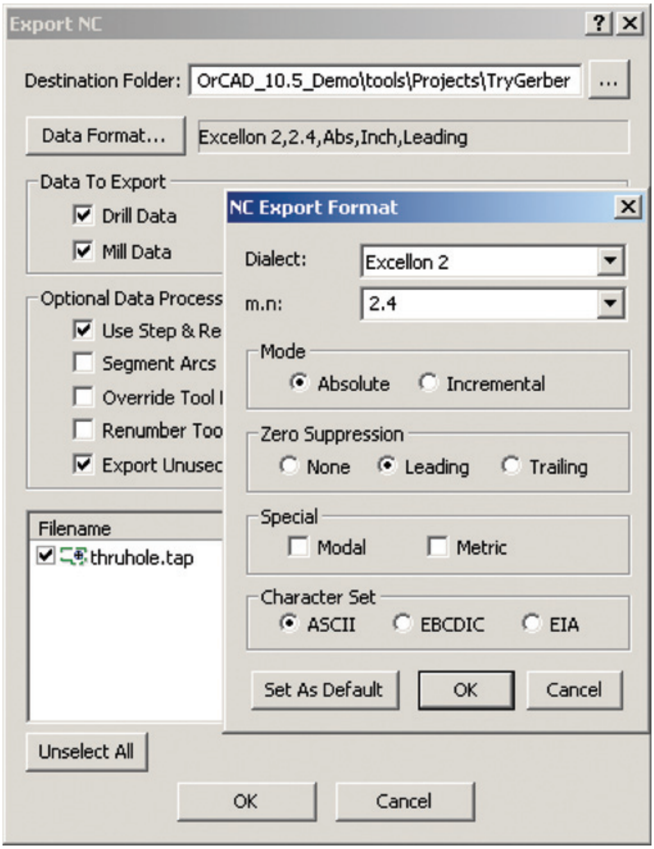
Figure 11-31 The design file with the imported drill data.


Undo
?
Select All
Undo
Cancel

0 items selected

Import NC

Figure 11-32 Edit undo.


Export NC
?
...
Data Format...
NC Export Format
Set As Default
OK
Cancel
Unselect All
OK
Cancel

Destination Folder: OrCAD_10.5_Demo\tools\Projects\TryGerber

Excellon 2,2.4,Abs,Inch,Leading

Data To Export
☑ Drill Data
☑ Mill Data

Optional Data Process
☑ Use Step & Re
☐ Segment Arcs
☐ Override Tool I
☐ Renumber Too
☑ Export Unusec

Filename
☑ thruhole.tap

Dialect: Excellon 2

m.n: 2.4

Mode
● Absolute ○ Incremental

Zero Suppression
○ None ● Leading ○ Trailing

Special
☐ Modal ☐ Metric

Character Set
● ASCII ○ EBCDIC ○ EIA

Figure 11-33 **Export NC** dialog box.

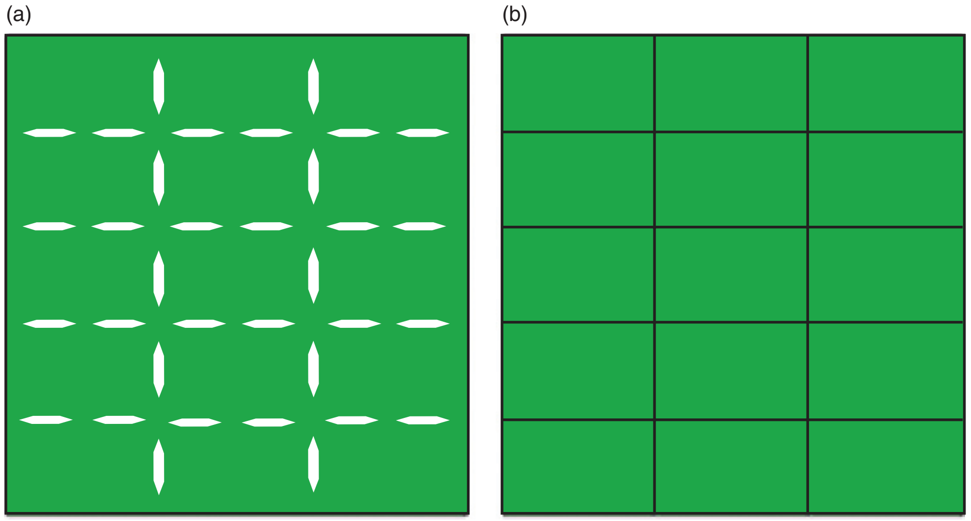


Figure 11-34 Panelized PCBs. (a) Tab-routed. (b) V-scored.

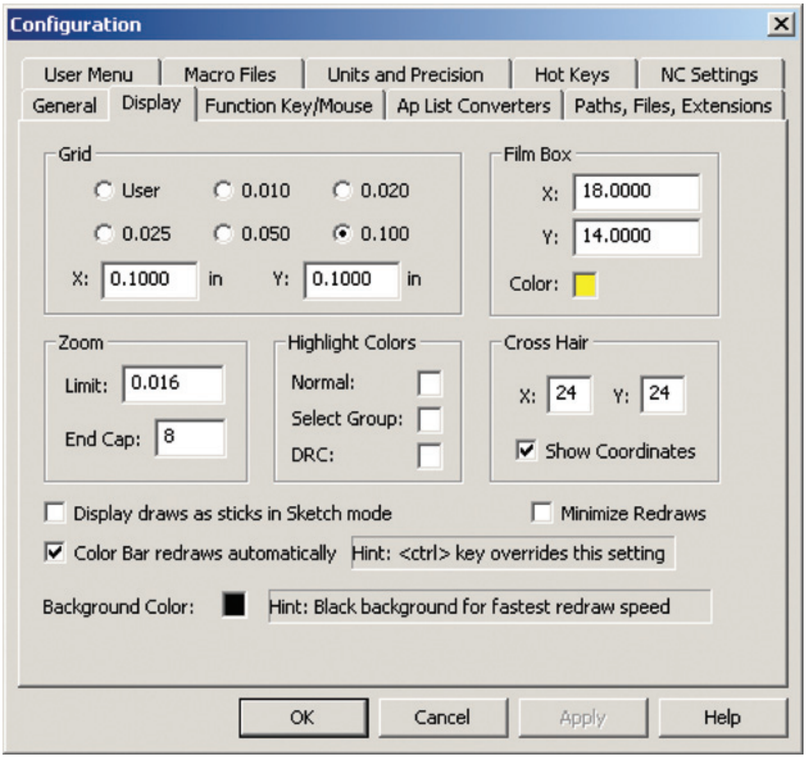
into the panel from one or both sides of the panel over its full length. Tab-routing requires about 100 mils spacing between the PCB edges, and V-scoring requires about 10 to 20 mils spacing between individual PCB edges, depending on the capabilities and preferences of your board manufacturer.

Note

- *The following example provides only a very basic demonstration of how to panelized a PCB design. Please contact your board manufacturer to determine their panelization requirements and refer to the GerbTool User Manual for specific instructions on how to perform panelization.*

Layout does not provide a means of panelizing PCBs, but GerbTool does. **To panelize a PCB** postprocess the PCB design in Layout as you normally would. Then start GerbTool and open the .GTD file. Import drill files if needed (see above) and install any required milling instructions (see the *GerbTool User Manual*).

The first step is to define the panel size (see Chap. 4 for details on standard panel sizes). A panel size is defined by GerbTool with a film box. **To change the film box (panel) size** chose Options → Configure to display the Configuration dialog box. Click the Display tab (see Fig. 11-35). Set the X: and Y: parameters in the Film Box group as desired and click OK. To see the entire film box select Film Box from the View menu.



Grid
○ User ○ 0.010 ○ 0.020
○ 0.025 ○ 0.050 ● 0.100
X: 0.1000 in Y: 0.1000 in

Film Box
X: 18.0000
Y: 14.0000
Color: 🟨

Zoom
Limit: 0.016
End Cap: 8

Highlight Colors
Normal: ☐
Select Group: ☐
DRC: ☐

Cross Hair
X: 24 Y: 24
☑ Show Coordinates

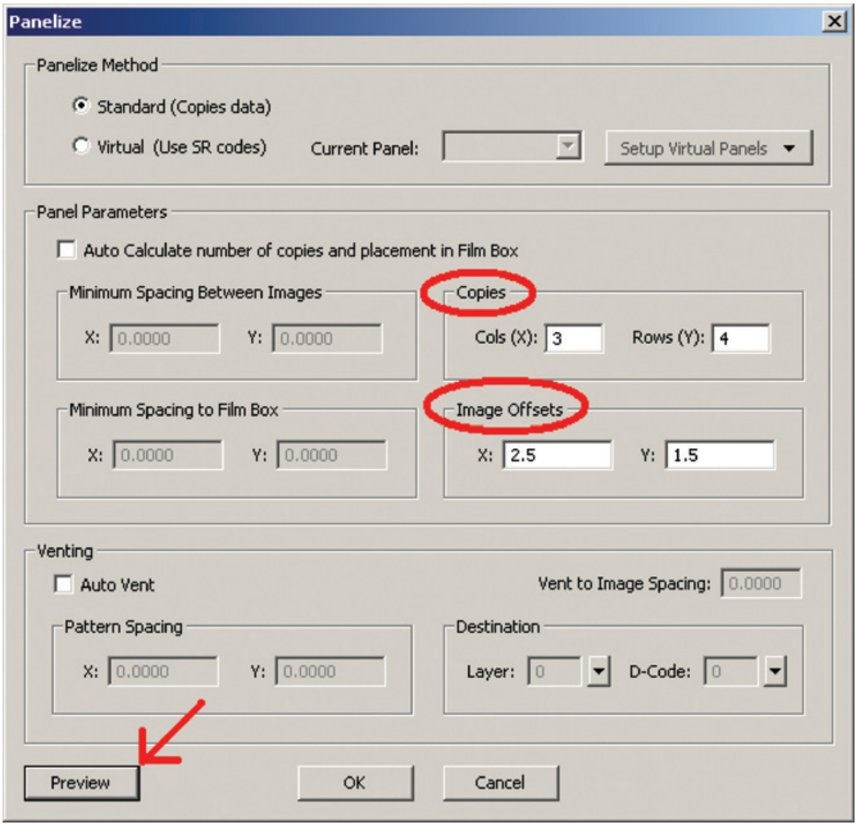
☐ Display draws as sticks in Sketch mode
☐ Minimize Redraws
☑ Color Bar redraws automatically
Hint: <ctrl> key overrides this setting
Background Color: ⬛
Hint: Black background for fastest redraw speed

Figure 11-35 Change film box size.

There are two methods of panelizing a design: advanced and simple. The simple method will be demonstrated here (see the *GerbTool User Manual* for information on the advanced method). **To panelize the design** choose Tools → Panelize → Simple… from the menu bar. The Panelize dialog box (Fig. 11-36) will be displayed. For this simple example set the parameters as shown in the figure. The image offsets are the size of the master board outline plus any extra spacing you want between the boards. You can click the Preview button to see what the panelized board will look like. Click OK.

After you click OK, GerbTool will ask you to define the boundaries of the area to panelize. At the lower left corner of the window the message “Panelize: enter first point…” will be displayed. Left click the origin of the board outline as shown in Fig. 11-37. GerbTool will then ask for the second point and display “Panelize: enter second point.…” Click the other end of the board outline as shown in the figure.

When GerbTool asks: “Document Panelize/Vent parameters?” you can select Yes or No; it does not matter for this example. The finished panel is shown in Fig. 11-38. Only the basics of panelizing a board were presented here. Please see the *GerbTool User Manual* for additional details and contact your board manufacturer to find out their requirements and needs for panelizing boards.



Panelize

Panelize Method

● Standard (Copies data)

○ Virtual (Use SR codes)

Current Panel:

Panel Parameters

☐ Auto Calculate number of copies and placement in Film Box

Minimum Spacing Between Images

X: 0.0000 Y: 0.0000

Copies

Cols (X): 3 Rows (Y): 4

Minimum Spacing to Film Box

X: 0.0000 Y: 0.0000

Image Offsets

X: 2.5 Y: 1.5

Venting

☐ Auto Vent

Vent to Image Spacing: 0.0000

Pattern Spacing

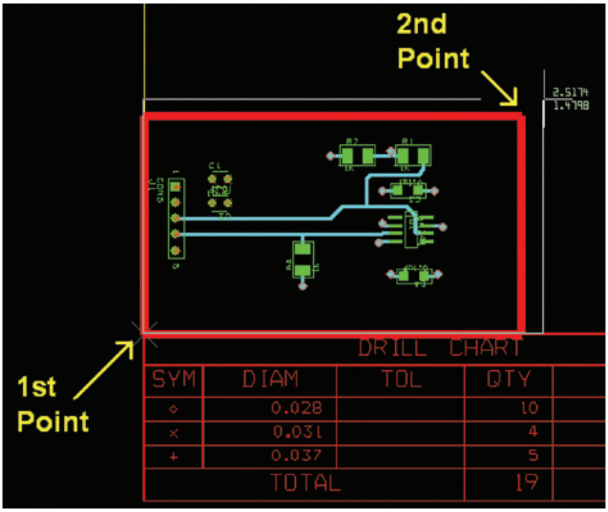
X: 0.0000 Y: 0.0000

Destination

Layer: 0 D-Code: 0

Setup Virtual Panels
Preview
OK
Cancel

Figure 11-36 The **Panelize** dialog box.



2nd Point
2.5174
1.4798
1st Point

DRILL CHART

SYM	DIAM	TOL	QTY
◇	0.028		10
×	0.031		4
+	0.037		5
TOTAL			19

Figure 11-37 Selecting the board outline to panelize.

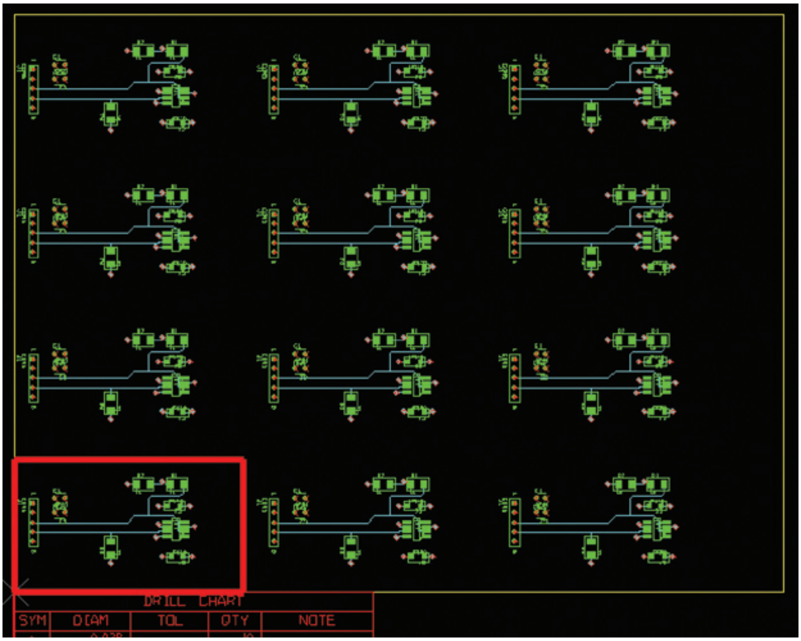


Figure 11-38 The panelized board design.

You can save the new panelized design as a .GTD file, but the Gerber files need to be updated in order to fabricate the board. **To update the Gerber files** select Export → Gerber from the File menu. From the Export dialog box you can select the data format and location of the new Gerber files (saving and exporting are disabled in the Demo version).

Using the IPC-7351 Land Pattern Viewer

The IPC Land Pattern viewer is an indispensable tool for designing footprints. The viewer provides drawings and dimensions of hundreds of footprints that are based on established standards. You can download a freeware version of the software from the IPC Web site at http://www.ipc.org. From the home page look under the Knowledge tab and then click on the PCB Tools and Calculators link. On the next page click on the IPC-7351 Land Pattern Viewer and Tools link. From the next page, click the IPC-7351 Land Pattern Viewer—Version X.xxx (.zip) link (where X.xxx is the latest version).

Once you have downloaded and installed the viewer you can immediately run the application without restarting Windows. When you first open the viewer you will be presented with an application window as shown in Fig. 11-39. Click the Master Library Search button to begin looking for footprints.

The first step is to select a library from the Search Library: selection list (see Fig. 11-40). Four libraries are included by default. You can download some additional free libraries and

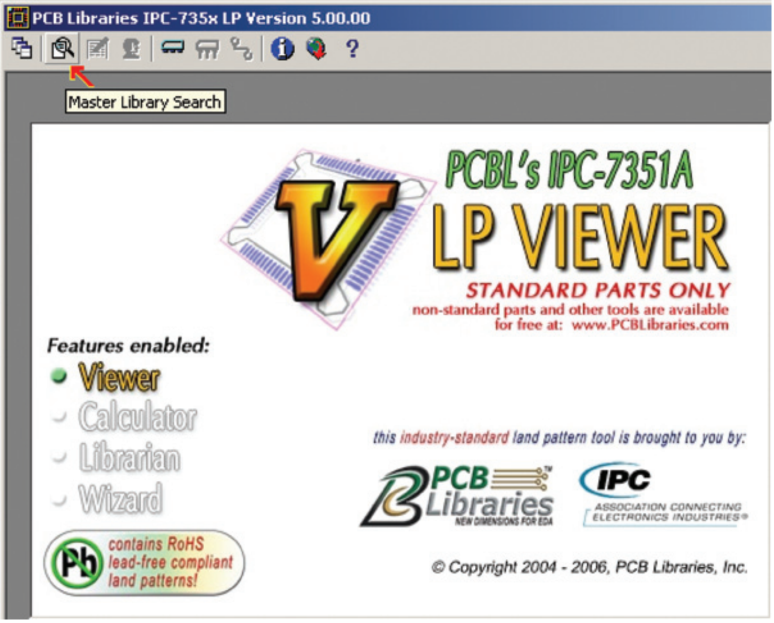
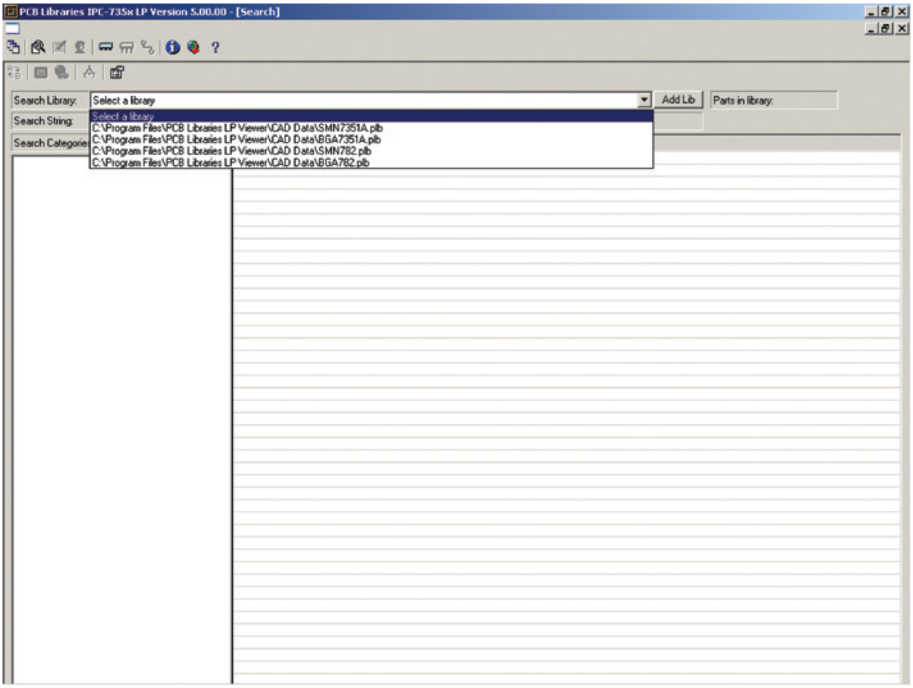

PCB Libraries IPC-735x LP Version 5.00.00
Master Library Search
PCBL's IPC-7351A
LP VIEWER
STANDARD PARTS ONLY
non-standard parts and other tools are available
for free at: www.PCBLibraries.com
Features enabled:
Viewer
Calculator
Librarian
Wizard
contains RoHS
lead-free compliant
land patterns!
this industry-standard land pattern tool is brought to you by:
PCB Libraries
NEW DIMENSIONS FOR EDA
IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES
© Copyright 2004 - 2006, PCB Libraries, Inc.

Figure 11-39 Initial view of the IPC-7351 Land Pattern viewer application.


PCB Libraries IPC-735x LP Version 5.00.00 - [Search]
Search Library:
Add Lib
Parts in library:
Search String:
Search Categorie

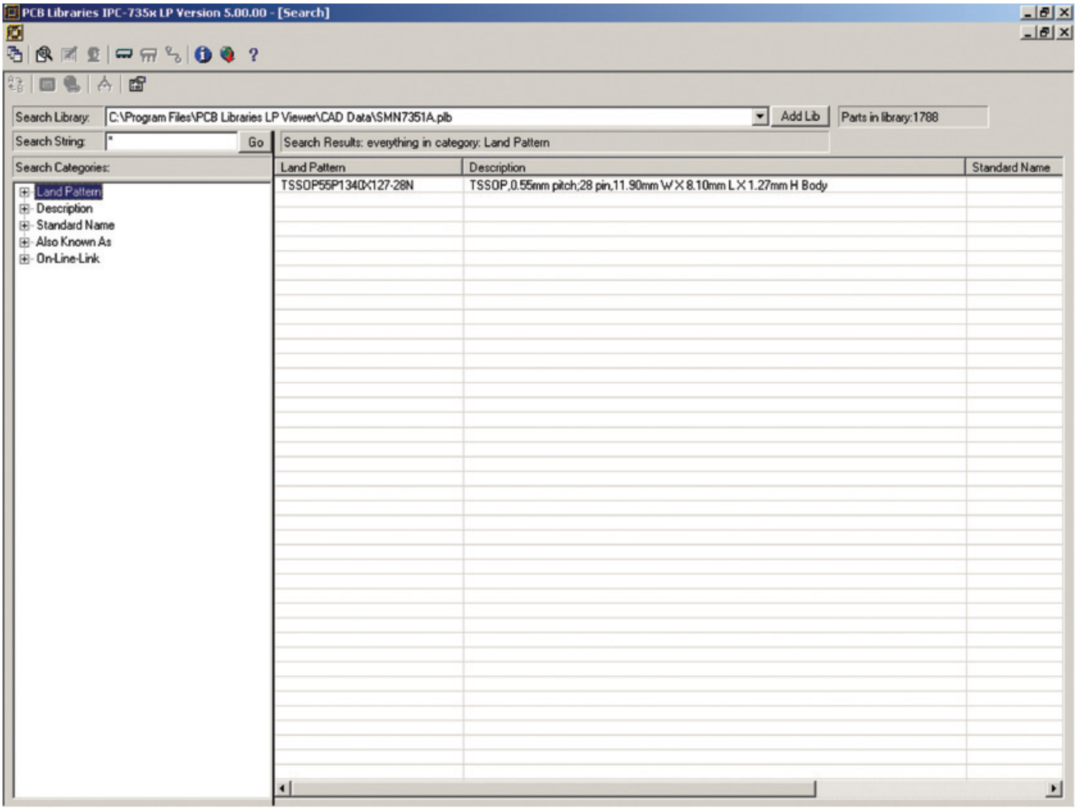
Select a library

Select a library
C:\Program Files\PCB Libraries LP Viewer\CAD Data\SMN7351A.plb
C:\Program Files\PCB Libraries LP Viewer\CAD Data\BGA7351A.plb
C:\Program Files\PCB Libraries LP Viewer\CAD Data\SMN782.plb
C:\Program Files\PCB Libraries LP Viewer\CAD Data\BGA782.plb

Figure 11-40 Selecting a library.

for-fee libraries from the IPC Web site through PCBLibraries.com. The SM**N**7351A.plb library (included with the viewer) contains footprints for most of the discrete and IC packages on the market with nominal outline and pad dimensions. Footprints with tighter tolerances (least i.e. smaller features) are in the SM**L**7351A.plb library and footprints with larger (most) features are in the SM**M**7351A.plb library, both of which can be downloaded from the Web site.

Once you have selected a library, five search modes will be listed under the Search Categories: pane. Click a "+" box to expand a category (see Fig. 11-41). Regardless of which category you select the same information is contained in the search results (for the most part), but footprints are listed differently within each category. The most noticeable difference is the Standard Name category. Rather than listing the footprints by package names they are listed by industry standard document numbers (e.g., JEDEC MO-187 or MIL-PRF-xxx).



Search Library: C:\Program Files\PCB Libraries LP Viewer\CAD Data\SMN7351A.plb

Parts in library:1788

Search String: *

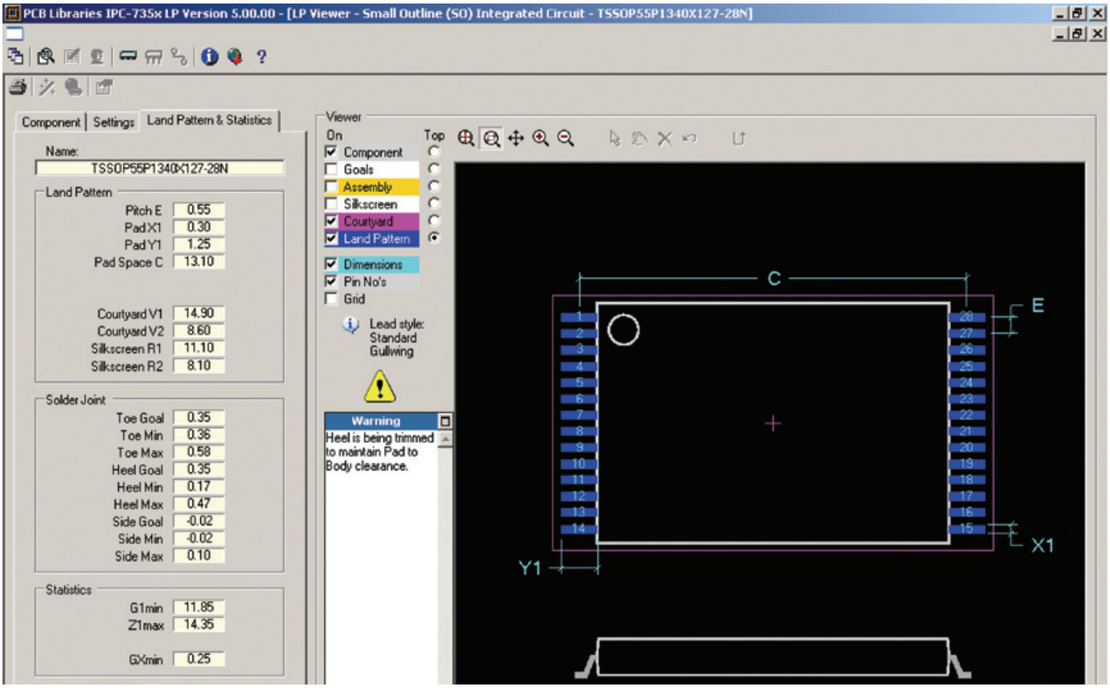
Search Results: everything in category: Land Pattern

Land Pattern	Description	Standard Name
TSSOP55P1340X127-28N	TSSOP,0.55mm pitch;28 pin,11.90mm W X 8.10mm L X 1.27mm H Body	

Figure 11-41 Selecting a search category.

Once you have found the package name, description, or standard in the Search Categories: list, double click the package to display it (and its variations) in the Search Results: window.

Double click a land pattern to display the package view window as shown in Fig. 11-42. By selecting the Component, Settings, and Land Pattern & Statistics tabs along with the Viewer radio buttons, you can find out every detail about a package's dimensions, including the suggested pad sizes and spacing, silk-screen sizes, etc.



PCB Libraries IPC-735x LP Version 5.00.00 - [LP Viewer - Small Outline (SO) Integrated Circuit - TSSOP55P1340X127-28N]

Component | Settings | Land Pattern & Statistics

Name: TSSOP55P1340X127-28N

Land Pattern
Pitch E 0.55
Pad X1 0.30
Pad Y1 1.25
Pad Space C 13.10
Courtyard V1 14.90
Courtyard V2 8.60
Silkscreen R1 11.10
Silkscreen R2 8.10

Solder Joint
Toe Goal 0.35
Toe Min 0.36
Toe Max 0.58
Heel Goal 0.35
Heel Min 0.17
Heel Max 0.47
Side Goal -0.02
Side Min -0.02
Side Max 0.10

Statistics
G1min 11.85
Z1max 14.35
GXmin 0.25

Viewer
On | Top
☑ Component ○
☐ Goals ○
☐ Assembly ○
☐ Silkscreen ○
☑ Courtyard ○
☑ Land Pattern ●
☑ Dimensions
☑ Pin No's
☐ Grid

Lead style:
Standard
Gullwing

Warning
Heel is being trimmed to maintain Pad to Body clearance.

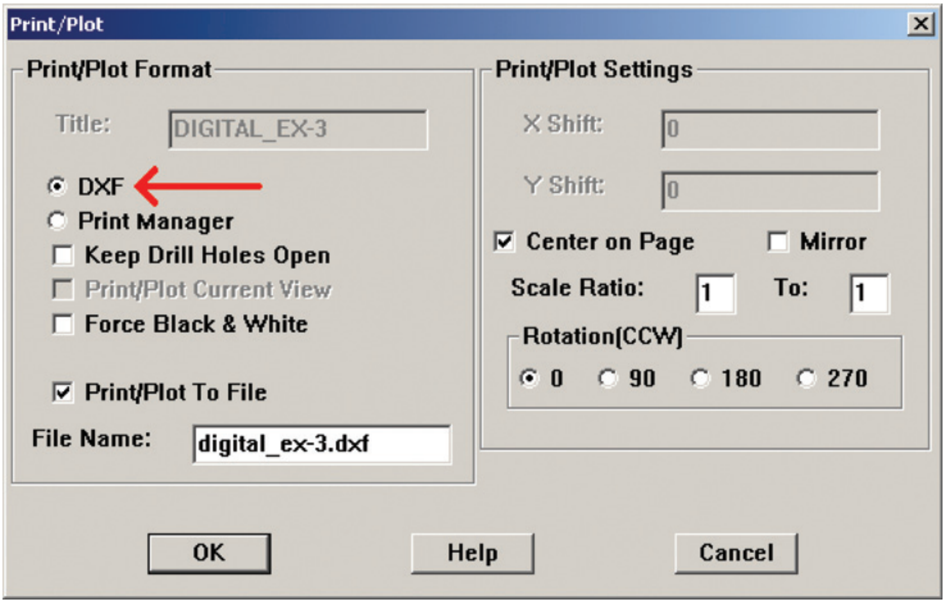
Figure 11-42 Viewing a footprint land pattern.

Using CAD Tools to 3-D Model a PCB

Before you send the Gerber files off to the board house to be manufactured you might want to know if the board will be physically compatible with its mounting hardware (i.e., "Will it fit?"). You can export the design information from Layout's .MAX file to a .DXF file, which you can open with most popular CAD drawing packages.

Graphically speaking there is a tremendous amount of information in the .MAX file, a lot of which does not need to be exported to a drawing file. To select layers to plot use the Layer selection list. Any layers you see on the display will be plotted.

To export a PCB design as a .DXF file, from within Layout, select Print/Plot from the File menu to display the Print/Plot dialog box (Fig. 11-43). Select the DXF radio button, choose a name, and click OK. That is all there is to it.


Print/Plot

Print/Plot Format

Title: DIGITAL_EX-3

● DXF
○ Print Manager
☐ Keep Drill Holes Open
☐ Print/Plot Current View
☐ Force Black & White

☑ Print/Plot To File

File Name: digital_ex-3.dxf

Print/Plot Settings

X Shift: 0

Y Shift: 0

☑ Center on Page ☐ Mirror

Scale Ratio: 1 To: 1

Rotation(CCW)

● 0 ○ 90 ○ 180 ○ 270

*Figure 11-43 Using **Print/Plot** to create CAD drawing data.*

The digital design board from Chap. 9 is shown in Fig. 11-44 with only the board outline and place outlines (default (global layer), place outline (global layer), and place outline (TOP)) layers active. Figure 11-45 shows a 3-D-rendered model of the same information using a popular drawing program (the colors were modified with the CAD program). Dimensions and other manufacturing information can easily be added to the drawing file to fully describe manufacturing and assembly instructions.

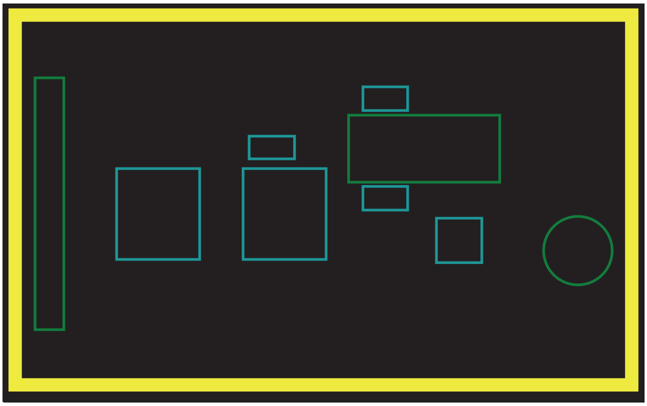


Figure 11-44 Flat board representation in Layout.

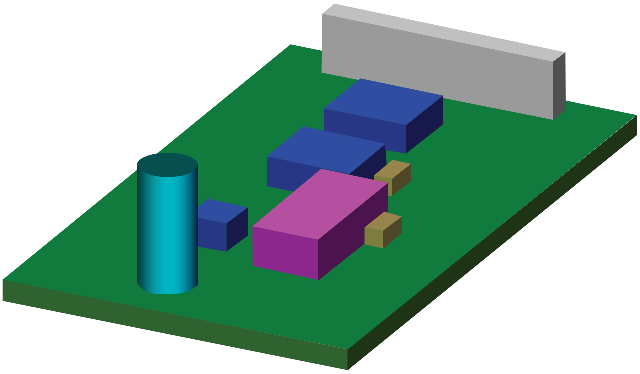


Figure 11-45 3-D CAD model of the PCB.

Appendix A

Layout Technology Files

Usage	**Technology files (*.TCH)**	**Design complexity level/class**	**Units**	**Trace width**	**Route spacing**	**System settings Grid settings (mills)**			**Default via size**			**Layers provided**		**Default board outline**
						Place	**Routing**	**Via**	**Route**	**Plane**	**Drill**	**Route**	**Plane**	
Typical	_default	A	Mils	12	12	100	25	25	50	75	28	12	2	None
	default	A	Mils	12	12	100	25	25	50	75	28	12	2	None
	1bet_any	A	Mils	12	12	100	25	25	50	75	28	12	2	None
	2bet_smt	B	Mils	8	8	100	$8\frac{1}{3}$	$8\frac{1}{3}$	40	70	20	12	2	None
	2bet_thr	B	Mils	10	8	100	20	20	40	70	20	12	2	None
	3bet_any	C	Mils	6	6	100	$12\frac{1}{2}$	$12\frac{1}{2}$	36	70	20	12	2	None
	metric	B	Metric	0.254	0.254	1.27	0.254	0.254	0.762	1.524	0.381	12	2	None
Chip package	ceramic	B	Metric	0.25/0.28	0.254	1.27	0.254	0.254	0.762	1.524	0.381	12	2	None
	hybrid	B	Metric	0.25/0.28	0.254	1.27	0.254	0.254	0.762	1.524	0.381	12	2	None
	mcm	B	Metric	0.25/0.28	0.254	1.27	0.254	0.254	0.762	1.524	0.381	12	2	None
Jumper	jump5535	A	Mils	12	12	100	25	25	55	70	35	12	2	None
	jump6035	A	Mils	12	12	100	25	25	60	70	35	12	2	None
	jump6238	A	Mils	12	12	100	25	25	62	70	38	12	2	None

(Continued)

Usage	Technology files (*.TCH)	Design complexity level/class	Units	Trace width	Route spacing	System settings Grid settings (mills)			Default via size			Layers provided		Default board outline
						Place	Routing	Via	Route	Plane	Drill	Route	Plane	
Translators/ other	386lib	A	Mils	12	12/8 (ext/int)	100	25	0	50	75	28	13	3	6.0 × 6.0
	cadstar	A	Mils	12	12	100	25	25	50	75	28	12	2	None
	p99se	A	Mils	12	12, 10 (rtg, pln)	100	25	25	50	75	28	12	4	None
	pads	A	Mils	12	12	100	25	25	50	75	28	14	2	None
	pcad	A	Mils	12	12	100	25	25	50	75	28	12	2	None
	protel	A	Mils	12	12	100	25	25	50	75	28	12	4	None
	tango	A	Mils	12	12	100	25	25	50	75	28	12	2	None
	tutor	A	Mils	12	12	100	25	25	50	75	28	12	2	4.6 × 3.0

Appendix B

List of Design Standards

ANSI Standards

ANSI B94.11-197 (see also ASME B94.1 IM-1993), Twist Drills

ANSI Y32.2-1975 (see also IEEE Std 315-1975), Graphic Symbols for Electrical and Electronics Diagrams

ASME Standards

B18.2.8–1999, Clearance Holes for Bolts, Screws, and Studs

B18.6.3–2003, Machine Screws and Machine Screw Nuts

ASA 618.11-1961, Miniature Screws

Y 14.5M, Dimensioning and Tolerancing

ASME B94.1 IM-1993, Twist Drills

IEEE Standards

IEEE Std 315-1975 (ANSI Y32.2-1975), Graphic Symbols for Electrical and Electronics Diagrams

IPC Standards

IPC-1902/IEC 60097, Grid Systems for Printed Circuits

IPC-2141, Controlled Impedance Circuit Boards and High-Speed Logic Design

IPC-2221A, Generic Standard on Printed Board Design

IPC-2222, Sectional Design Standard for Rigid Organic Printed Boards

IPC-2223A, Sectional Design Standard for Flexible Printed Boards

IPC-2224, Sectional Standard for Design of PWBs for PC Cards

IPC-2225, Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

IPC-2226, Sectional Design Standard for High-Density Interconnect (HDI) Printed Boards

IPC-2251, Design Guide for the Packaging of High-Speed Electronic Circuits

IPC-2515A, Sectional Requirements for Implementation of Bare Board Product Electrical Testing Data Description [BDTST]

IPC-2615, Printed Board Dimensions and Tolerances

IPC-4101A, Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-7351, Generic Requirements for Surface-Mount Design and Land Pattern Standard

IPC-9252, Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-A-600G, Acceptability of Printed Boards

IPC-A-610, Acceptability of Electronic Assemblies

IPC-HDBK-610, Handbook and Guide to IPC-A-610

IPC-CM-770E, Guidelines for Printed Board Component Mounting

IPC-D-322, Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes

IPC-D-350, Printed Board Description in Digital Form

IPC-D-356B, Bare Substrate Electrical Test Data Format

IPC/JPCA-2315, Design Guide for High-Density Interconnects (HDI) and Microvias

IPC/JPCA-6801, Terms and Definitions, Test Methods, and Design Examples for Built-Up/ High-Density Interconnect (HDI) Printed Wiring Boards

IPC-SM-780, Component Packaging and Interconnecting with Emphasis on Surface Mounting

IPC/WHMA-A-620, Requirements and Acceptance for Cable and Wire Harness Assemblies

JEDEC Standards

Master Index for JEDEC Publication No. 95 (see also Appendix C for specific standards)

MIL-STD

MIL-HDBK-198A, Capacitors, Selection and Use of

MIL-HDBK-199A, Resistors, Selection and Use of

MIL-HDBK-5961A, List of Standard Semiconductor Devices

MIL-STD-1276G, Leads for Electronic Component Parts

MIL-STD 275E, Printed Wiring for Electronic Equipment (superceded by IPC-2221A)

Appendix C

A Partial List of Packages and Footprints and Some of the Footprints Included in OrCAD Layout

Abbreviation	Full name
BDIP (SDIP)	Butt-mounted dual inline package (surface DIP, std pitch)
BGA	Ball grid array
BQFP	Bumper quad flat package
CBGA	Ceramic column ball grid array
CFP	Ceramic flat packages
CGA	Column grid array
CQFP	Ceramic quad flat packages
DIMM	Dual inline memory module
DIP	Dual inline package
DO	Diode outline
DPAK	Discrete packaging (type 1, TO-252)
D2PAK	Discrete packaging (type 2, TO-263)
D3PAK	Discrete packaging (type 3, TO-268)
LCC/LCCS	Leadless chip carrier/leadless ceramic chip carrier
LGA	Land grid array
MELF	Metal electrode face
MSOP	Micro (mini) small outline package
MLP	Micro leadframe package (no lead)
PGA	Pin grid array
PLCC	Plastic leaded chip carriers
PLCCR	Plastic leaded chip carriers rectangular
PLCCS	Plastic leaded chip carriers square
PQFP	Plastic quad flat package
QBCC	Quad bottom chip carrier
QFP	Quad flat packages
QFN (QFPNL)	Quad flat no lead package

Table C-1 A List of Package Abbreviations (Continued)

Abbreviation	Full name
QLCCC	Quad leadless ceramic chip carrier (see LCC/LCCS)
SIMM	Single inline memory module
SDIP	Shrink dual inline package
SOD	Small outline discrete (or diode)
SOIC (SOJ)	Small outline integrated circuit, J-lead
SOIC (SOG)	Small outline integrated circuit, gull wing
SON	Small outline nonleaded
SOP	Small outline package
SOT	Small outline transistor
SSOT	Shrink small outline transistor
SQFP	Shrink quad flat package
SSOP	Shrink small outline package
TO	Transistor outline
TQFP	Thin quad flat package
TSOP	Thin small outline package
TSSOP	Thin shrink small outline package

Table C-1 (Continued)

Name or type	Name, case, or size	Standards	Layout	
			Library	Footprint
Resistor, chip	0402, 0805, 1206, etc.	IEC 60115-B, JIS C 5201-B, EIAJ RC-2134B	SM.LLB	SM/R 0805, SM/R_1206, etc.
Capacitor, chip	0402, 0805, 1206, etc.	MIL-PRF-55681	SM.LLB	SM/C_0805, SM/C_1206, etc.
Capacitor, tantalum (molded)	A	EIA 3216-18	SM.LLB	SM/CT_3216, SM/CT_3216_12
	B	EIA 3528-21		SM/CT_3528, SM/CT_3528_12
	C	EIA 6032-28		SM/CT_6032, SM/CT_6032_12
	D	EIA 7343-31		SM/CT_7343, SM/CT_7343_12
	E	EIA 7260-38		—
	R	EIA 2012-12		—
	T	EIA 3528-12		—
	V	EIA 7343-20		—
	X	EIA 7343-43		—
	Y	EIA 7343-40		—
MELF (DL-41, LL-34)	Metal electrode face	EIC 10H01, LL-34	SM.LLB	SM/D_MLL34, SM/D_MLL41 (+variations)
SOD, SC-76 (molded)	Small outline diode	JEDEC DO215-D, EIAJ SC-76, EIAJ SC-76	SM.LLB	SM/D_SOD87 (+variations)
SMA (molded)	SMT diode outline	JEDEC DO214-D (variation AC)	SM.LLB	SM/DO214 (AA, AB, AC; +variations)
SMB (molded)	SMT diode outline	JEDEC DO214-D (variation AA)	SM.LLB	SM/DO214 (AA, AB, AC; +variations)
SMC (molded)	SMT diode outline	JEDEC DO214-D (variation AB)	SM.LLB	SM/DO214 (AA, AB, AC; +variations)
DO-213	Diode outline (~MELF)	JEDEC DO213-D	SM.LLB	SM/DO213 (AA, AB, AC; +variations)
DO-214 (see SMA, etc.) (See also SOT, DPAK, D2PAK packages)	Diode outline (molded)	JEDEC DO214-D	SM.LLB	SM/DO214 (AA, AB, AC; +variations)
Inductor, chip	0805, 1206, etc.	(see Resistor, chip)	SM.LLB	SM/L_0805...SM/L_3312 etc.
Inductor, molded		IMC-2220 (see Vishay Web site)		–
Inductor, wire wound	Power SMD inductor	MSS5131 (see Coilcraft Web site)		–

Table C-2 A List of Common Discrete Component Packages

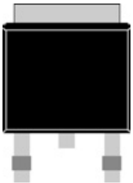
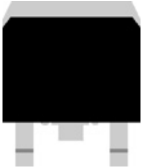
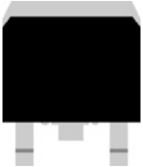
Name	**Package outline**	**JEDEC DWG No.**	**Variation—pitch**	**Layout (Lib: Footprint)**
DPAK (TO-252)		TO252-E	AA–0.090 in. (3-lead) AB–0.090 in. (3-lead) AC–0.090 in. (3-lead) AD–0.045 in. (5-lead)	(3-lead only) TO: TO252AA/DPAK TO252AB/DPAK SM: SM/_DPAK
D2PAK (TO-263)		TO263-D	AA–0.100 in. (4-lead) AB–0.100 in. (3-lead) BA–0.067 in. (6-lead) BB–0.067 in. (5-lead) CA–0.050 in. (8-lead) CB–0.050 in. (7-lead)	TO: TO263AA TO263AB
D3PAK (TO-268)		TO268-A	AA–5.45 mm (4-lead)	None

Table C-3 Discrete Package (DPAK)

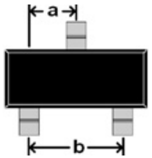
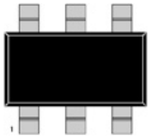
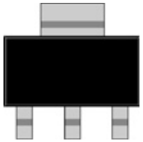
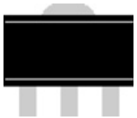
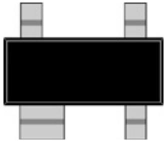
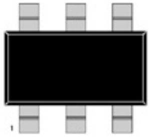
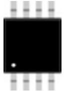
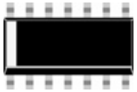
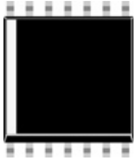
Name	Package outline	JEDEC DWG No.	Variation—pitch	Layout (Lib: Footprint)
(all 3-lead) SOT23-3 SC-59 SSOT-3 (1.9 mm)		TO-236	AA–0.95 mm (a) AB–0.95 mm (a) –1.90 mm (b)	TO: TO236xx/SOT23 SM: SM/SC59_xxx
SOT23-5 (5-lead) EIAJ SC-74A (5-lead) SOT-26 (6-lead) SOT23-8 (8-lead)		MO178-C MO193-C	AA–0.95 mm (5-lead) AB–0.95 mm (6-lead) BA–0.65 mm (8-lead)	None
SOT223-3 (4-lead) SOT223-4 (5-lead)		TO261-C	AA–2.30 mm (4-lead) AB–1.50 mm (5-lead)	(4-lead only) SM: SM/SOAT223_xxxx TO: TO261AA/SOT223
SOT-89 (2- & 3-lead)		TO243-C	AB–3.0 mm (2-lead) AA–1.5 mm (3-lead)	TO: TO243AB/SOT89-2 TO: TO243AA/SOT89 SM: SM/SOT89_xxx
(4-lead) SOT-143 SOT-343		TO253-D (EIAJ SC-61B)	AA–1.92 mm –1.30 mm	SM: SM/SOT143_xxx TO: TO253AA/SOT143 (SOT-143 only)
SOT-353 (5-lead) SC-88 (5-lead) SC70 (6-lead) SC-74 (8-lead) SSOT-n (5, 6, 8-leads)		MO059-B MO203-B	AA–0.65 mm (5-lead) AB–0.65 mm (6-lead) BA–0.50 mm (8-lead)	None

Table C-4 Some of the Small Outline Transistor (SOT/SSOT/SC) Packages

Name	Package outline (No. leads)	JEDEC DWG No.	Variation—pitch	Layout (Lib: Footprint)
MSOP Body width 2.3 mm, 2.8 mm, 3.0 mm	 (8, 10)	MO187-E	AA–0.65 mm (8-lead) AA–T–0.65 mm (8-lead) DA–0.65 mm (8-lead) CA–0.50 mm (8-lead) BA–0.50 mm (10-lead) BA–T–0.50 mm (10-lead)	None (note: also called TSSOP in some applications)
SOIC Narrow body (0.150 in.) (3.8 mm)	 (8, 14, 16)	MS012-E	Width at lead–0.236 in. (6.0 mm) Pitch–0.050 in. (1.27 mm) Lead width–0.016 in. (0.40 mm) Lead spacing–0.034 in. (0.87 mm)	SOG: SOG.050/xx/WG.244/L.xxx
SOIC Wide body (0.300 in.) (7.5 mm)	 (14, 16, 18, 20, 24, 28)	MS013-E	Width at lead–0.403 in. (10.3 mm) Pitch–0.050 in. (1.27 mm) Lead width–0.016 in. (0.4 mm) Lead spacing–0.034 in. (0.87 mm)	SOG: SOG.050/xx/WG.420/L.xxx

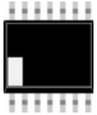
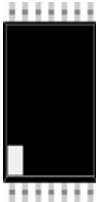
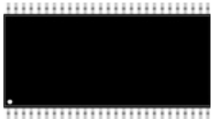
SSOP Narrow body (0.150 in.) (3.8 mm)	 (14, 16, 18, 20, 24, 28)	MO137-C	Width at lead–0.236 in. (6.0 mm) Pitch–0.025 in. (0.635 mm) Lead width–0.010 in. (0.25 mm) Lead spacing–0.015 in. (0.385 mm)	SOG: SOG.65M/xx/WG8.20/Lxx
SSOP Wide body (0.300 in.) (7.5 mm)	 (28, 48, 56, 64)	MO118-B	Width at lead–0.410 in. (10.4 mm) Pitch–0.025 in. (0.635 mm) Lead width–0.010 in. (0.25 mm) Lead spacing–0.015 in. (0.4 mm)	SOG: SOG.025/xx/WG.420/L.xxx SOG.65M/xx/WG14.20Lxx
SOP	 (44 - 90...)	MO174-A MO175-A MO180-B	Various package configurations	SOG: SOG.80M/64/WG14.50/L26.43

Table C-5 Some of the Small Outline Integrated Circuit (SOIC/SOP/SO) Packages

Package	Name	JEDEC standard(s)
DIP	Dual inline package (0.100-in. pitch)	MS001-D, TO250-A, MO043-A
DO-15 (DO-41 glass/plastic)	Diode outline	DO204B-D
DO-35	Diode outline	DO-204-AH
IPAK (TO-251)	Transistor outline, flange mount	TO251-D
I2PAK (TO-262)	Transistor outline, flange mount	TO262-A
TO-205AF/TO-39	Transistor outline	TO205-E
TO-3P/TO-41/TO-247AD	Transistor outline	TO204-C
TO-92	Transistor outline	TO226-G
TO-92; TO-18, lead form STD	Transistor outline	TO226-G, TO206-B
TO-126	Transistor outline	(Similar to TO-220)
TO-218AC	Transistor outline	TO218-E
TO-220 (and variations)	Transistor outline	TO220-K, TO262-A
TO-226AE	Transistor outline	TO226-G
TO-247, 2L, 3L	Transistor outline	TO247-E_01
TO-264	Transistor outline	TO264-B

Table C-6 Some of the Common Through-hold Packages

JEDEC doc.	JEDEC title
MO-151	Elevated to MS-034A. MS-034A was revised and became MS-034B, 2/20/03.
MO-156	Square ceramic ball grid array (BGA) family, 1.00, 1.27, and 1.50 mm pitch, CBGA.
MO-157	Rectangular ceramic BGA family, CBGA.
MO158-D	The addition of 47.5, 50.0, 52.5, and 55.0 mm body variations with 1.27 and 1.00 mm ball pitch to column grid array registration.
MO163-B	Replaced by MS-028-A.
MO-192	Low profile square ball grid array family.
MO-195	Thin, fine pitch ball grid array family, 0.5 mm pitch.
MO-205	Low profile, fine pitch BGA family, 0.80 mm pitch (rectangular).
MO-207	Square and rectangular die-size, ball grid array family.
MO-210	Thin, fine pitch, rectangular ball grid array family, 0.80 mm pitch.
MO-211	Die size ball grid array, fine pitch, thin/very thin/extremely thin profile.
MO-216	Thin profile, square, and rectangular BGA family, for 1.00 and 0.80 mm pitch.
MO-219	Low profile, fine pitch ball grid array (FBGA) registration, 0.80 mm pitch (square and rectangle).
MO-221	Extremely thin, two row cavity down, 0.50 mm pitch BGA family.
MO-222	Ceramic BGA rectangular.
MO-225	Addition of variations AB and BC to VFBGA.
MO-228	Square, dual pitch and FBGA family.
MO-233	Mixed pitch (0.80 and 1.00 mm), rectangular die size, fine dual pitch ball grid array (DSBGA) family.
MO-234B	Low profile rectangular ball grid array family.
MO-237E	DDR2 SDRAM DIMM package with 1.00 mm contact centers.

Table C-7 A List of Ball Grid Array Standards (Continued)

JEDEC doc.	JEDEC title
MO-242B	Rectangular die-size, stacked ball grid array family, 0.80 mm pitch.
MO-246C	Rectangular, fine pitch, thin ball grid array, 0.65 mm pitch.
MO-261A	Thick and very thick, fine pitch, rectangular ball grid array family, 0.80 mm pitch.
MO-264A	Rectangular die-size, stacked ball grid array family, dual pitch.
MO-266A	Very thin, fine pitch, stackable BGA family, 0.50 mm pitch.
MO-273A	Upper pop package, square, fine pitch BGA, 0.65 and 0.50 mm pitch.
MO-275-A	Low profile, fine pitch ball grid array family, square.
MO-280A	Ultra thin and very, very thin profile, fine pitch BGA family.
MO-028-C	Addition of rectangular BGA variations to BGA family.
MS-034-D	Elevation of registration MO-151, plastic BGA, 1.0, 1.27, 1.5 mm pitch, with increased ax dimensions to allow for thicker packages.

Because there are so many types and variations, only some of the JEDEC standards and titles are listed here.

Table C-7 (Continued)

JEDEC doc.	JEDEC title
MO-134-A	Ceramic quad flatpack family (CQFP), 0.50 mm lead pitch with ceramic nonconductive tie bar.
MO-143-C	Replaced—see MS-029-A.
MO-148-A	Multichip module (MCM) ceramic quad flatpack family, S-CQFP.
MO-188-B	Power PQFP with heat slug.
MO-189-A	Plastic QFP/heat slug (H-LQP/G) 2.00 mm thick/2.00 mm footprint.
MO-198-A	3-tier family, PQFP-B.
MO-204-B	Plastic quad flatpack (PQFP) outline with exposed heat sink, thermally enhanced PQFP's.
MO-220K	Thermally enhanced plastic very thin and very very thin fine pitch quad flat no lead package.
MO-239-B	Thermally enhanced plastic very thin dual row fine pitch quad flat no lead package.
MO-241-B	Dual in-line compatible, thermally enhanced, plastic very thin fine pitch, quad flat no lead package family.
MO-243-A	Thermally enhanced plastic very thin and very very thin fine pitch bumped quad flat no lead package.
MO-247C	Plastic quad no lead staggered multirow packages.
MO-248E	Thermally enhanced plastic ultra thin and extremely thin fine pitch quad flat no lead package.
MO-250-A	New family of thermally enhanced plastic very thin and very very thin pitch bumped quad flat no lead packages.
MO-251-A	Thermally enhanced plastic very thick, quad flat no lead package.
MO-254-A	Thermally enhanced plastic low and thin profile fine pitch quad flat no lead package.
MS026-D	Standard–low/thin profile plastic quad flat package, 2.00 mm footprint, optional heat.
TO271-A	4 lead quad flat pack.

Table C-8 A List of Quad Flat Packs Standards

JEDEC doc.	JEDEC title
MO-220K	Thermally enhanced plastic very thin and very very thin fine pitch quad flat no lead package.
MO-241-B	Dual in-line compatible, thermally enhanced, plastic very thin fine pitch, QFN package family, includes addition of very thin profile variations.
MO-247C	Plastic quad no lead staggered multirow packages.
MO-255-B	Plastic very very thin, ultra thin, and extremely thin, fine pitch quad flat small outline, nonleaded package family.
MO-257-B	Plastic fine pitch quad no lead staggered two row thermally enhanced package family.
MO-262A	0.50 mm pitch very thin and very very thin flange-molded thermally enhanced (top side) QFNs.
MO-263A	0.50 and 0.40 mm pitch very thin and very very thin flange-molded QFNs.
MO-265A	Thermally enhanced plastic very thin fine pitch quad flat no lead package, including corner terminals.
MO-267B	Punch-singulated, fine pitch, square, very thin, leadframe-based quad no lead staggered dual-row QFN package family.

Table C-9 A List of Some Quad Flat Packs–No Lead (QFN) Standards

JEDEC doc.	JEDEC title
MO041-C	0.050 in. center leadless rectangular chip carrier type E, variations AA–AF
MO042-A	0.050 in. center leadless rectangular chip carrier type F.
MO044-A	Leaded ceramic chip carrier 0.050 in. center, 68 and 84 terminals, item 11.11-138.
MO047-B	Plastic chip carrier (PCC) family, 0.050 in. lead spacing, square, item 11.11-242
MO052-A	Replaced—see MS-016-A. PCC family 0.050 in. lead spacing, rectangular).
MO056-A	Ceramic 0.025 in. center chip carrier.
MO057-A	Ceramic 0.020 in. center chip carrier.
MO062-A	148 pin leadless ceramic chip carrier, 0.025 in. pitch.
MO075-A	0.050 in. center nonhermetic leadless chip carrier quad series, square.
MO076-A	0.050 in. center nonhermetic leadless chip carrier SO series, rectangular
MO107-A	Ceramic multilayer leaded chip carrier, 0.050 in. pitch, J-bend leadform, 20 mil min.
MO110-A	Round lead, J-form square body, 0.050 in. pitch center ceramic chip carrier.
MO111-A	Family of round leads, 0.050 in. pitch, gull-wing leadform, center ceramic chip carrier.
MO126-B	Leadless small outline ceramic chip carrier, 0.400 in. body, 0.050 in. pitch, 28, 32, 26 leads, variations AA–AC.
MO129-A	Top brazed ceramic leaded chip carrier (0.020 in. lead pitch) with plastic nonconductive tie bar.

Table C-10 A List of Some Leadless Chip Carrier Standards (Continued)

JEDEC doc.	JEDEC title
MO130-A	Top brazed ceramic leaded chip carrier (0.015 in. lead pitch) with plastic nonconductive tie bar.
MO131-A	Top brazed ceramic leaded chip carrier (0.025 in. lead pitch) with plastic nonconductive tie bar.
MO144-A	Leadless small outline ceramic chip carrier, 0.350 in. body, 0.050 in. pitch, R-CDCC-N.
MO147-A	Small outline J-lead ceramic chip carrier, 0.415 in. body, 0.050 in. lead spacing.
MO217-B	Very very thin quad bottom terminal chip carrier family with addition of variations AE, AF, AG, BE, BF, and BG.
MS002-A	0.050 in. leadless chip carrier, type A, variations AA–AH.
MS003-A	0.050 in. leadless chip carrier, type B, variations BA–BH.
MS004-B	0.050 in. center leadless chip carrier, type C, variations CA–CH.
MS005-A	0.050 in. center leadless chip carrier, type D, variations DA–DH.
MS006-A	0.050 in. center leaded chip carrier, 24 terminal leaded, type A.
MS007-A	0.050 in. center lead chip carrier, type A, variations AA–AH.
MS008-A	0.050 in. center lead chip carrier, type B, variations BA–BH.
MS009-A	0.040 in. center leadless chip carrier packages, variations AA–AJ.
MS014-A	Single layer chip carrier family, 0.040 in. terminal spacing, ceramic, variations AA–AJ.
MS016-A	PCC family, 1.27 mm/0.050 in. lead spacing, rectangular.
MS018-A	Square plastic chip carrier family, 1.27 mm/0.050 in. pitch.

Table C-10 (Continued)

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Appendix D

Rise and Fall Times for Various Logic Families

Logic family		Transition Time (ns)		Rank (fastest)
		RT	FT	
BiCMOS	ABT	1.6	1.4	14
	BCT	0.7	0.7	12
	LVT	2.7	2.8	29
CMOS	AC	1.7	1.5	15
	ACT	1.7	1.5	25
	ACQ	2.4	2.4	16
	ACTQ	2.5	2.4	27
	AHCT	2.4	2.4	26
	C	35	25	39
	FCT	1.5	1.2	13
	HC	3.6	4.1	33
	HCT	4.6	3.9	34
	LCX	2.9	2.4	28
	LV	3.0	3.0	30
	LVQ	3.5	3.2	31
	LVX	4.8	3.7	35
	VCX	2.0	2.0	20
	VHC	4.1	3.2	32
ECL	10K	2.2	2.2	22
	10KH	1.7	1.7	17
	100K	0.6	0.6	11
	300K	0.5	0.5	**10**
	E	0.38	0.38	**8**
	EP	0.11	0.11	**6**
	LVEL	0.22	0.22	**3**

(*Continued*)

Logic family		Transition Time (ns)		Rank (fastest)
		RT	FT	
	EL	0.23	0.23	**5**
	SiGe-2.5 V	0.02	0.02	**1**
	SiGe-3.3 V	0.3	0.03	**2**
GaAs		0.3	0.1	**4**
LVDS		0.3	0.3	**7**
SSTL		0.3	0.5	**9**
TTL	74nn	8.0	5.0	36
	ALS	2.3	2.3	24
	AS	2.1	1.5	18
	F	2.3	1.7	21
	FR	2.1	1.5	19
	H	7.0	7.0	37
	L	35	30	40
	LS	15	10	38
	S	2.5	2.0	23

Partial data from IPC-2251 and Coombs.

Appendix E

Drill and Screw Dimensions

Screw size No. or Diam.	Threads per inch	Clearance hole (drill diameter)						Head diam. Typ. (in.)	Washer diam. typ. (in.)	Nut size (in.)
		Close fit		Normal fit		Loose fit				
		Drill bit gauge	Min. (in.)	Drill bit gauge	Med. (in.)	Drill bit gauge	Max. (in.)			
0	80	No. 51	0.067	No. 48	0.079	$^{3}/_{32}$	0.104	0.116	0.188	$^{5}/_{32}$
1	72 or 64	No. 46	0.081	No. 43	0.092	No. 37	0.114	0.141	0.219	$^{5}/_{32}$
2	64 or 56	$^{3}/_{32}$	0.094	No. 38	0.105	No. 32	0.126	0.167	0.250	$^{3}/_{16}$
3	56 or 48	No. 36	0.106	No. 32	0.119	No. 30	0.140	0.193	0.312	$^{3}/_{16}$
4	48 or 40	No. 31	0.120	No. 30	0.130	No. 27	0.156	0.219	0.375	¼
5	44 or 40	$^{9}/_{64}$	0.141	$^{5}/_{32}$	0.160	$^{11}/_{64}$	0.184	0.245	0.406	¼
6	40 or 32	No. 23	0.154	No. 18	0.174	No. 13	0.197	0.270	0.438	$^{5}/_{16}$
8	36 or 32	No. 15	0.180	No. 9	0.200	No. 3	0.225	0.322	0.445	$^{11}/_{32}$
10	32 or 24	No. 5	0.206	No. 2	0.225	B	0.250	0.373	0.500	$^{3}/_{8}$
¼	28 or 20	$^{17}/_{64}$	0.266	$^{9}/_{32}$	0.286	$^{19}/_{64}$	0.311	0.492	0.625	$^{7}/_{16}$
$^{5}/_{16}$	24 or 18	$^{21}/_{64}$	0.328	$^{11}/_{32}$	0.349	$^{23}/_{64}$	0.373	0.615	0.688	$^{9}/_{16}$
$^{3}/_{8}$	24 or 16	$^{25}/_{64}$	0.391	$^{13}/_{32}$	0.411	$^{27}/_{64}$	0.438	0.740	0.813	$^{5}/_{8}$

Table E-1 English Sizes

Screw size	Pitch (mm)	Clearance hole fit			Head/nut size	Washer diameter
		Close	Normal	Loose		
M 1.6	0.4	1.7	1.8	2.0	2.9	3.2
M 2.0	0.4	2.2	2.4	2.6	3.6	4.0
M 2.5	0.5	2.7	2.9	3.1	4.5	5.0
M 3.0	0.5	3.2	3.4	3.6	5.4	6.0
M 4.0	0.7	4.3	4.5	4.8	7.2	8.0
M 5.0	0.8	5.3	5.5	5.8	9.0	10.0
M 6.0	1.0	6.4	6.6	7.0	10.8	12.0
M 8.0	1.3	8.4	9.0	10.0	14.4	16.0
M 10	1.5	10.5	11.0	12.0	18.0	20.0

Table E-2 Metric Sizes (mm)

Appendix F

References by Subject

Component Package Types and Mounting (SMD)

IPC-7351, Section 8.0, pp. 44–70.

IPC-D-330, Section 5.

(see also Land Patterns)

Component Placement, Spacing, and Orientation

General considerations

IPC-1902 (grid resolution considerations).

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IPC-7351, Section 3.4, p. 20 (SMD).

IPC-AJ-820.

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Land Patterns (Footprint Design)

SMD

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(see Lead Relationships)

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Lead Relationships

Lead-to-hole ratio

IPC-AJ-820, Section 2.5.2, p. 2-11.

IPC-SM-780, Section 8.6.1.5, p. 103.

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Lead bend radius and spacing

IPC-2221A, Fig. 8-9, p. 61.

IPC-AJ-820, Section 2.5.1.4, p. 2-11; Section 2.5.3.1, p. 2-13.

IPC-CM-770, Section 11.1.8, p. 67.

IPC-D-330, Section 11, Fig. 11-8, p. 12.

IPC-SM-780, Section 8.4.2, p. 94.

Materials

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General design information

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IPC-7351, Section 1.2.1, p. 2.

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Assembly types

IPC-2222, Section 1.5.1, Fig. 1-1, p. 1.

IPC-AJ-820, Section 1.3.2, Fig. 1-1, p. 1-5.

IPC-CM-770E, Sections 1.2.2, 1.2.4, p. 1.

Density levels

IPC-7351, Section 1.4, p. 2.

Producibility levels

IPC-2221A, Section 1.6.3, p. 2.

IPC-7351, Section 1.3.1, p. 2.

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Power distribution concepts

IPC-2221A, Figs. 6-1, 6-2, 6-3, p. 38.

Sizes/panels

IPC-2221A, Fig. 3-5, p. 14; Fig. 5-1, p. 28.

Testing

IPC-2221A, Sections 3.5–3.5.6, p. 7-12.

Plated Through-holes

Types: through, blind, buried, mounting holes

IPC-2221A, Section 9.2, p. 75.

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IPC-2222, Section 9.3, p. 20.

IPC-D-330, Section 6.18, Tables 6-29 through 6-32, p. 53.

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(see also Lead Relationships)

Hole-to-land ratio

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Land requirements

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Components, orientation

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Components, mounting

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Stripline

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Asymmetric stripline

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(see also Transmission Lines)

Transmission Lines

Characteristic impedance (microstrip, stripline topologies, etc.)

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Index

**on Net spreadsheet, 305
&COMP, & PACK, & VALUE, 220–221
0/GND symbol (for PSpice simulations), 199, 361, 365
10-W rule, trace spacing, 164
3w rule, trace spacing, 163–164

A

Absolute dimensions, 294–296
Add,
  Capture Library, 18, 21
  Free Via, 311–313, 345–351, 372, 382–386, 391, 395, 397
  Layout Library (.LLB), 267, 288
  parts to the placement queue, 297–298
  pins to a part, 176
  ports to a schematic, 203
  PSpice model to an existing Capture part, 195, 206
AGND, 127, 322–329, 335–337, 353–359, 367, 372–377
Allegro PCB Router, 429, 437
American National Standards Institute (ANSI), 67, 76–8, 119
Ampere–Maxwell Law, 118
Annotation, 47, 282
  back annotation, 43, 47, 53, 319, 321, 392
  Capture schematic, 282
  forward annotation, ECO to Layout, 47, 288–290, 372
Annular ring, 69–71
  breakout, 70–71
  width, design, PTH land dimension, 103–105, 227, 237–238
Anti-copper, 334–338, 349–351, 395–396
Aperture 48, 62–64, 437
Aspect ratio (AR) (PCB-thickness-to-drill-hole relationship), 76–77
Assembly, 79
  automated processes (pick and place), 15, 80–81, 84, 98
  automated process steps, 15, 79–84, 145
  Gerber files (.AST and .ASB), 14, 80, 408
  layer (.AST, .ASB), 14, 28, 61
  layers, hide and display in Layout, 296
  manual, 79
  rates, automated processes (SMDs, THDs), 80
  types, 69, 79
Asterisk (* or **) on nets spreadsheet, 305
AutoECO, 25–28, 44–47
  types of, 401
  updating an existing board, 288–290, 372
Autopath Route Mode (Interactive manual routing tools), 32, 53, 55, 342, 370
Autorouter, types of 57
Autorouting, 32–34, 55, 56–9, 316–320, 340, 370
  using SPECCTRA, 429,
  using the DRC route box, 370
Axial-leaded and radial-leaded devices, 80
  footprint design, 101–103, 214, 221, 237–239

B

Back Annotate,
  general from Layout to Capture, 43, 47, 53
  in Capture, 321, 394
  in Layout, 53, 321, 392, 400, 406
  swap information (to Capture), 43, 393–394

Back Annotate (*continued*)
  synchronizing Layout and Capture, 43, 283, 319, 394
Background noise, 109
Bad Pad Exits, 34, 59, 397
Balanced Stripline, 133, 149–150, 487
Ball Grid Array, Footprint design, 214, 243, 248
Barrel (plating in a PTH), 10, 82, 106
Bed-of-nails testing, grid, 85
Bill of Materials (BOM),
  examples of, 277–279, 282, 379, 427
  sorting and customizing in Microsoft Excel, 427
Blind Via, 358, 355, 367
  blind via setup example, 367–371
Board house, submitting designs to, 77, 79, 411–422
Board outline, 11, 14, 72, 87–93, 419
  how to draw/make, 29–30, 289, 291, 396, 403
  Obstacles, 30–31, 52, 218
Board templates (.TPL file extension), 43, 403, 407–408
Board warpage, 147
Breakout and annular ring control, 70–71, 76, 227, 237, 350, 480
B-stage laminate, 3
Built-up PCBs, 4, 258, 404
Bulk capacitors, 147, 299
Buried vias, 4, 258
Busses, 327, 359
Bypass capacitors and fanout, 151, 310, 412

C
Cache, design, 39, 42
  Cleanup, 283, 398, 400
  Replace, 399, 400
  Update, 399
CAD Tools, 1
  using to 3-D Model a PCB, 452
Capacitance, interplane, 147
Capacitive coupling, 112, 117
Capacitors, 151, 207, 216, 242, 258, 279
  models/libraries, 207, 271
  routing/fanout, 310–313
Capillary action, 84, 103–104
Capture,
  adding parts to library list, 18, 21, 271
  database file (.DBK), 43
  design file (.DSN), 42, 191, 198
  library file (.OLB), 167, 191, 193, 271
  Library folder, 39, 167, 191, 208
  library, saving, 179
  Part Editor, 175–179, 194, 273–275, 360
  parts saving, 179
  Parts constructing, *see* Capture, Part Editor
  project file (.OPJ), 42, 205
  Project Manager, 20, 23, 41, 179, 198, 205, 277, 281–285, 321, 357, 374, 394, 398, 428
  PSpice folder, 167, 191, 193, 360, 424
  symbols, constructing, 208
Catalog of a footprint library, 261
Change,
  pin name or number, 176, 178
  visibility of the pin names and numbers, 169, 178, 181–183
Characteristic impedance, 127, 138, 165
  design, 153–162
  routing, 388
  simulating, 424
Chassis shield, 352–353
Classes and Types of PCBs, 68
Cleanup,
  cache, 283, 398, 400
  routing, 34, 59–60
Clearance Area in/from plane layers, 10, 76, 103, 106–107, 218, 240, 259
Clock circuits, moated ground areas for, 390
CNC machine, making a .DRL file for, 438
Color,
  dark yellow nets, 358, 403
  net, changing, 309, 330
  Settings (Layer or Net), 53, 57, 406
Combined Property String, 277, 282
Common Ground Area, 325, 353
Common,
  ground system (daisy chain), 120
  impedance, 121–122
  reference point, 125
COMPGROUP, 281, 428
Component,
  grouping 280, 428
  outline obstacle, 218, 221, 224, 235, 241
  placement and orientation, spacing, 85–94, 101

  Selection Criteria dialog box, 297
Composites, 437
Computer numerical control (CNC), 8, 11, 14, 63, 438
Computer-aided,
  design (CAD), 1
  engineering (CAE), 1
  manufacturing (CAM), 1,
Conduction current, 118, 128
Connection tool, 52, 342, 350
Constructing,
  a part using the design spreadsheet, 187
  capture parts, 171
  capture symbols, 208
  controlled impedance traces, 153–162, 379, 387, 423
Converting a routing layer to a plane layer, 302, 315
Coordinates,
  cursor, 56, 235, 293–295
  X-Y indicator, 56, 221, 241, 383
Copper,
  anti copper, 338, 349
  area (obstacle) as part of a ground plane, 336, 339, 344
  area Obstacle Type, 218, 220, 254–257, 408
  clad, 2–4, 74
  cladding/foil thickness, Table of, 74
  foil, 2–4, 74
  heat spreader, placing, 381, 382, 385–387
  islands, 338, 348
  pour areas, Obstacles, 52, 326–328, 342, 347, 349, 390, 395, 413
  pour spacing clearance, how to change, 347
  pours, nested, 330, 336
  thickness for PTHs and vias, 73
Copying,
  graphic objects, 177, 186,
  Layers, 304
  pad properties of one layer to another layer, 315
Cores, 2–4, 9, 258, 286, 380, 404
Corners, Traces with acute and 90° angles, 164, 389
Courtyard, courtyard excess, 70, 99–101
Critical trace length, 142–143, 153, 162, 387, 424–427
Cross talk, 111, 115, 117, 125, 147, 163
  EMI reduction, 163, 352–354
Current handling, trace width, 151, 286
Curved traces, Routing, 390

D
Dark yellow nets, 358, 403
Datums and insertion origins (Footprints), 220. *see also* printed circuit board, Origin
D-Codes, 62, 64
Density Levels, 70, 96–101
Design cache, 273
  Cleanup, Replace, Update, *see* Cache
  folder, 42, 399
Design complexity levels, 44, 68, 288
Design Flow, Overview of, 17–37, 264
Design for Manufacturing (DFM), 79–107
Design levels in OrCAD Layout vs. IPC design levels, 44
Design Resources folder, 42, 191
Design rule check (DRC),
  Capture, how to, 283
  Layout, how to, 35, 54, 314
Desmear, 9, 76
Detail obstacle, 220, 223
Dialog boxes,
  Add Free Via, 312, 346, 382, 384
  Add Library (Layout), 267, 288
  Add Library… (Capture), 21, 42, 271
  AutoECO, 25–28, 43–47, 288, 290, 329, 365, 374, 403
  Cleanup Design, 34, 60
  Component Selection Criteria, 297,
  Create Netlist,
    Layout (MNL), 24, 285, 373
    PSpice, 205
  Create New Footprint, 221, 232, 245
  Display Properties, 275, 326, 360, 412
  Edit Array Alphabet, 248
  Edit Filled Graphic, 178
  Edit Layer, 303, 241, 365
  Edit Obstacle, 223–224, 335, 337, 339, 344, 350
  Edit Pad, 228, 230, 235, 376
  Edit Padstack, 230, 234, 261, 294, 367, 379, 381
  Edit Padstack Layer, 230, 240, 315, 367

Dialog boxes (*continued*)
  Edit Part Properties, 179
  Find, 280, 297
  Find Coordinate or Reference Designator, 48, 297
  Import Model Wizard, 207
  Link Footprint to Component (AutoECO DB Option), 27, 45, 290
  Modify Connections, 293, 391
  New Project, 197, 268, 356
  New Symbol Properties, 209
  Pad Array Generator, 246, 255
  Pin Properties, 176, 275
  Pin Property Editor, 274
  Place Ground, 200
  Place Hierarchical Port, 204
  Place Part, 21, 43, 199, 271
  Place Pin, 176
  Post Process Settings, 36, 415
  Save Footprint As, 225
  Select Next, 299,
  Simulation Settings, 202, 363
  System Settings, 233, 254, 297, 383, 408
  User Preferences, 375
  User Properties, 179, 210, 360
Dielectric constant, *see* permittivity, relative
Digital gate ground pin, connecting to a ground net, 183, 272, 322, 324–326, 328–336, 352–355, 359, 373–377
Dimensions, Absolute, Relative, 293–296, 389
Disable (net) after fanout, 333
Discontinuities in the return plane, 107, 123, 165
Displacement current, 128–129
Display Component information on the schematic, 412
Distortion, 110
Documentation files, 60–64
Dogbone (via), 250
Done flag, clearing, 318, 319, 395
Draws and flashes, 63–64, 165
DRC,
  Capture, Layout, *see* Design Rule Check (DRC)
  online, 29–30, 35, 53–55, 291, 311, 317
  Project, 29, 35, 53–55
DRC box,
  autorouting with, 370
  description, 29
  errors, overriding and viewing, 370
  hide and display the, 29, 289
  setting the size of, 370
Drill,
  bit sizes, ANSI standard B19.11M, 76, 473–474
  drill file (.npt, .tap), 63, 260, 293, 414
  drill hole, diameter, padstack, 11–12, 63, 103, 217, 219, 226, 237, 240
  DRILL layer, 13, 61, 240, 254, 260, 366, 368
  Layer, how to make using, 438
  tape, 63
DRLDWG layer, 62, 240, 254, 366
Dual rail power supply, 267, 286

E

ECO, *see* AutoECO *and* Annotation, Forward
Edge (trace) definition, 75
Edit Simulation Profile, 202, 363, 425
EIA, *see* Electronic Industries Alliance
Electric fields, 4–22
Electrically long traces, 139, 153, 162
Electromagnetic (EM),
  compatibility (EMC), 111–12, 475
  interference, *see* EMI and crosstalk reduction
  waves, 130
Electronic Industries Alliance (EIA), 66, 461
Electrostatic discharge (ESD), 81
Embedded passives, 4, 258, 437
EMI and cross talk reduction, 111–12, 117, 138, 147–148, 346, 354
Enable Editing of Footprints, 375
Equal length traces, 389
Errors and Warnings,
  All sweeps completed or disabled, 318, 319
  bad pad exit, 316, 397
  markers, 53, 283, 314, 370, 408
  No connection to plane, 385
  off-grid via, 316
  viewing descriptions of, 314
Etch back,
  desmear (hole), 9, 76
  undercut (trace), 74–75
Excellon output format (a.k.a. RS-274X, Extended), 61, 63, 415
Exporting a PCB design as a .DXF file, 452
Exposing copper (solder thief), 83, 408

Extended, output format (Excellon, RS-274X),
    see Excellon output format

F
Fabrication,
  PCB, process, 2, 4
  PCB, yield %, 65, 71, 80, 94
False triggering, 138
Family, digital logic, 387, 425, 471
Fanout, 226, 251,
  automatic, 305–309,
  bypass capacitors and SMDs, 151
  board with multiple via types, 367
  Disable after, 333
  fanning out power and ground, 308, 320, 369
  fanout (stringer pad), 226
  fan-out vias, placement and spacing (soldering considerations), 83
  manually routing, 310, 327
  moving and unrouting, 311
  via assignment and specification, 312, 333, 367, 387
Faraday's Law of Induction, 113–114
Ferrite bead, 354
Fiducials, 9, 85,
File types,
  .AST, .ASB, 14, 61, 80, 224, 296, 366, 408, 419
  .DBK, 43
  .DRD, 14, 62
  .DRL, 61, 366, 438–442
  .DSN, 42
  .DXF, 452
  .ERR, 44
  .GTD, 35, 62, 437–449
  .LIB, 39–40, 192, 196, 205
  .lis, 35, 44, 62
  .LLB, 39, 213
  .log, 18, 25, 44
  .MAX, 14, 17, 26, 321
  .MNL, 17, 25, 43, 264, 280, 284, 321, 373, 402
  .model, 192
  .npt, 260, 293, 414
  .OLB, 18, 39, 167, 191, 207, 270, 323, 365
  .OPJ, 40 197, 205, 356
  .plb, 451
  .SES, 433
  .SF, 57, 288, 317
  .subcircuit, 192, 196
  .SWP, 43, 321, 394
  .tap, 14, 35, 61, 260, 293, 414, 438, 441
  .TCH, 17, 26, 43, 57, 265, 286, 403, 455–456
  .TPL, 43, 403
Film box, GerbTool, changing the size of, 446
Find,
  Find tool (Capture), 280
  Find tool (Layout), 48, 297
  Find/Goto, 50, 297
  Find/Goto (with Query Window), 50
  footprints in Layout's footprint libraries, 211–217
  parts (Capture liblist), 167
Flashes and draws, 64, 165
Floating pins, 327
Flood Planes/Pours via assignment, 381, 391
Footprint,
  assigning to a part, 276–279
  assigning to multiple parts simultaneously, 279
  catalog of, 409
  composition of, 217
  design of BGAs, 248
  design of PGAs, 243
  design of surface mount devices, 232
  design of through-hole devices, 221, 237
  Enable Editing of, 375
  finding in Layout's footprint libraries, 213, 278
  libraries, 213
  modifying, 237
  naming conventions, 213
  new, 221, 232, 243, 248
  saving, 212, 225
  spreadsheet, 225
Forced thermals to connect ground planes, 372
Forward annotation, *see* AutoECO *and* Annotation, Forward
FR4, 2, 44, 75, 131, 387
  temperature rise on, 152
Free track,
  in a footprint, 255
  Obstacle, 334, 344, 350, 354, 391, 395
Free Via, 148, 254, 312, 382
  moving, deleting, 384
  placing with a routing tool, 311, 312, 342, 346, 348, 350

Free Via (*continued*)
  placing with the Free Via Matrix tool, 383, 395
Frequency response, 110, 203

G
Gate swapping, 392, *see also* Swap
Gerber files, 14, 35, 60–62, 75, 80, 221, 370, 406
  nonstandard, 422
  Opening Layout-generated files, *see* GerbTool
  submitting and requesting a quote, 408, 414, 417–418
GerbTool, 2, 47, 62, 64, 417
  intro to, 437
  open a Layout-generated Gerber (GTD) file with, 437
  panelizing a PCB, 443
  using with CNC machines, 438
Global,
  changes (layers/padstacks), 228–230, 318
  names (nets/pins/symbols) in Capture, 169, 272–273, 322, 324–326, 330, 358–360
  objects, 30, 85, 217, 225, 236, 241, 291
  spacing, 164, 347
Grid,
  Capture, graphics (lines and arcs), 170, 177, 181
  Capture, Pin placement and parts design, 170, 173, 175, 181
  Capture, Schematic/components/wiring, 19, 23, 170, 269
  Capture, Snap-to-Grid, 19, 23, 170, 173
  Layout,
    all, 58, 233
    component placement, 44, 56, 58, 85, 220
    Dimension, 295
    display and visibility, 58, 232, 242
    graphics (details, obstacles), 58, 235, 242
    padstack placement, 102, 232
    routing, 44, 58
    via placement, 44, 58, 316
Ground,
  bounce and rail collapse, 119, 123–125
  files/Gerber, 61
  layer stackups, 146, 328
  moated area, 390
  plane, 9–12, 115, 117, 119–120, 125–127
  plane area, adding to a routing layer (using copper pours/areas), 343–345, 395–397
  plane area, (removal using copper pours/areas/tracks), 334–336, 349
  plane layer, adding in Layout, 302, 304
  plane, assigning net connections to, 272, 293, 304, 308, 329–331, 367
  plane, clearance from, *see* clearance area in/from plane layers
  plane, discontinuities and slots in, 107, 123, 138, 165, 348
  plane, split, 125–127, 328, 334–336, 352
  plane, stitching manually and free via matrix, 395–397
  return plane, 115, 117, 119, 122
  single point connection on PCB, 359, 372–376
  symbol, IEEE/ANSI, 119
  symbol, placing, 325
  symbols, analog and digital, 119, 322, 324–325, 352, 358, 373
  systems, separate, series, common, parallel, 120–122, 352
Group,
  add parts to (Capture), 280
  information, viewing, 281
  placing into the queue, 297–299
Guard,
  shield, 352–355, 366
  traces and rings, 349–351

H
Harmonic distortion, 110
Heat spreader, pipes, 220, 336, 381–387
Heterogeneous, 168–169, 184
Hierarchical,
  designs, 42
  ports, 196, 203–204, 208–209
Hole,
  diameter to lead-diameter ratio and padstack design, 76, 103, 226, 237, 259
  drill sizes, 473–474
Homogeneous, 168–169, 172, 180
Hot-air solder leveled (HASL), 81
Hotkey (Layer), 56, 366

I
Image plane, 117, *see also* Ground, Return plane
Impedance,
  characteristic, 107, 127–133, 153–161, 165, 388, 424
  input/output, 138
  instantaneous, 128–129
  mismatches, 110, 137, 143, 165
Import,
  .MNL file into Layout, 25, 288
  drill (.tap file) into GerbTool, 441
Inductive coupling, 112
INNER layer template, 63
Input impedance/resistance, see impedance, input/output
Insertion,
  move/center, 237
  origins and datums (Footprint), 217, 220–221
  outlines, Obstacles, 52, 80, 218, 236
Instantaneous impedance, 128–129
Institute for Printed Circuits (IPC-Association Connecting Electronics Industries), 66
  IPC land pattern density levels, 70
  IPC Land Pattern Viewer, 66, 94, 99, 217, 232, 449–452
  IPC Standards, 457–458
Institute of Electrical and Electronics Engineers (IEEE), 667
International Engineering Consortium (IEC), 67
Interplane capacitance, 147
Intertool communication, 1, 301
Intrinsic noise, 110
Intrinsic propagation delay, (t_{PD}), 153–162, 387, 424, 427, 488
Islands of copper, 338, 347
Isolated planes (ground/power), 126, 146, 336, 352, 372

J
Joint Electron Device Engineering Council (JEDEC), 66
  package standards, 94, 98, 248, 451, 458, 459–469

L
Laminate, 2
  epoxy (core) thicknesses, 73
  etchback or desmear, 76
Land Pattern Viewer, 66, 94, 99, 217, 232, 449–452
Land Patterns for Surface-Mounted Devices, 94
Laser direct imaging (LDI), 6, 63
Layer LibName, layer templates, 60, 63, 302, 367
Layer NickName, 61–63, 303, 355, 366
Layer selection menu (list), 218–219
Layer,
  adding with spreadsheet, 302, 304
  adding using the Stack-up Editor, 404, 406
  assembly, 14, 218, 220–221, 224, 237, 296, 408
  assigning nets to, 272, 293, 304, 308, 329–331, 367
  change the name of, 63, 303
  changing the order of, 404
  Converting for routing to plane, etc., 302–303
  deleting using the Stack-up Editor, 406
  DRILL, 13, 61, 240, 260, 368
  DRLDWG, 62, 240, 366
  hiding and displaying (example), 296
  modify settings, 35, 63, 365, 404
  moving trace to, 342
  polarity of a, 419
  stack-ups, 3, 73, 146, 286, 302, 304, 328, 354, 365, 380, 403, 406, 419
  template, types, 60, 63, 303
Layout ,
  design window, 28, 46
  library, Adding, 267, 288
  netlist (.MNL) how to generate, 25, 288
  session frame, 46
  User's Guide (lay_ug.pdf), see the doc folder in OrCAD directory
Lead-diameter-to-drill-hole ratio, see hole
Length of the rising edge (transition distance, spatial extent, edge length), 138–139
Lenz's Law, 113
Level A multilayer board, 44
Library Manager, Capture, 18, 21, 172, 180, 191, *see also* Capture, Library
Library Manager, Layout, footprint library, 48, 211, 278

Link existing footprint to component, 27, 45, 290
Locking traces,
  after fanout, enabling and disabling, 306, 311, 333
  how to, 34, 59, 313
Logic families, RT and FT of, 387, 425, 471
Loop inductance, 115–117, 127, 129, 131, 147, 348, 352
Lumped-element model, transmission line, 128

M
Machine-vision-assisted assembly, 85
Magnetic fields, 112
Manual,
  assembly processes, 79
  routing fanouts/vias/test points, 310, 316, 382, 400
  routing traces, 32, 54, 59, 342, 434
  soldering, 81
Mass soldering processes, 81
Matching impedances,
  General, *see* impedance, mismatches
  source to transmission line, 144
  transmission line to load, 144
Mechanically supported components, 86, 103
Microstrip transmission line, *see* transmission lines, microstrip
Microvias, 258, 458
Military Standards (MIL-STD), 67
Milling, 8
Moat,
  creating on a plane layer, 391, 396
  ground areas planes, 125, 376, 390, 483
Mounting holes, 260, 292, 413, 480
Multilayer printed circuit boards, 69
Multipage schematic project, 352
Multipart packages and connections to, 180, 187, 272
Multiple-ground systems, setting up, *see* ground
Mutual inductance, 114, 120, 128

N
Names of nets and busses, 327, 359
Names of power pins and power symbols, 273, 324
NC drill, 441
Nested copper pours and power planes, 330, 336
Netlist,
  for PSpice, 205, 361
  for Layout, 23, 285, 373
Nets,
  assigning to ground/power planes, 272, 293, 304, 308, 329–331, 367
  color, changing, 309, 330
  enable and disable for routing, 296, 299, 302, 305, 307, 311, 313, 316, 333, 339, 369
  renaming, 327, 359
  specify the width of, *see* traces, width
  visibility, 296
New design project, how to start, 18, 268, 196–197
New Part from Spreadsheet, 172, 187
New Project dialog box, 197, 268, 356
No-connect symbol, 327
Noise, types of, 109–111, *see also* cross talk *and* EMI
Nonfunctional lands, 106
Non-soldermask-defined (NSMD) pad, 250, 252
Nonvisible power pin, *see* visibility, power pins
Not in Netlist checkbox, 260, 292

O
Obstacles, 52, 217, 218
  board outline, 29, 62, 72, 87–93, 218, 289
  component outline, 99, 101–103, 221, 224
  copper area, 220, 254–256, 338
  copper pour, 148, 163, 328, 330, 336–338, 342, 347, 349, 395
  detail, 218, 223, 235
  Free Track, 255, 334–336, 344, 350, 354, 391, 395
  insertion outline, 218, 236
  moving, 241
  Pin Attachments to, 255–256
  place outline, 87–93, 96, 99–103, 224–225, 235–236, 242, 246–248, 291, 388, 453
  resizing, 241
  silk screen, 61, 94, 221–224, 236–237, 241, 248, 408, 420, 452
  soldermask, 217, 233, 240, 249, 250, 256, 385
  solder Paste, 217
Off-page connectors, 209, 324, 357–360
Online Design Rule Check (DRC), 29, 53
Ounces (oz) of copper per square foot, 2, 132, 75

Output impedance, 138
Overbar, 358
Overriding DRC errors, 370

P
Package standards, JEDEC, 66, 94, 248, 451, 458, 459–469
Pad, see Padstack
Pad Array Generator, 243
Padless mounting hole, see Mounting hole
Padstack, *see also* Plated through-hole
  design for surface mount devices, 232
  design for through–hole devices, 237
  drill hole size, 76, 103, 226, 237, 259
  editing a single layer, 314–316
  exchanging with a different one, 234–235, 376–377
  Layout name pad vs. Capture pin, 176
  making/modifying, 227, 232, 239, 253, 375
  properties, *see* spreadsheet, padstacks
  replace with Edit pad dialog box, 314–316
  saving to the Padstack library, 228, 230, 234–235, 240, 246
  shapes, 226
  spreadsheet, 49–50, 96–98, 225, 227
  templates, 226
Panelization, 71, 84, 443–449
Parallel ground system, 120
Part,
  add a part to group, 280
  adding a library to the Libraries: list (Capture), 18, 21, 271
  assigning footprints, 276–280
  finding in libraries,
    Capture, 167
    Layout, 278
  Manager, *see* Library Manager, Capture
  outlines, Obstacles, *see* Obstacles, Silkscreen *and* Obstacles, place outline
  placement for electrical considerations, 145
  placing (Capture), 20
  placing (Layout), 31
  placing on bottom of board, 81, 297, 365
Part Editing Tools, Capture, 120, see Capture, Part Editor
Passes and sweeps, 57–59, 318
PC Board Wizard, *see* Wizards
PCB, *see* Printed Circuit Board
Permeability,
  of free space, 113, 131
  relative, 115, 131
Permittivity,
  of free space, 118, 131
  relative, 131, 162, 165, 477
Photo resist, 5
Photolithography, 5–7
  masks, negative/positive, 6
Photoplotter, 5, 11, 14, 62, 165
Pick and place, *see* Assembly, Automated processes
Pin Grid Array, Footprint design, 243
Pin Matching tool, 207
Pins, 169
  add to a part (pin tool), 170, 176, 181, 186
  attaching to obstacles, 255–256
  Capture pin name/order vs. PSpice pin name/order, 176, 206
  Capture pin number vs. Layout pad, 176
  floating errors (RtoGND), 327
  name, 173, 178, 179, 272, 274, 358
  number, 173, 178,
  power, 169, 180–183, 188–189, 272–274, 310, 324
  Properties, changing properties (multiple pins), 176
  Properties dialog boxes, 176, 179
  properties spreadsheet, 177, 186–187, 188
  selection tool, Layout, 52, 221
  swapping, 392–393
  types of, 170
  visibility, 173, 179, 181, 183
Pivot, spreadsheet properties, 201, 277, 279
Place,
  grid resolution, *see* grid, Layout, component placement
  parts (Layout), 20
  parts (Capture), 31
  wires, how to, 23
Place outline, *see* Obstacles, Place outline
Place Queue, 297
Plane,
  discontinuities/slots, 107, 123, 347–348
  ground, 117, *see also* ground, return plane
  image plane, *see* ground, return plane

Plane (*continued*)
  power, 61, 147, 151, 303, 310, 328, 330, 336, 419, *see also* VCC
  return plane, *see* ground, return plane
Plane layer, *see* Layer
PLANE layer, template, 60–61, 63, 240, 303, 316
Plane-to-plane connector,
  shorting strip, 126, 352, 354, 369
  thermal reliefs, 372
Plated through-hole (PTH), 9, 71, 76, 103–106, 218, 238, 258–259
Polarity of a layer, 419
Polyline, 171, 186
Postage Stamp View, 56
Postprocessor,
  Gerbers, *see* Gerber files
  report, 416
  setting up and running, 35, 37, 60, 63, 370, 416
Power distribution system, 123–125
Power pins, *see* Pins, Power
Power plane, net connections to, *see* Layer, Assigning nets to
Power symbols, 209, 272–274, 358
Prepreg,
  description and use, 3, 73, 149–150, 404, 477
  types and thicknesses of, 74 (Table 4–5)
Primary net/plane, 330, 336, 413
Primitive models (.model), 192–194
Printed circuit board (PCB),
  3-D Model of using CAD tools, 452
  assembly subclass, 69
  built-up, 4, 258, 458
  classes and types of, 68
  cores, 2–4, 9, 258, 286, 380, 404
  Design Flow, 1–15, 17–37, 264
  fabrication types, 69
  land pattern density Levels, 70
  origin, 28–29
  panelizing, see panelization
  PCB-thickness-to-drill-hole relationship, *see* aspect ratio
  performance classes, 68, 479
  postprocessing, 14, 35, 60, 62, 408, 411–422
  power distribution system, 123, *see also* ground and VCC
  producibility levels, 68, 479
  registration tolerances, 70
  stack-ups, *see* Layer, Stackups
  standard panel sizes, 71, 446
Project Manager, *see* Capture, Project manager
Propagation time (PT), 138–139, 142, 153, 162, 387, 424, *see also* Intrinsic propagation delay
Propagation velocity, 138, 162, 427
Property Editor spreadsheet, 201, 279, 281, 412
PSpice,
  Capture parts design with PSpice, 172, 176, 183, 190–195
  library list (lib_list.pdf), 167
  model (.mod), 194–196
  model from Capture circuit simulation, 196–206
  Model Editor, 192–198
  model Library (.LIB), 21, 40–43, 167, 190
  probe window, 203, 362–364
  project template (.opj), 357
  simulating transmission lines (using PSpice), 423
  simulation profile, 202, 361–363, 425
  simulations, 202–203, 355, 423–425
  templates, 40, 196–198, 206, 361
PT, *see* Propagation time

Q
Query window, 50, 53, 54
Queue, 297–298
  adding parts to, 298
  place the next part automatically, 298
  placing groups into the, 298
  placing parts into the, 298
  selecting a particular part from the, 298

R
Radial- and axial-leaded devices and design, 80, 103
Rail collapse, 123–125
Rat’s nest, 31, 46, 53, 55, 296, 307, 311–313, 318, 333, 338, 350, 358
Receipt inspection and testing, 422
Reconnect Mode, 53, 296
Reference designator, 48, 199, 220–221, 237, 298, 299
Reflection coefficient, 135, 138, 140–141, 424

Reflections, 133–145
Reflow soldering, *see* Solder Processes
Refresh All, 53, 307, 309, 333, 338, 343, 347, 369, 390
Registration, 9, 70, 76, 77, 103, 252, 260
Relative dimensions, *see* Dimensions, Absolute, Relative
Relative permeability, *see* Permeability, Relative
Relative permittivity, *see* Permittivity, Relative
Reliability, 65, 68, 69, 71
Renaming a schematic folder, 198
Replacing parts in the design cache, *see* Cache, Replace
Resizing obstacles, *see* Obstacles
Return plane, 107, 115, 117–120, 122–127, 146–148, 162, *see also* Ground, Return plane
  discontinuities/slots, *see* ground, plane, discontinuities and slots
Right-hand rule for electric generators, 112, 114
Ringing, 137–143, 165, 423
Rise time (RT), 113, 122, 138–139, 142, 143, 151, 153, 165, *see also* Logic families
Rising (Falling) edge, length of, 139
Round place outline obstacle, 242, *see also* Obstacles, place outline
Route Box (Online DRC), 53, 55, 58, 317
Route Pass Done flag, clearing, 318, 320
Routing,
  autoroute, see autorouting
  controlled impedance traces, 153–162, 379, 387, 423
  curved traces, 390
  layer, adding, *see* layer, adding
  layer, converting to a plane layer, *see* layer, converting
  statistics, 53, 318, 395
  strategy file, loading and editing, 48, 57, 63, 288, 317, 340, 413
  strategy parameters, 317
  enable and disable nets, *see* Nets
  manual routing tools, Routing traces, 32, 54–55, 59
    Add/Edit Mode (Manual routing tool), 32, 34, 55, 307, 311, 342, 350, 383, 388, 397
    Autopath Route Mode (Interactive manual routing tool), 55, 342, 370
    Edit Segment Mode (Manual routing tool), 32, 34, 55, 311–313, 342, 383, 395
    Shove Track Mode (Interactive manual routing tool), 32, 53, 56, 334, 337, 342
RS-274D, RS-274X (Excellon, Extended) output formats, 61–62, 63, 214, 414
Rise time (RT and FT) of logic families, *see* Logic families
RtoGND, 327

S

Save,
  capture library, Capture part, 179
  layout board design, 48
  layout footprint, 225, 229–230, 234
  layout library, 221, 229, 234
  layout padstack, 228, 229–230, 234, 240
  layout technology files, 407–408, *see also* templates
  PSpice Library, 195–196, *see also* PSpice model library
  PSpice model, *see* PSpice model
Schematic page, 19–23, 42, 198–199, 204, 269, 283, 298, 362, 402
  adding to a schematic folder, 356–357
  changing the name of, 356–357
  multi-page projects, 352, 356–357
Secondary net, 336–337, *see also* Nets, Assigning to ground/power planes
Select Next dialog box (Layout), 298–299
Selection tools (Capture), 170
Selection tools (Layout), 47, 50
Self-alignment, 84, 248, 252
Self-induced electromotive force, 113
Self-inductance, 113, 115, 117
Separate ground system, 120, 326, 352, *see also* Ground, Systems
Sequential, reflow—wave soldering, 80
Series connected ground system, 120, *see also* Ground, Systems
Settling time, 141
Shadowing, solder, 83, 252
Shape-based autorouter, 57, 429
Shared pins, 168, 172, 180, 183, 184, 189, 272
Shield layer, 353, 355
Signal-to-noise ratio, 109

Silk screen, 11, 13, 14, *see also* Obstacles, Silk screen
Simulation, profile, settings, etc., *see* PSpice, Simulation profile
Slots in the ground (return) plane, *see* Ground, Plane, Discontinuities and slots
SMD padstack footprint design, *see* Padstack, Design for *and* Footprint, Design of
Snap-to-Grid, *see* Grid, Capture, Snap-to-Grid
SOG/SOIC/SOJ, 97–98, 213–214, 459–469
Solder,
  bridge, 11, 83, 253
  paste, 11, 80–81, 84, 217–219, 249, 258, 404
    dimensions, 107
    layer (.SPT, .SPB), 14, 61
  processes,
    intrusive/sequential, 80, 84
    mass soldering processes, 71
    reflow, 14, 77, 80–82, 84–85, 151, 389, 485
    wave, 80–85, 408, 443, 476, 485
  thief, 38, 408
Soldermask (Solder resist), 4, 11–15, 61, 70, 77, 107, 163, 218–219, 218–219, 250–252, 287, 382, 404, 420, *see also* Obstacles, Soldermask; Tented via; Heat spreader; and Solder, Thief
SPECCTRA, 1, 64, 340, 392, 429–437
Split ground planes, *see* Ground, Plane, Split *and* Layer, Assigning nets to
Spreadsheets, 49, 221
  browse (Pin), 176–177
  color, 57
  error, 314, 370, 397
  footprints, 225–226, 242
  layers, 56, 303–304, 365, 379, 404
  net, 296, 299, 301–307, 311, 358, 368, 379
  new Part, 172, 187
  padstacks, 98, 226–229, 231–234, 239, 245, 253, 259, 293, 314, 375
  postprocessor, 35–36, 63, 414
  property Editor (Capture), 201, 206, 227, 279, 281, 326, 361, 412
  spacing, 164, 347
  statistics, 53, 395
  text, 221, 223
Stack-up drawing, *see* Stack-Up Editor
Stackup Editor, 304, 404–408
Stack-ups, *see* Layer, Stack-ups
Standard Fabrication Allowances (SFAs), 44, 70, 79
Standard Hole Dimensions, 76, *see also* Hole
Standard panel sizes, 71–72, 458, 479
Standards Organizations, 66, 457–458
Statistics, routing etc., 53, 318–320, 395
Stencil, solder, *see* Obstacles, Soldermask *and* Soldermask
Stitching a ground plane, *see also* Ground, Plane, Stitching
  free via matrix, 395
  manually, 348
Strategy files (.SF), 57, 59, 63, 288, 319, 340
  loading, 317
Stringer pad, *see* Fanout
Stripline, *see* Transmission lines, Stripline
Subcircuit models (.subcircuit), 192, 194, 196, 198, 205
Substrate, 2–7, 73, 251, 458
Surface Microstrip, *see* Transmission lines, Microstrip
Surface tension (solder), 83
Surface-mount (SMD, SMT),
  fanout, *see* fanout, bypass capacitors
  pads and design, *see* padstack, design
Swap,
  file, 393–394, *see also* back annotate
  gate/pin, *see* pins, swapping
Sweeps and passes, 53, 57–59, 318
Switching noise, 86, 109, 123–125, 146, 322, 328, *see also* Noise and EMI
Symbols, Capture, *see* Capture, Symbols; Hierarchical, Ports; Off-page connectors; Pins, Power; *and* Title block
Synchronizing the design with Capture, *see* Back Annotate

T
Tab route, 84, 443, 446
Technology Templates, files (.TCH),
  list of, 44, 455–456
  selecting, 17, 26, 43, 57, 265, 286, 403, 455, *see also* file types/.TPL
Templates, creating custom,

- capture projects, 403
- creating with the Stackup Editor, 407
- layout technology/template files, 403

Tented via, 11, 250, 253, 258, 345, 380
Test points, Adding, 400
Text, 52, 220–221
Thermal relief, 10, 12, 53, 122, *see also* Plane-to-plane connector
Thermal stresses, 83, 85
Thief, solder, 38, 408
Through-hole technology (THT), 80, 85, 86, *see also* Padstack and Plated through-hole
thruhole.npt, 293, 414, 417, *see also* File types/.npt
thruhole.tap, 260, 293, 414, 438, *see also* File types.tap
Time domain analysis, 202, 363
Title block, how to make, 209
Tombstoning, 84
Toolbar (Capture), 20, 198
Toolbar (Layout), 47
Tooling area, 72
Traces,
- change the layer of, 342
- corners, acute and 90º angles, 164
- current, 151
- curved, 380
- edge definition, 75
- etchback, 74
- impedance, 153, 388
- locking, *see* locking traces
- moving after routed, 32, 55, 342
- spacing for voltage withstanding, 163, 487
- spacing to minimize cross talk (3w rule), 163, 487
- undercutting, 75
- width (current), 151
- width (impedance), 153, 388, 160, 162, 165
- width tolerances, 68, 76
- width, changing, 389

Trace-to-trace spacing, 106, 164
Transmission delay (TD), 424
Transmission lines, 148, 487–488
- coplanar, 148, 162
- lumped-element model, 128
- microstrip, 132, 148–150, 153–157, 380, 387, 424, 487
- stripline, 133, 148–150, 158–161
- terminations, 143, 483

U
Units, PCB how to change, 58, 232–233
Unroute,
- fanouts, 311
- traces, 34

Update (part instance), 273

V
VCC, 272–273, 322, 328, 331, 358
Via,
- Assign to fanouts, 312, 333, 367, 387
- assignment to a net, 306, 367
- blind/buried, 4, 69, 258, 352, 355, 367
- changing the grid settings, 316
- dogbone how to make, 251, 256
- for Flood Planes/Pours, 345, 381, 390
- microvias, 258
- multiple via Fan out, 367
- new, 305, 345, 349,
- specifying for fanouts, 367
- tented, 250, 253, 258, 345, 380

Visibility, power pins, 183, 272, 324, 358, *see also* Pins, Visibility
Voltage markers (PSpice probes), 202, 362
Voltage withstanding (trace spacing), 163
VPULSE (example), 424
V-score, Panelized PCBs, 446

W
Wave soldering, 82, 85, 443
Wavelengths, number of (NL), 423
Wet acid etching, 4
Width of the trace,
- current, 151
- impedance, 153, 388

Windows ToolTips, 42
Wires, how to place, 23
Wire-to-hole ratio, 238, *see* Hole
Wizards, 40
- analog or Mixed-Signal A/D, 39, 196, 355

Wizards (*continued*)
  PC Board Wizard, 18, 268, 403
  programmable Logic Wizard, 39–40
  schematic, 39–40

X
X-Y coordinates indicator, 56, 221, 241

Y
Yield, percent, PCB fabrication, 65, 71, 80, 94

Z
Z order, 336, 349
Zero (0) ground reference (0/SOURCE), 199
Zero-length power pins, 272
Zoom,
  capture, 171
  layout, 29